INTEGRATED CIRCUIT DESIGN OF SIGMA-DELTA MODULATOR FOR ELECTRIC ENERGY MEASUREMENT APPLICATIONS

Jorge Vicente De la Cruz Marin

Dissertação de Mestrado apresentada ao Programa de Pós-graduação em Engenharia Elétrica, COPPE, da Universidade Federal do Rio de Janeiro, como parte dos requisitos necessários à obtenção do título de Mestre em Engenharia Elétrica.

Orientador: Antonio Petraglia

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Jorge Vicente De la Cruz Marin

Outubro/2013

Orientador: Antonio Petraglia

Programa: Engenharia Elétrica

O projeto de um modulador sigma-delta, como parte de um conversor analógico-digital de um circuito integrado de medição de energia eléctrica é apresentado. Os principais requisitos deste tipo de aplicação são uma resolução de 16 bits e uma largura de banda de 40 Hz a 2 KHz. O projeto foi otimizado a nível de sistema para atingir o SNR máximo usando valores de capacitância mínimos. No circuito, o consumo de energia foi priorizado e blocos de baixo consumo foram utilizados como OTA com polarização adaptativo e comparador chaveado. O circuito foi desenvolvido na tecnologia CMOS 180 nm que utiliza 1.8 V como tensão de alimentação padrão. Simulações em cada *corner* da tecnologia confirmam que o modulador atinje as especificações, mesmo no pior caso. Além disso, simulações de Monte Carlo foram realizadas.

Abstract of Dissertation presented to COPPE/UFRJ as a partial fulfillment of the requirements for the degree of Master of Science (M.Sc.)

INTEGRATED CIRCUIT DESIGN OF SIGMA-DELTA MODULATOR FOR ELECTRIC ENERGY MEASUREMENT APPLICATIONS

Jorge Vicente De la Cruz Marin

October/2013

Advisor: Antonio Petraglia

Department: Electrical Engineering

The design of a sigma-delta modulator as part of an analog-to-digital converter for a monolithic electric energy measurement system is presented. The main requirements such applications are a resolution of 16 bits and a bandwidth ranging from 40 Hz to 2 KHz. The design was optimized at system level to attain maximum SNR using minimal capacitance values. At circuit level, the power consumption was prioritized and low power blocks, such as adaptive bias OTA and clocked comparator were used. The circuit was developed in a 180 nm CMOS process technology that employs 1.8 V as standard supply voltage. The simulations on each corner of the technology confirm that the modulator satisfies the specifications even in the worst case. Monte Carlo simulations were performed, as well.

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List of Acronyms

AAF	*Anti-aliasing filter*
ADC	*Analog-to-digital converter*
ASIC	*Application specific integrated circuits*
CMOS	*Complementary metal oxide semiconductor*
CT	*Continuous time*
DAC	*Digital-to-Analog converter*
DC	*Direct current*
DR	*Dynamic range*
DSP	*Digital signal processor*
DT	*Discrete time*
ENOB	*Effective number of bits*
FOM	*Figure of merit*
GBW	*Gain-bandwidth product*
IC	*Integrated circuit*
INL	*Integral non-linearity*
MASH	*Multi-stage noise-shaping*
NTF	*Noise transfer function*
OSR	*Oversampling Ratio*
OTA	*Operational transconductance amplifier*
PSD	*Power spectral density*

PVT	*Process, voltage and temperature*
RMS	*Root mean square*
SC	*Switched capacitor*
SFDR	*Spurious free dynamic range*
SINAD	*Signal to noise and distortion ratio*
$\Sigma\Delta$	*Sigma-Delta*
SNDR	*Signal to noise plus distortion ratio*
SNR	*Signal to noise Ratio*
SoC	*System on Chip*
STF	*Signal transfer function*
SQNR	*Signal to quantization noise ratio*
THD	*Total harmonic distortion*
UGF	*Unity gain frequency*
VLSI	*Very Large scale of Integration*
X_{OL}	*Overload level*

Chapter 1

Introduction

The present work aims at showing the entire design of a sigma-delta ($\Sigma\Delta$) modulator as part of an analog-to-digital converter (ADC) for an electric energy measurement integrated circuit(IC). The modulator was designed using $180nm$ CMOS (complementary metal oxide semiconductor) process technology with $1.8V$ of supply voltage featuring low power consumption. The $\Sigma\Delta$ ADC is divided into two main parts: $\Sigma\Delta$ modulator (analog domain) and the decimator (digital domain). Basically, the decimator consists of a digital filter and a downsampler that deliver a limited frequency signal with a specific number of bits and reduced sampling frequency (typically by the same ratio as the oversampling ratio). The $\Sigma\Delta$ modulator conveys the modulated input signal to the digital circuit with a high signal-to-noise ratio (SNR) that permits to attain the resolution required. There are numerous ways to implement a $\Sigma\Delta$ modulator and, depending on the application, each one possesses its respective advantages. Electric energy measurement applications require high accuracy (more than 16 bits) and a bandwidth that range from 40 Hz to 2 KHz. Hence, the main focus of this work is to design a $\Sigma\Delta$ modulator that accomplish the application requirements considering the issues at each stage of the top-bottom design flow (from the system level to physical design).

1.1 Motivation

The evolution of the CMOS technology during the last decades has allowed the presence of electronic systems in many aspects of our daily life: automotive, communications, consumer electronics, information technology, medicine, etc. Clearly, the most important evolution is the geometry dimension reduction of the devices and interconnections of the CMOS technology. The miniaturization has allowed the integration of millions of transistors -very large scale of integration (VLSI)- in a single chip as, for example, the last microprocessor of Intel whit its 1.4 billion of transistors in their Third Generation Intel® Core™ Processor. Furthermore, the

speed of the digital circuits has been upgraded as well, allowing its operation in the gigahertz range. In addition, the power supply voltage has been decreased (see Fig. 1.1) to maintain moderate electric fields inside the device thus avoiding large leakage currents. Consequently, the power consumption of the digital circuits has diminished, further enhancing their performances. The mentioned features have permitted to integrate complete electronic systems on a single chip, where the digital signal processor (DSP) is used to implement complex algorithms that process huge quantity of data in a few seconds. Hence, it is clear that there is a trend to exploit the digital capability by implementing all the system functionalities in the digital domain and letting only the interfacing tasks to the analog circuits (in most cases). This is commonly known as system-on-chip (SoC). It is worth noting that although the characteristics of modern technologies improve the operation of the digital circuits, significant drawbacks have introduced in the analog design such as the operation at low voltage, the short-channel effects and larger leakages currents.

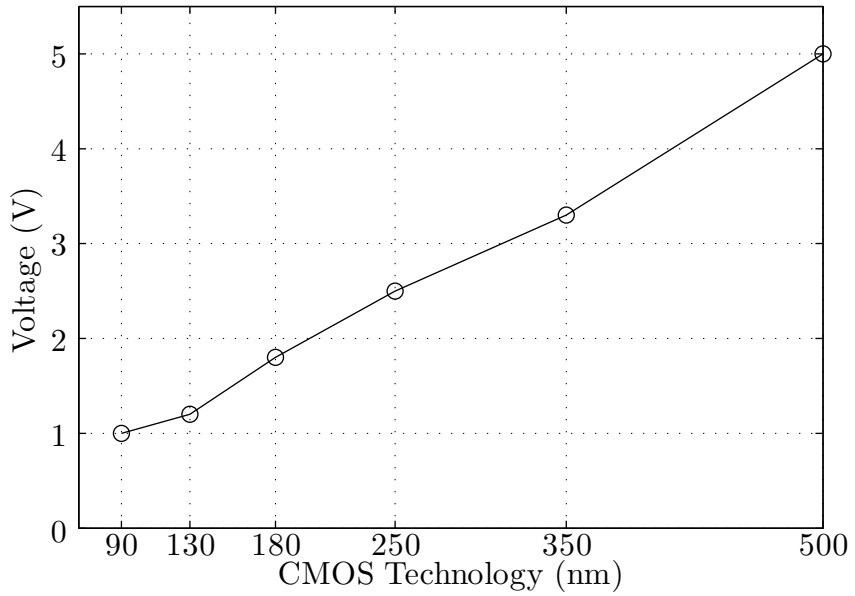


Figure 1.1: Standard supply voltage of various CMOS technologies.

The essential part of the interfacing circuits on a SoC is done by the ADC and the digital-to-analog converter (DAC), whereby these blocks are implemented in the same die that the DSP. It is important to notice that the converters are the bottleneck of the overall system so that the resolution, dynamic range and speed converter requirements have increased with modern technologies to maximize the DSP capacity. The issue here is that the analog circuits of the converters are implemented in a digital CMOS process in which the analog primitives are not fully optimized. As a result, they operate at low voltage supply with relatively high threshold voltage and in an environment full of noisy digital circuits. In conclusion, among the existing ADC topologies, the $\Sigma\Delta$ ADC is the more suitable solution for SoCs implemen-

tations since it is able to achieve high accuracy at a reasonable speed conversion, leverages the digital CMOS process features and is relatively insensitive to fabrication process variations. This balance is obtained using noise shaping technique and high sampling rate at the cost of the circuit complexity.

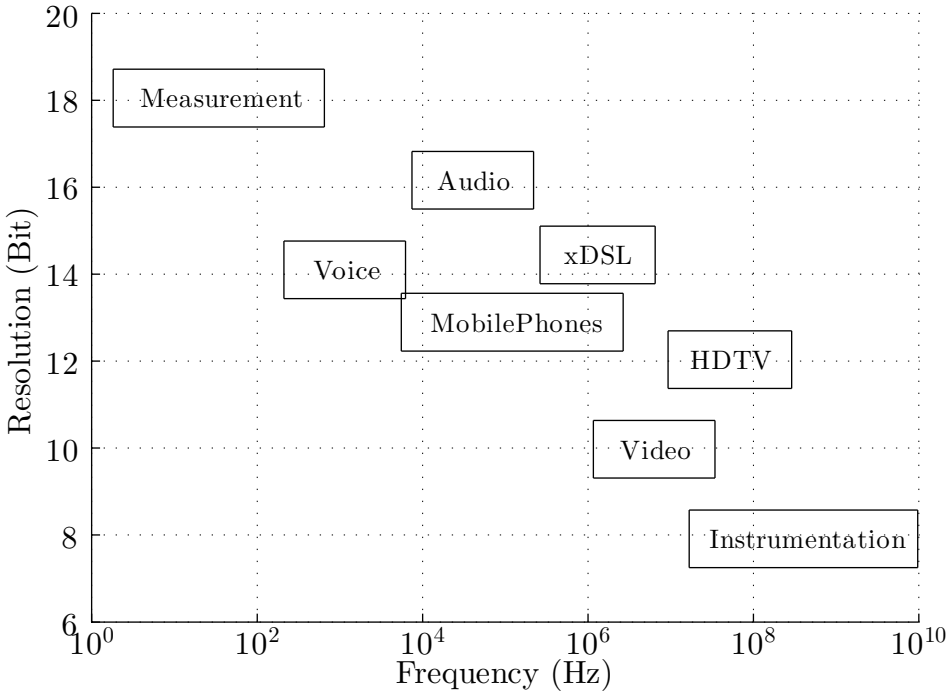


Figure 1.2: Bandwidth and resolution requirements of an ADC for different applications.

Figure 1.2 illustrates the frequency range and resolution requirements of the ADCs for different applications. It is important to note that despite the fact that the measurement systems operate at low frequencies, the ADC requires a large number of bits. This is the case of electric energy measurement ICs wherein the bandwidth of the input signal goes from 40 Hz to 2 KHz and demand minimum resolution of 16 bits. Those values are determined by the specifications of the standard IEC-61036, which requests more than 20 harmonics, wide dynamic range, measurement accuracy of 0.5% and detection of an input signal that varies from 4% to 400%. It is worth mentioning that the ADC receive a nearly constant amplitude signal since it is preceded by a programmable gain amplifier. An important quality parameter of the measurement IC is also based on its low power consumption, specially because it uses the power of the source being measured. Hence, the design of a $\Sigma\Delta$ modulator that reaches the application requirements featuring low power consumption and using an standard CMOS fabrication process is a trend. Moreover, since the main consumer of static power in the modulator is the operational transconductance amplifier (OTA) and it requires high bandwidth and high slew-rate, the design of this amplifier using the minimum power consumption represents a challenge.

1.2 Market Summary of Electric Energy Meters

The electric energy measurement IC is a growth market and there are products from simple application specific integrated circuits (ASICs) to SoC circuits. Table 1.1 lists some products that are available in the market and their corresponding ADC features. It is important to remark that some system requirements are set by the standard IEC-61036, in which the minimum accuracy is specified as 0.5% and is given by

$$Accuracy(\%) = \frac{Energy\ Registered - True\ Energy}{True\ Energy} \times 100\%. \tag{1.1}$$

Table 1.1: Review of the electric energy measurement IC market

Component	V_{DD} (V)	V_{REF} (V)	**Bits**	f_s(Hz)	BW(Hz)	**Type**	**Year**
AD51xx (66,59)	$2.4-3.7$	1.2	24	819.2K	$40-2$K	SoC	2008-2012
AD55xx (66,69)	$2.4-3.7$	1.2	24	819.2K	$40-2$K	SoC	2008-2012
AD71xx (16,56,66,69)	$2.4-3.7$	1.2	24	819.2K	$40-2$K	SoC	2007-2008
AD75xx (18,66,69)	$2.4-3.7$	1.2	24	819.2K	$40-2$K	SoC	2007-2008
AD7753	5	2.4	24	819.2K	$40-2$K	ASIC	2009
AD7756	5	2.5	20	819.2K	$40-2$K	ASIC	2001
AD7759	5	2.5	20	819.2K	$40-2$K	ASIC	2009
AD7763	5	2.5	24	819.2K	$40-2$K	ASIC	2004-2009
STPMxx (01,11)	2.5	1.2	16	1M	$40-2$K	ASIC	2011

The use of 20 harmonics, which means a bandwidth of 40Hz$-$2KHz, is enough to develop a solution for this kind of application. Furthermore, in order to accomplish the resolution requirements, 16 bits at the ADC output are sufficient.

1.3 The Need for Oversampling ADCs

The ADC architectures are classified in two main types in the literature: Nyquist-rate and oversampling converters. In the former, the bandwidth of the input signal comprises a half of the available bandwidth while in the second one only a small portion of the bandwidth is occupied. This difference is quantized by the oversampling ratio ($OSR = f_s/2f_{in}$) which is defined as the ratio between the sampling frequency (f_s) and the minimum sampling frequency ($2f_{in}$), also known as the Nyquist frequency . The Nyquist-rate ADCs have a small OSR (typically less than 8) and the oversampling ADCs have a OSR value ranging from 8 to 512. Figure 1.3 illustrates

the trade-off between accuracy and speed of various ADC architectures, of which the only oversampling converter is the $\Sigma\Delta$ architecture.

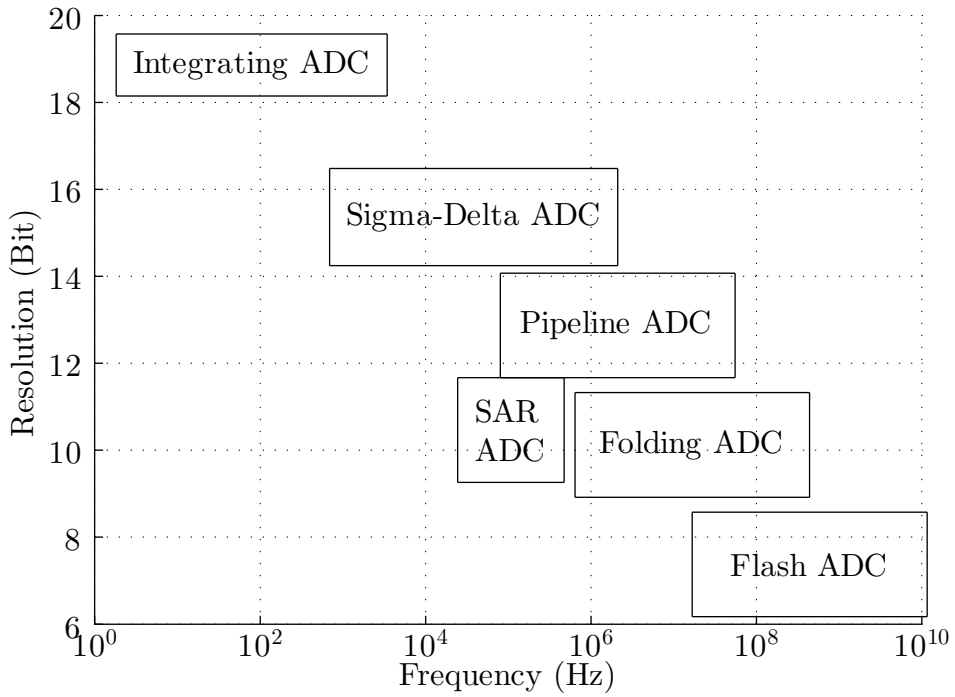


Figure 1.3: Typical bandwidth and resolution specifications of different ADC architectures.

The faster ADC is the full-flash converter (capable of operating at a conversion speed above 1GHz), but its drawback is that only achieve low resolutions (usually up to 8 bits) since its area is directly proportional 2^M(where M is the number of bits). Moreover, its resolution is even more critical when it is implemented using low-voltage technologies. The folding architecture does not achieve the speed conversion of the full-flash ADC, but allows a couple of more bits at high speed conversion. The pipelined ADC fits better for applications that require more than 10 bits and speed conversion from 1MHz to 100MHz. The successive approximation register (SAR) architecture is adequate for medium speed and medium resolution applications. When high resolution is required, the integrating ADC is a good alternative, but it requires at least 2^N (N is the number of bits) clock periods to convert a single sample. Hence, this architecture is the best option for applications that manage very low frequencies and need high resolution. In general, the Nyquist-rate converters cannot provide good accuracy with high speed conversion. In contrast, the $\Sigma\Delta$ ADC is able to achieve over 20 bits with reasonable conversion speed at the cost of circuit complexity and high sampling frequency. In conclusion, the requirements considered above indicate that the more appropriate ADC architecture for the implementation of an electric energy measurement IC is a $\Sigma\Delta$ structure.

1.4 Objectives and Methodology

The general objective of this work is the design of a ΣΔ modulator that is used in an ADC for electric energy measurement application. Basically, the modulator must achieve a high SNR that allows more than 16 bits at the ADC output for signals that range from 40Hz to 2KHz. An additional objective is reaching low power consumption by reducing the static power of the integrator's OTA.

Figure 1.4 illustrates the design flow of the ΣΔ modulator. It can be observed that each superior level defines the specifications of an inferior level and the verification must be done at each stage and from the bottom to the system level. It means that the extracted parameters of the lowest level must be used to simulate the critical system level parameters. In order to accomplish this design flow this work is developed in four stages, as described below.

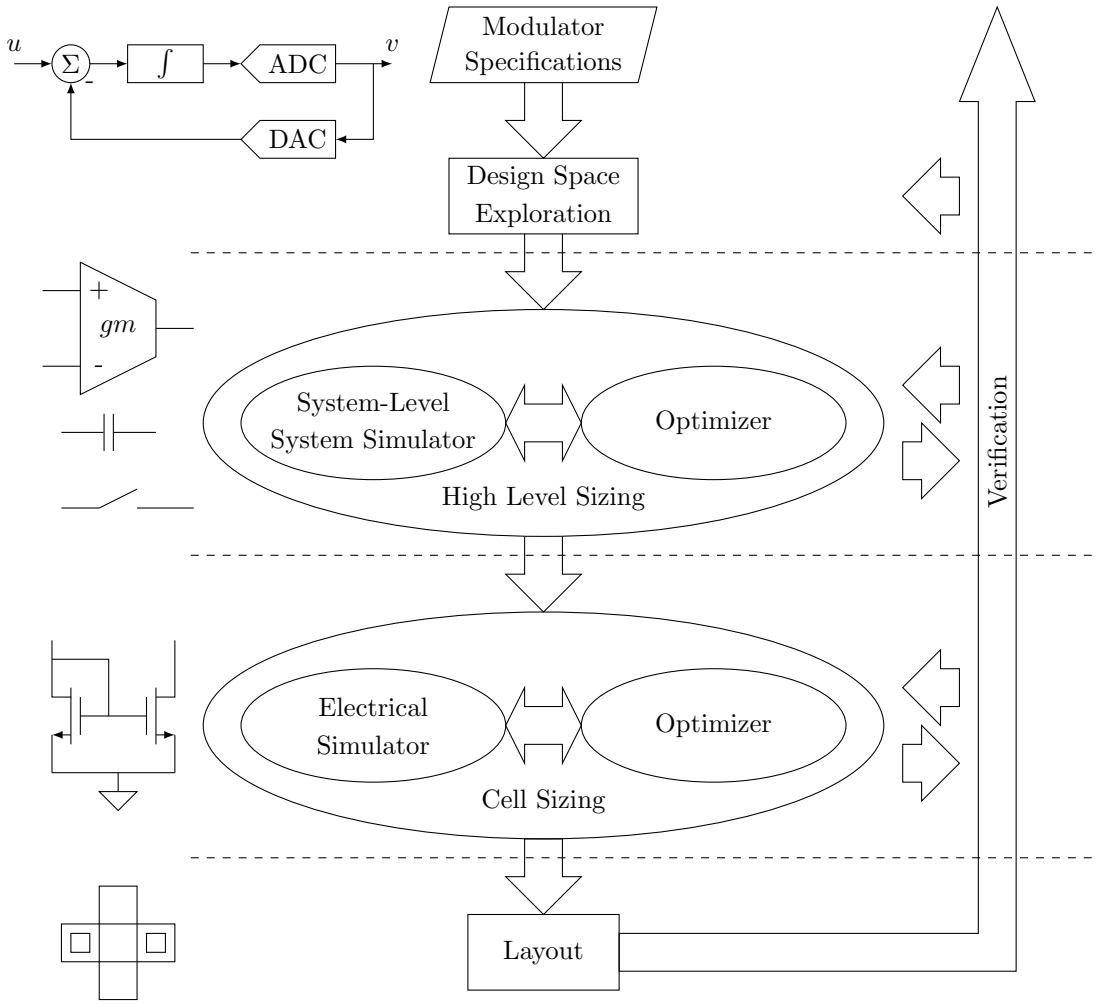


Figure 1.4: Top-down/Bottom-up design flow of the ΣΔ modulator.

1. **Study of the state of art of ΣΔ converters** and definition of the system specifications based on the application requirements. Also, a study of the commercial ICs for electric energy measurement is carried out.

2. **Analysis and design of the ΣΔ modulator architecture**. In this stage, the domain (continuous or discrete), integrator order, number of bits of the quantizer, loop topology and extra techniques (if necessary) are evaluated and set to attain the optimum performance for the application. Furthermore, the specifications of the analog blocks are defined such that the fabrication process variations do not affect the system performance. The architecture is validated using system level simulations with MATLAB and SIMULINK.

3. **Design (transistor and physical level) of the ΣΔ modulator circuit**. The design of each analog block is verified considering process, supply voltage and temperature variations (PVT simulations) by using electrical simulators Spectre and SpectreRF.

4. **Simulation results and conclusions** are presented. In this stage the results are discussed and recommendations for a future work are given.

1.5 Structure of the Dissertation

The next chapters are organized as follows. **Chapter 2** focuses on studying the existing architectures used to implement a ΣΔ modulator. It is also defined the appropriate architecture to accomplish the requirements. **Chapter 3** shows the architectural design of the ΣΔ modulator. Using a system level model, the architecture is validated using MATLAB and SIMULINK. The requirements of the analog blocks are determined based on the system level results. **Chapter 4** presents the design of the analog circuits and the listed the transistor dimensions of each block. **Chapter 5** depicts the relevant simulations and results that validate the functionality of the analog blocks and the modulator. Finally, **Chapter 6** presents the concluding remarks.

Chapter 2

Sigma-Delta Modulator

In the present chapter, the fundamentals and architectures of the $\Sigma\Delta$ modulator are studied. At first, the fundamentals of the ADC are reviewed including the basic structures of a Nyquist-rate ADC, oversampled ADC and noise-shaping ADC. Also, the useful performance metrics to characterize the modulator response are listed and defined. In order to introduce the basics of sigma-delta modulation, a brief historical reviewed and the plot of the output response of a first-order single-bit modulator are provided.

The next section describes the possible modulator architectures in: loop filter order, loop topology, domain and quantizer. The objective is to reduce the alternatives for implementing a sigma-delta modulator by organizing the design-space of the architecture in those categories. There is an emphasis on the single-loop single-bit architectures since the requirements settled in Chapter 1 specify only a resolution of 16 bits with a narrow band at low frequencies. Therefore, the study of high-order loop filters (above third-order) or cascade structures escapes from the focus of this dissertation. The fundamentals aspects of the following review are based on [2],[3],[4][5], [6] and [7].

Finally, the advantages and disadvantages of the architectures are contrasted to choose the most appropriate architecture for the application considered in this thesis. Also, some works that demand similar requirements are shown to compare the performance of the designed sigma-delta designed with the previously implemented modulators.

2.1 Fundamentals

The ADCs transform analog signals to digital domain using basically two blocks: a sampler and a quantizer. An anti-aliasing filter (AAF) is usually placed before the sampler since it removes the components outside the bandwidth and thereby avoids the fold-over of the signal replicas that appear after the sampling process. Despite

the fact that it is an essential block of the converters, its function is not considered as part of the conversion process. Figure 2.1 illustrates the conversion process in a Nyquist-rate converter and shows that the analog input signal $x_a(t)$ passes through the AAF, which limits the frequency components into a range between $-\frac{f_s}{2}$ to $\frac{f_s}{2}$. The signal is not affected and only the undesirable components are attenuated. After the signal conditioning, the AAF output $x_b(t)$ is sampled at a frequency f_s by the sampler obtaining a discrete-time signal $x_s(n) = x_b(nT_s)$, where $T_s = 1/f_s$ and n is an integer number from 0 to the total number of samples. The second stage of the conversion process is done by the quantizer. It maps the continuous values of the sample data onto a finite number of discrete levels (M bits are equivalent to $k = 2^M$ levels). This process introduces an error called quantization error (ϵ_Q) that is often referred as the quantization noise of the ADC. Its average power is considered as white noise and is given by the following expression:

$$v_{n,q}^2 = \frac{\Delta^2}{12}, \tag{2.1}$$

where

$$\Delta = \frac{V_{FS}}{k}, \tag{2.2}$$

and V_{FS} is the full-scale of the quantizer.

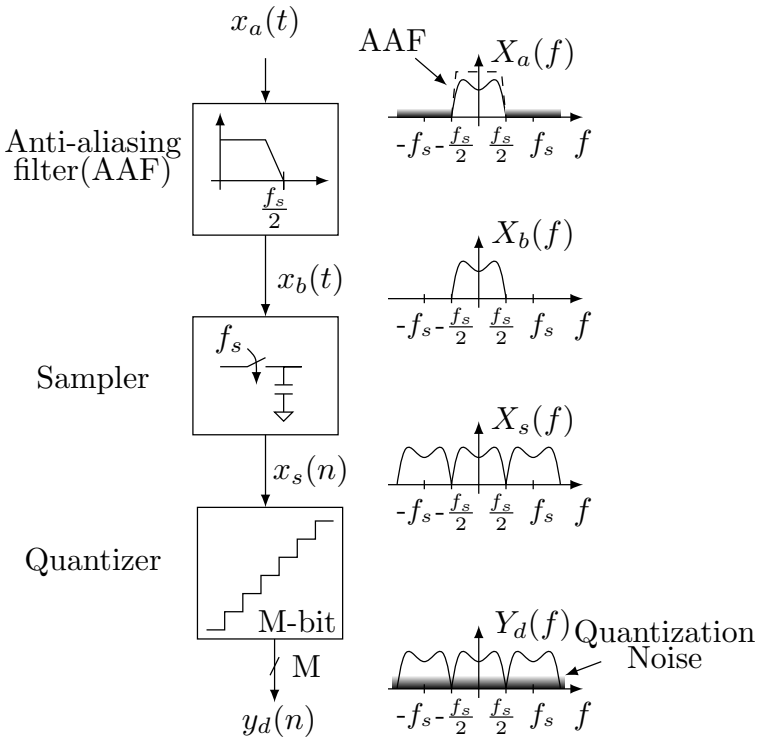


Figure 2.1: Block diagram of a Nyquist-rate ADC.

2.1.1 Performance Metrics

There are many metrics that characterize an ADC as shown in [2],[7], [8]. Some of them are also valid to measure the performance of a $\Sigma\Delta$ modulator, specially the ones that analyze the output spectrum. The most useful metrics to characterize a $\Sigma\Delta$ modulator are presented below. The first two are spectral metrics which are based on the analysis of the output spectrum directly. They are illustrated in Fig. 2.2. The remain metrics are obtained by analyzing many output spectra for a determined input power (an example is shown in Fig. 2.3). Usually the input signal used to measure the modulator is a sine wave.

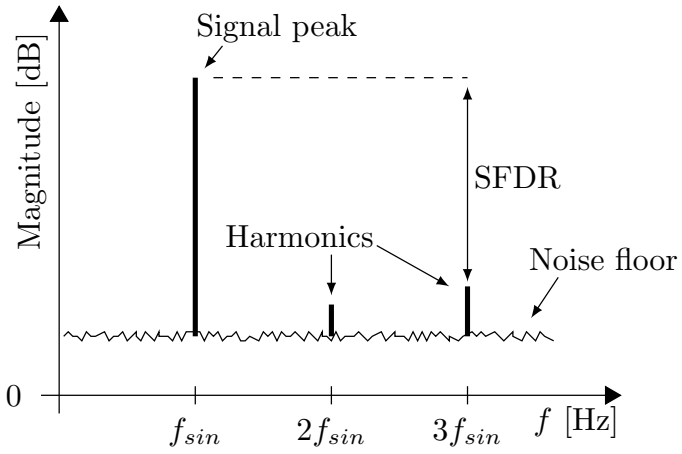


Figure 2.2: Typical spectrum of a modulator output.

2.1.1.1 Total harmonic distortion (THD)

It is given by the ratio between the sum of the powers of the harmonic components inside the signal bandwith and the power of the fundamental component.

2.1.1.2 Spurious free dynamic range (SFDR)

It is defined as the ratio between the signal power and the strongest harmonic component power.

2.1.1.3 Signal-to-noise ratio (SNR)

It is the ratio between the signal power and the noise power. In the case when the noise is only quantization noise, it is called signal-to-quantization-noise ratio (SQNR).

2.1.1.4 Signal-to-(noise+distortion) ratio (SNDR)

This parameter is also known as SINAD, and is defined as the ratio between the signal power and the sum of powers of the harmonics components inside the signal bandwidth plus the noise power.

2.1.1.5 Dynamic range (DR)

It is the power of the input signal at which the SNR (or the SINAD) is 0 dB. It can be interpreted as the power of the sinusoidal input that stimulate an output signal at the input frequency with power equal to the noise power.

2.1.1.6 Effective number of bits (ENOB)

This metric is the equivalent in number of bits of the SNR or SNDR. It is given by:

$$ENOB = \frac{SNR - 1.76}{6.02}, \tag{2.3}$$

2.1.1.7 Overload level (X_{OL})

It is the maximum amplitude of the input signal for which the system still operates correctly.

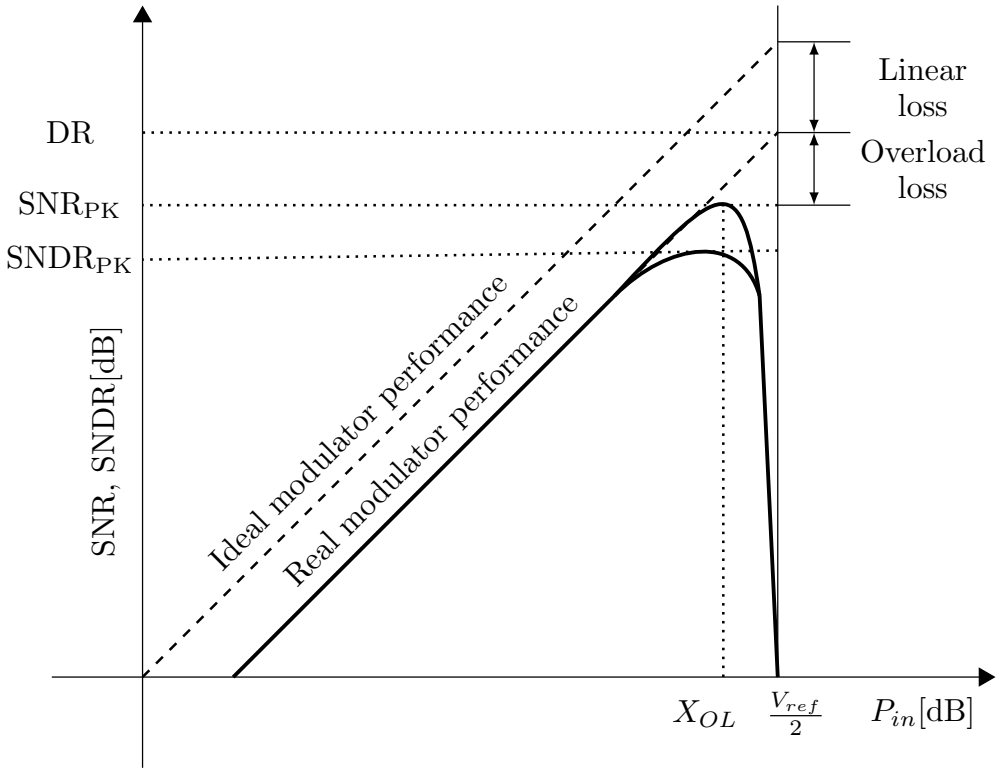


Figure 2.3: Example of plot of SNR vs. Input power.

2.1.2 Oversampling

From the Nyquist theorem, it is known that the minimum frequency (called Nyquist frequency f_N) to sample a signal with bandwidth f_b is $2f_b$. Hence, the oversampling ratio (OSR) quantifies by how much the sampling frequency (f_s) is greater than the Nyquist frequency:

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_b}. \tag{2.4}$$

As mentioned in Chapter 1, when an ADC operates with an OSR greater than one, it is called an oversampling ADC (see Fig. 2.4). This architecture adds a decimator to the process conversion to filter the oversampling data and reduces the sampling frequency by the same value as the OSR.

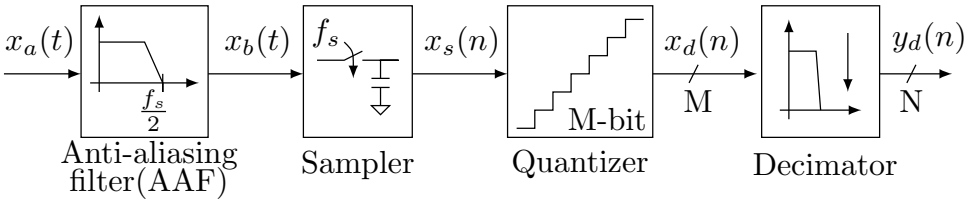
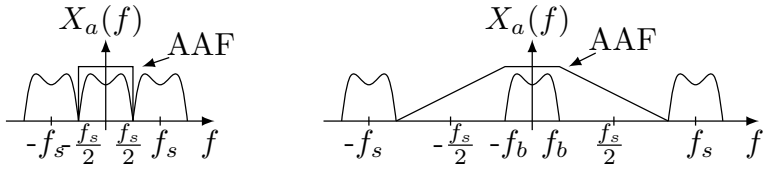
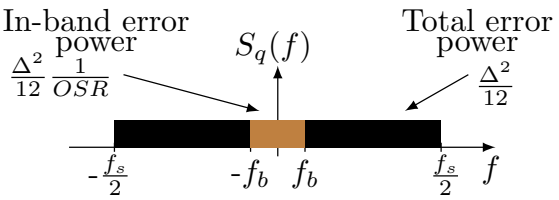


Figure 2.4: Block diagram of an oversampling ADC.

An advantage about using oversampling ADCs is that the specifications of the AAF are relaxed because the signal bandwidth is smaller than $f_s/2$ and hence the images of the signal are more separated than in a Nyquist-rate converter (see Fig. 2.5(a)). Furthermore, the quantization noise power is reduced since only a fraction of the total noise affects the signal (see Fig. 2.5(b)).



(a) Anti-aliasing Filter

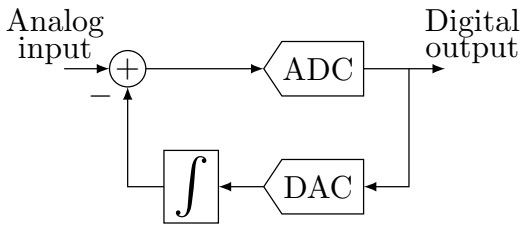


(b) Quantization Noise Power

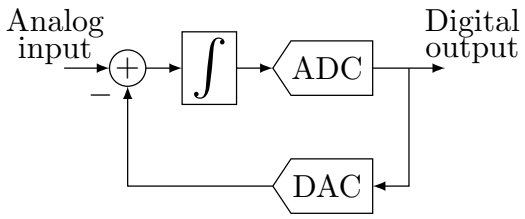
Figure 2.5: Advantages of the oversampling ADC.

2.1.3 ΣΔ Modulation

The oversampling idea was initially conceived to improve the transmission of the pulse code modulation (PCM). It consists on transmitting the sample changes at high sampling rate instead the actual samples. The idea was based on the operation of the human brain, whereby the physiological signals are transmitted to the brain by a series of electrical pulses in the nerve system. Figure 2.6(a) shows a block diagram where if the ADC is a 1-bit quantizer, the structure is called delta modulator and if it is a multi-bit quantizer, it is called as differential PCM. The basic operation consists of comparing the input signal with an estimate of the output data and quantizing this error. The feedback signal is obtained by integrating the DAC output which is the analog estimation of the digital output. This structure is advantageous for oversampling signals since the amplitude of the difference signal is much smaller than that of the input signal.



(a) Delta Modulator



(b) Sigma-Delta Modulator

Figure 2.6: Delta and Sigma-Delta Modulators.

The first patent of delta modulation was done by ITT laboratories in France in 1946 [9][10]. Later, in 1952, the concept was published by Jager as a method of PCM transmission[11]. In 1960, Cutler from Bell Laboratories patented an early description of using feedback to improved the resolution of a converter [12]. This was the first publication about the application of this technique in converters but the integrator still remained in the feedback path. It was not until 1962 that H. Inose et al. [13] proposed to move the integrator from the feedback loop to the forward loop (see Fig. 2.6(b)). The relocation of the integrator changes the transfer function from high-pass to low-pass, thereby obtaining an unchanged replica of the

analog input at the output. Furthermore, the quantization noise of the ADC is attenuated as much as the integrator gain (known as **noise shaping**). The name of $\Sigma\Delta$ comes from the operation of the modulator, that is the integration (sigma) of the difference (delta).

2.1.4 Oversampling Noise-Shaping ADC

The techniques of oversampling and noise-shaping (by employing a $\Sigma\Delta$ modulator) lead to attain high resolution converters using a low resolution quantizer. This is achieved by reducing as much as possible the quantization noise located in the signal bandwidth and by using a decimator. The scheme of the oversampling noise-shaping converter (also know as $\Sigma\Delta$ converter) is depicted in Fig. 2.7.

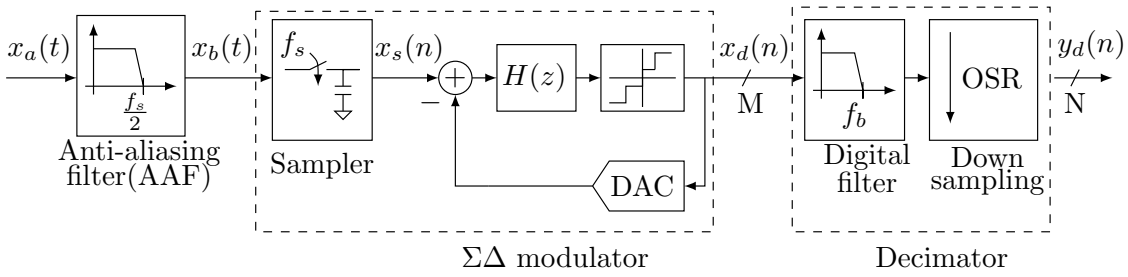


Figure 2.7: Block diagram of a $\Sigma\Delta$ ADC.

2.1.5 First Order $\Sigma\Delta$ Modulator

Since the $\Sigma\Delta$ modulator is the key of the converter operation, a basic modulator is analyzed to understand its operation. Assuming that the loop filter is a discrete-time(DT) forward-Euler integrator,

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}, \tag{2.5}$$

the linear model of a first order $\Sigma\Delta$ modulator can be represented by the block diagram shown in Fig. 2.8 whose output is:

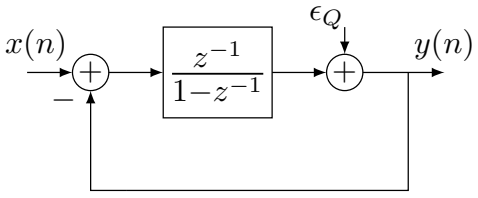


Figure 2.8: Linear model of Fig. 2.6(b).

$$Y(z) = (X(z) - Y(z))\frac{z^{-1}}{1 - z^{-1}} + \epsilon_Q \tag{2.6}$$

which leads to

$$Y(z) = X(z)z^{-1} + \epsilon_Q \left(1 - z^{-1}\right) = STF(z)X(z) + NTF(z)\epsilon_Q, \tag{2.7}$$

where STF and NTF are the signal transfer function and noise transfer function, respectively. From these expressions it is clear that the input is replicated at the output only delayed by one clock period and the quantization noise is shaped by a high-pass filter. A metric to quantify how much the quantization noise interferes in the signal bandwidth is the SQNR. Thus, in order to obtain the total noise power inside the signal band, the product of the quantization noise PSD and the square of the absolute value of the NTF is integrated from 0 to f_b as

$$V_{n,Q}^2 = S_{n,Q} \int_0^{f_b} |NTF|^2 \, df, \tag{2.8}$$

where the quantization noise PSD is given by

$$S_{n,Q} = \frac{v_{n,Q}^2}{f_s/2}. \tag{2.9}$$

Using the definition $z = e^{j\omega T}$, we can express the noise transfer function can be expressed in the frequency domain as

$$NTF = 2je^{\omega T/2} sin(\omega T/2) \tag{2.10}$$

Solving the integral and using the approximation $sin(x) \approx x$ (valid for $\omega_b T/2 \ll \pi/2$), are find the noise power inside the signal band:

$$V_{n,Q}^2 = S_{n,Q} \int_0^{f_b} 4sin^2(\pi f T) df \approx S_{n,Q} \frac{4\pi^2}{3} f_b^3 T^2 \tag{2.11}$$

Replacing Eqs. (2.1) and (2.9) in (2.11), the $V_{n,Q}^2$ is rewritten as:

$$V_{n,Q}^2 = v_{n,Q}^2 \frac{\pi^3}{3} \left(\frac{f_b}{f_s/2}\right)^3 = v_{n,Q}^2 \frac{\pi^2}{3} OSR^{-3} \tag{2.12}$$

In addition, assuming that the ADC has the same number of bits as the DAC, which is M, and recalling that the quantization interval is expressed by Eq. (2.2), the quantization power noise is written as:

$$v_{n,Q}^2 = \frac{V_{FS}^2}{k^2 12} \tag{2.13}$$

which leads to:

$$V_{n,Q}^2 = \frac{V_{FS}^2 \pi^2}{36k^2} OSR^{-3}. \tag{2.14}$$

Therefore, considering a single-tone with amplitude $A_{sin} = V_{FS}/2$ as input signal, the SQNR is expressed as:

$$SQNR_{\Sigma\Delta,1} = \frac{12}{8}k^2\frac{3}{\pi^2}OSR^3 \tag{2.15}$$

which in dB becomes:

$$SQNR_{\Sigma\Delta,1}|_{dB} = 6.02M + 1.78 - 5.17 + 9.03log_2(OSR). \tag{2.16}$$

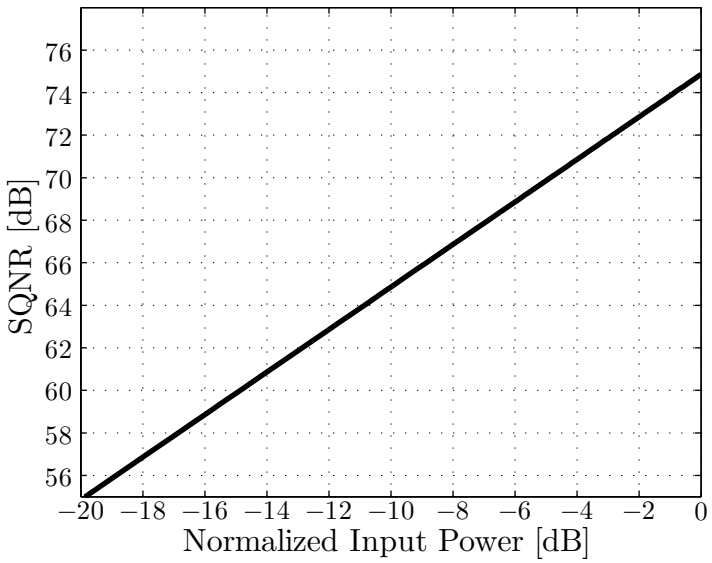


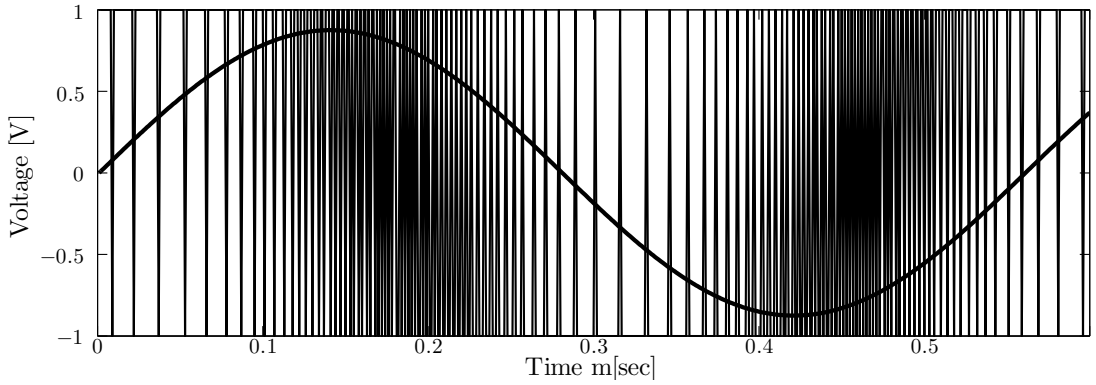
Figure 2.9: Ideal SQNR as a function of the normalized input power.

It can be noticed that for every doubling the OSR, the ENOB of the modulator output improves 1.2-bit, and adding one bit to the quantizer for a fixed OSR, the ENOB increases by 1 bit. Also, the SQNR depends on the input signal power (see Fig 2.9). As the input power increases, the SQNR increases, as well, since the quantization noise power is constant. This relationship is expressed as:

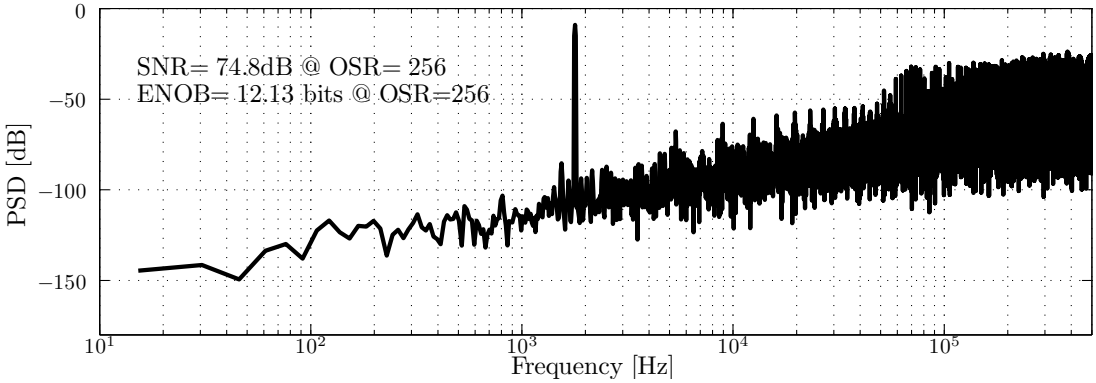
$$SQNR_{\Sigma\Delta,1} = \frac{A_{sin}^2}{V_{FS^2}}\frac{12}{2}k^2\frac{3}{\pi^2}OSR^3. \tag{2.17}$$

In order to show the basic operation of a single-bit first-order $\Sigma\Delta$ modulator, a simulation was performed using $f_s = 1MHz$, a $OSR = 256$, $N = 65536$ samples, an ADC output voltage(V_{ADC}) of $1V$, a DAC reference voltage(V_{REF}) of $1V$ and an input sine signal with amplitude of $0.9V_{REF}$. Figure 2.10(a) depicts the time response of the modulator, where the codification of the output signal can be observed. The output pulses are negative when the input signal is positive and, as the input increases, the time between each pulse decreases. Similar behavior occurs when the input signal is negative, but in this case the pulses are positive. The PSD of the output signal is illustrated in Fig. 2.10(b) and it can be observed that the

modulator reaches an ENOB of 12-bit using only 1-bit quantizer.



(a)



(b)

Figure 2.10: (a) Input and output signal of a first-order ΣΔ modulator; (b)PSD of the output signal.

2.2 Architectures

Since publication of the paper of H. Inose [13] many changes in the architecture of the ΣΔ modulator were proposed to improve its performance. These architecture changes can be classified in four categories: domain, integrator order, loop topology and the number of bits of the quantizer. An illustration of the large variety of proposed architectures is shown in Fig. 2.11.

2.2.1 Integrator Order

The expression of the SQNR for a first-order ΣΔ modulator(see Eq. 2.16) indicates that the ENOB only increases by 1.2-bit for every doubling of the OSR. This implies that when higher resolutions are required, a large OSR value must be used. A drawback of this scenario is that as the OSR increases, the correlation between the input signal and the quantization error becomes stronger, causing a coloration of the

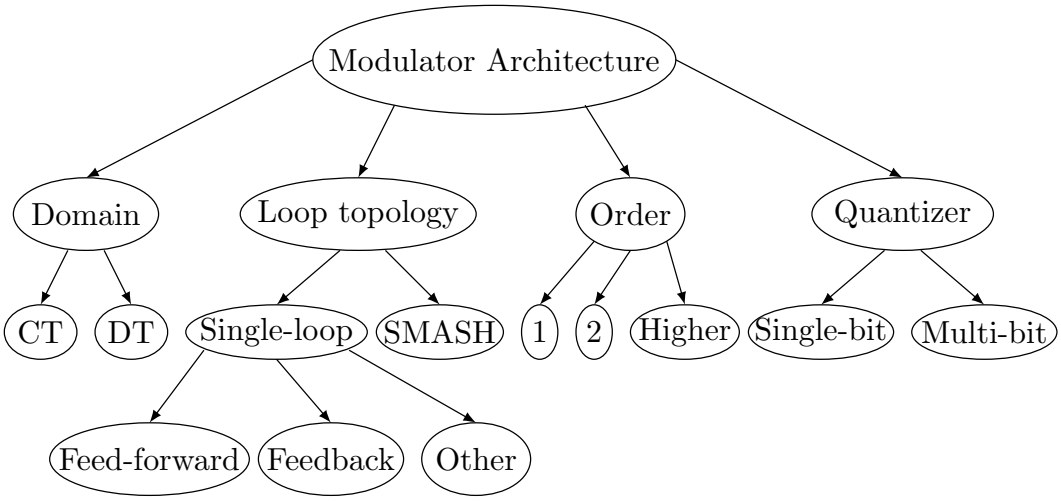


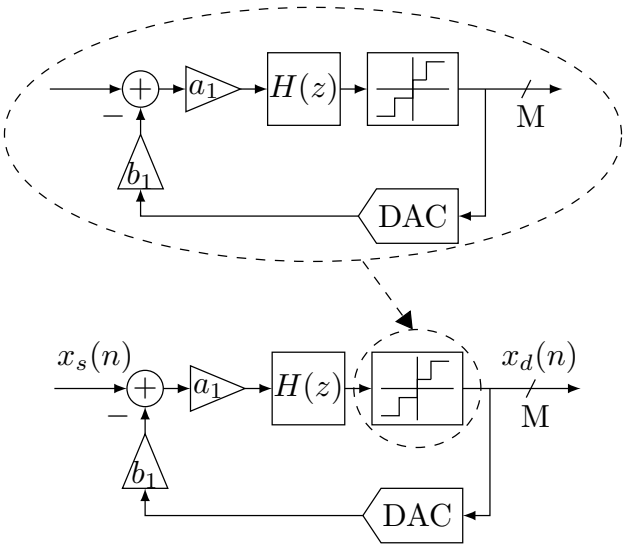
Figure 2.11: Design-space of a modulator architecture.

white noise and the presence of idle tones(called as pattern noise) inside the signal band[14]. As a consequence, the linear model is no longer accurate and the SQNR does not rise as in Eq. 2.16.

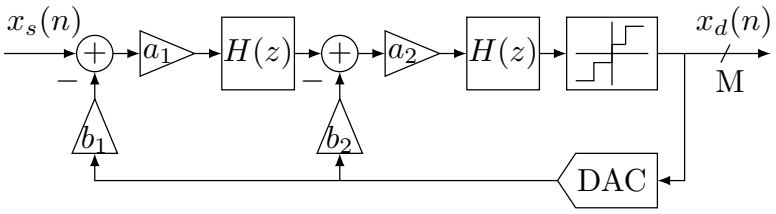
Therefore, an alternative to improve the SQNR is to replace the quantizer of a first-order single-loop $\Sigma\Delta$ modulator by another modulator, as illustrated in Fig. 2.12(a). The resulting structure is a second-order $\Sigma\Delta$ modulator (see Fig. 2.12(b)). In a first inspection it can be observed that the quantization error is filtered twice, and consequently it is expected that the attenuation is greater than when using only one integrator. By continuing the substitution of quantizers by modulators until we have L integrators in the forward path, the resulting topology becomes an L^{th}-order $\Sigma\Delta$ modulator, as shown in Fig. 2.12(c). The NTF of this topology is given by:

$$NTF = \frac{(1 - z^{-1})^L}{D(z)}, \tag{2.18}$$

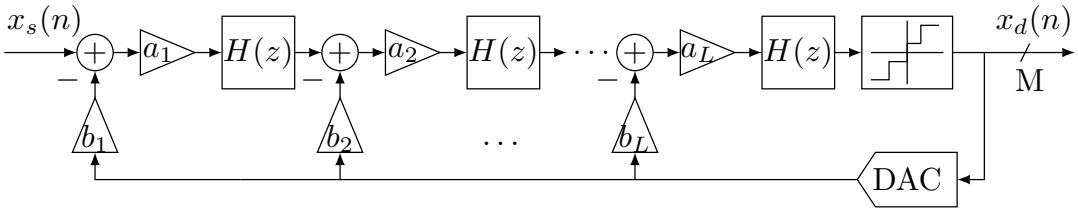
where $D(z)$ is the denominator of both the NTF and STF, which results from the multiple feedback paths in the structure. This polynomial introduces poles and zeros to the system, and their locations depend on the integrator and feedback coefficients(a_i and b_i, respectively). One of the functions of the coefficients is to guarantee the stability of the modulator (additional details about the coefficients are given in the topology subsection). Therefore, although not common, the following analysis considers $D(z) = 1$ since this assumption is valid for the purpose of illustrating the effect of the filter order in the topology and assure stability. Extending the analysis of the first-order $\Sigma\Delta$ modulator, the total quantization noise power inside the signal band of a L^{th}-order $\Sigma\Delta$ modulator is determined by[2]:



(a)



(b)



(c)

Figure 2.12: (a) First-order, (b) second-order and (c) L^{th}-order $\Sigma\Delta$ Modulators.

$$V_{n,Q}^2 = v_{n,Q}^2 \frac{\pi^{2L}}{2L+1} \left(\frac{f_b}{f_s/2} \right)^{2L+1} = v_{n,Q}^2 \frac{\pi^{2L}}{2L+1} \cdot OSR^{-(2L+1)} \tag{2.19}$$

which leads to

$$V_{n,Q}^2 = \frac{V_{ref}^2}{12k^2} \left(\frac{\pi^{2L}}{2L+1} \right) \cdot OSR^{-(2L+1)}. \tag{2.20}$$

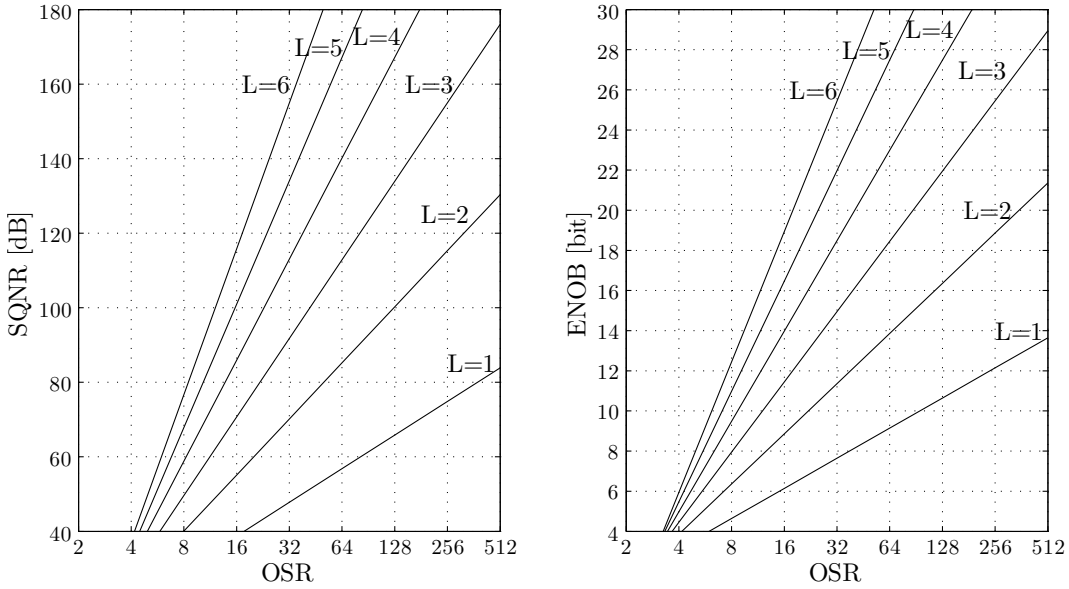
Thus, the SQNR is

$$SQNR_{\Sigma\Delta,L} = \frac{12}{8} k^2 \left(\frac{2L+1}{\pi^{2L}} \right) OSR^{2L+1} \tag{2.21}$$

or, expressed in dB,

$$SQNR_{\Sigma\Delta,1}|_{dB} = (1.78 + 6.02M) - 10log\left(\frac{\pi^{2L}}{2L+1}\right) + 3.01\,(2L+1)\cdot log_2\,(OSR)\,. \tag{2.22}$$

From the above expression, it can be observed that there is a fixed penalty for using a determined filter order in the modulator. It is represented by the loss of $10log\left(\frac{\pi^{2L}}{2L+1}\right)$ in SQNR. Moreover, the SQNR increases at a higher rate when a high filter order is used. For instance, for every doubling the OSR value, the SQNR rises 15.05dB, 21.07dB, 27.9dB and 33.11dB for a loop filter of second, third, fourth and fifth orders, respectively. Figure 2.13(a) shows the plots of the SQNR and ENOB in terms of the OSR for a single-loop $\Sigma\Delta$ modulator with different filter orders using a 1-bit quantizer. It can be observed that for resolutions greater than 20 bits, it is necessary to use a filter order greater than 2. When high resolution is required, a fourth or third order loop filter is sufficient to reach the specifications; but when the signal band is wide, the use of high OSR values is prohibited since it requires high-frequency amplifiers, which consumes too much power. Therefore, the commonly solution applied is the use of higher order filters and low OSR.



(a) (b)

Figure 2.13: Ideal SQNR and ENOB vs. OSR for different filter orders.

The main disadvantage of using high order filters is the instability of the system. The first and second order single-loop $\Sigma\Delta$ modulators are easy to stabilize but as the order increases, the guarantee of stability becomes less evident. Even when the stability is assured by using criteria of linear feedback networks, the system may be

unstable since there is a quantizer in the loop. This block turns the system into a non-linear one specially when it has low resolution[2].

2.2.2 Topologies

There are two common alternatives to implement a $\Sigma\Delta$ modulator: a single-loop or a cascade architecture. The former refers to the use of only one quantizer (it is also called single-stage or single-quantizer). The latter, also called MASH (multi-stage noise-shaping) $\Sigma\Delta$ modulators, is an alternative to implement high order modulators without stability problems. The principle of operation is depicted in Fig. 2.14(a). It can be observed that the structure consists of low-order single-loop modulators in series to form a high-order modulator[6]. Each modulator modulates the quantization error generated in the previous stage and the outputs are processed by a DSP using a digital cancellation logic (a typical implementation is shown in 2.14(b)) and thereby only remains the last quantization error shaped by all the modulators. There are many advantages and disadvantages of this architecture but are not detailed in the present document since escape from the main focus of the dissertation.

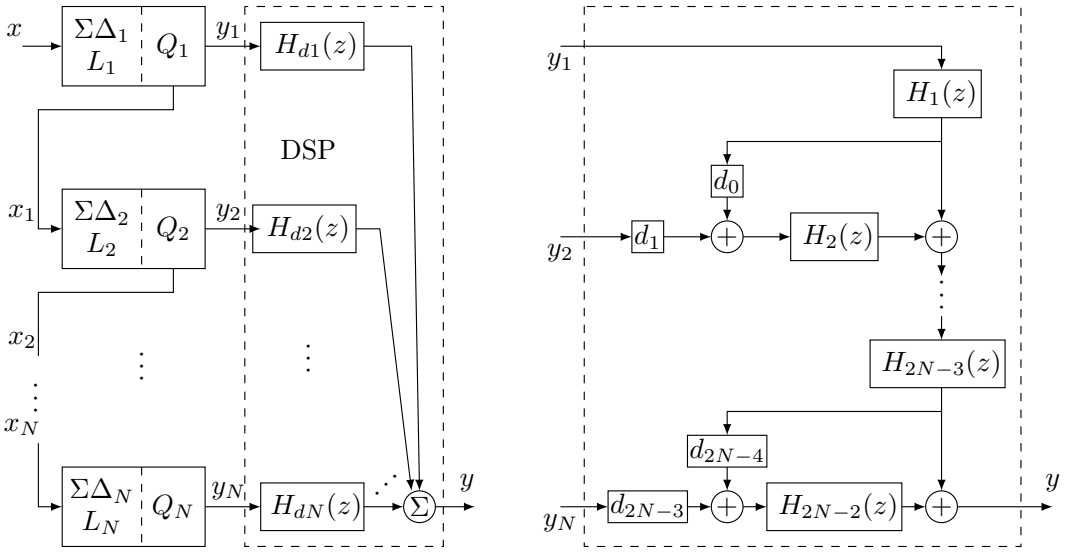


Figure 2.14: (a) Generic MASH architecture and (b) Typical implementation of the cancellation of quantization error in the DSP.

The single-loop topology is commonly used to implement first-order, second-order or even third-order $\Sigma\Delta$ modulators. Higher orders were also implemented in the literature but at the cost of complexity to assure the stability of the system. The common single-loop architectures can be classified as feedback, feedforward and

hybrid topologies. Also, the inclusion of local feedback loops is often employed to enhance the modulator performance.

2.2.2.1 Distributed feedback

This is the most common single-loop topology and is usually called as single-loop. Figure 2.12(c) illustrates the distributed feedback topology for any filter order. The coefficients in the forward path are called integrator scalings or weights and are used to limit the output dynamic range of the integrator. For instance, if the voltage swing at the integrator output ranges from -2 to 2, it can be reduced to -1 to 1 using 0.5 as integrator coefficient. The main feedback ensures that the quantized output tracks the input. The other feedback coefficients are used to adjust the transfer function. It is important to note that the coefficient values must accomplish the stability conditions of the system. The STF and NTF of a L^{th}-order distributed feedback topology are given by

$$STF = \frac{H^N(z)\Pi_{i=1}^N a_i}{1 + \Sigma_{i=1}^N b_i H^{N+1-i}(z)\Pi_{k=i}^N a_k} \tag{2.23}$$

and

$$NTF = \frac{1}{1 + \Sigma_{i=1}^N b_i H^{N+1-i}(z)\Pi_{k=i}^N a_k} \tag{2.24}$$

The major disadvantage of this topology is that the first integrator output contains an amount of the input amplitude. Hence, it requires significant swing capabilities to avoid saturation. Furthermore, when the output swing requirement exceeds the allowable voltage for a given technology (commonly in the newer technologies), the use of small coefficients is the only solution. One consequences is that bigger area is required to maintain the same capacitor noise and thereby more power is needed to charge this capacitor. Even if small coefficient values are chosen, the modulator doesn't operate correctly for input signals with amplitudes whose values are near that the reference voltage.

2.2.2.2 Feed-forward

The so called **feed-forward summation** topology is illustrated in Fig. 2.15. In this case, there is a main feedback and the coefficients are in the feed-forward paths. Each integrator output has a weight, and these outputs are added at the quantizer input. The STF and NTF of the topology are given by:

$$STF = \frac{\Sigma_{i=1}^N c_i H^i(z)}{1 + b_1 \Sigma_{i=1}^N c_i H^i(z)} \tag{2.25}$$

$$NTF = \frac{1}{1 + b_1 \Sigma_{i=1}^{N} c_i H^i(z)} \tag{2.26}$$

For a desirable NTF, the STF is defined, which could cause problems when an optimized NTF is not an appropriate STF[4]. The major advantage of this topology is that the first integrator output does not contain significant part of the input signal. Nonetheless, it still carries an amount of the input amplitude. Thus only this one must have a considerable output swing. It is worth mentioning that the SNR peak of this topology is greater than the distributed feedback but it still saturates for input amplitudes near V_{REF}.

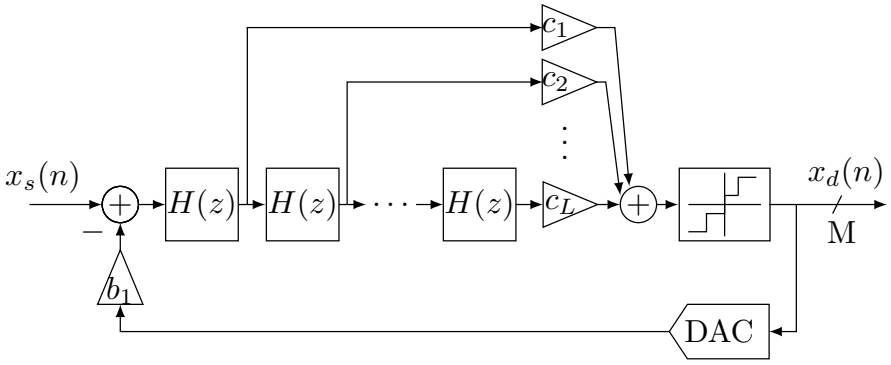


Figure 2.15: L^{th}-order feed-forward summation topology.

In a discrete-time implementation, the integrator has an inherent weight that is equal to 1 when its capacitors are equal but could assume other values if distinct capacitors are used. Therefore, the above topology assumes its generic form by adding coefficients to the integrators and implementing a direct injection of the input signal to the quantizier[15]. The resulting topology is illustrated in Fig. 2.16 and is called **full-feedforward**[5]. It keeps the same NTF as those of feed-forward or feedback topologies but relaxes the integrator requirements since only quantization error is processed by the integrators. In this case,

$$STF = \frac{c_0 + \Sigma_{i=1}^{N} c_i H^i(z) \Pi_{k=1}^{i} a_k}{1 + b_1 \Sigma_{i=1}^{N} c_i H^i(z) \Pi_{k=1}^{i} a_k} \tag{2.27}$$

$$NTF = \frac{1}{1 + b_1 \Sigma_{i=1}^{N} c_i H^i(z) \Pi_{k=1}^{i} a_k}. \tag{2.28}$$

The coefficient b_1 only represents the gain of the STF and NTF and does not have influence on the SQNR. However it does affect the location of the poles and zeros of the system. The influence of the coefficient c_0 is only noted when the quantizer employs more than one bit (this is detailed in the next chapter). Therefore, with $c_0 = 1$ and $b_1 = 1$, the STF and NTF are given by:

$$STF = 1 \tag{2.29}$$

$$NTF = \frac{1}{1 + \Sigma_{i=1}^{N} c_i H^i(z) \Pi_{k=1}^{i} a_k}. \tag{2.30}$$

It is important to note that for any value of b_1, the STF and NTF at low frequencies still maintain the above expressions. Therefore, it can be seen that this topology allows the optimization of NTF without modifying the STF.

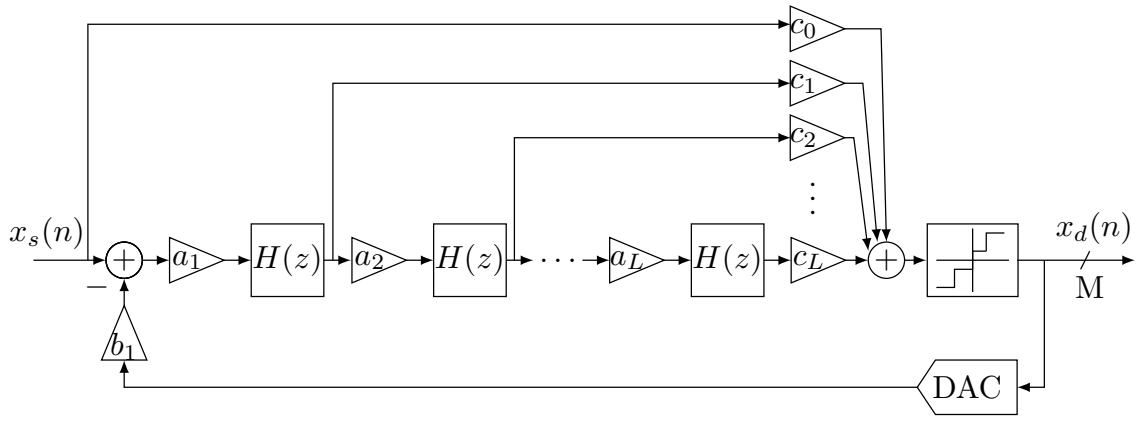


Figure 2.16: L^{th}-order fully feed-forward topology.

The main advantage is that the integrators only process the quantization noise, thereby relaxing the requirement of output swing. Also, the SNR peak is greater than the presented above and it could be obtained with an amplitude of 90% of the V_{REF}.

2.2.2.3 Hybrids

Figure 2.17 illustrates the combination of weighted feedback and distributed feed-forward in a modulator. The major advantages of using feed-forward is not exploited in this topology since the distributed feed-forward injects the input signal at each integrator input. Moreover, alike the classic distributed feedback topology, the STF and NTF are somewhat independent and thereby can be optimized separately.

The cost of using feedback coefficients is greater than that ofusing feed-forward coefficients. The feedback coefficients are usually implemented with active circuits that consume static power and, in contrast, the feedforward coefficients are usually implemented with pasive circuits when a 1-bit quantizer is employed.

2.2.2.4 Local Feedback Loops

A common characteristic among the above topologies is that the zeros of the NTF are located at DC. As a consequence, the quantization noise is attenuated at low

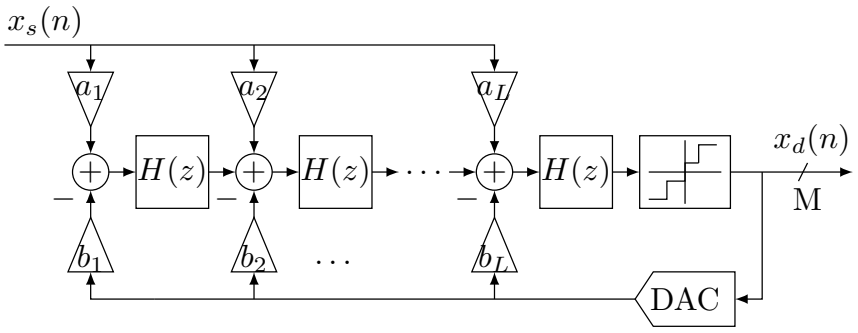


Figure 2.17: L^{th}-order hybrid topology.

frequencies but quickly increases next the bandwidth. By adding local feedback loops between two integrators (see Fig. 2.18) in the forward path of the modulator, the zeros are spread over the bandwidth to optimize the frequency response. This type of topology is usually employed in high-order modulators and wide-band applications.

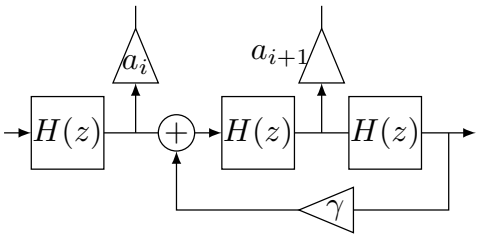


Figure 2.18: Local feedback loop.

2.2.3 Domain

In Fig. 2.7, it is depicted a discrete-time ΣΔ Modulator (DT-ΣΔM) where the loop filter $H(z)$ is an analog discrete-time filter. An alternative implementation can be achieve using a continuous-time filter ($H(s)$), as is shown in Fig.2.19. Here, the input signal can be applied directly to the modulator without preceding an AAF since the continuous-time ΣΔ modulator (CT-ΣΔM) has an implicit AAF in the structure[14]. The sampling operation is carried out before the quantizer, which represents the major advantage of the structure since all the errors generated by the non-idealities of the sampling process are attenuated by the NTF.

Another important difference between both implementations is that in a DT-ΣΔM, the loop filter is realized using switched-capacitor(SC) circuits (see Fig. 2.20(a)) while in a CT-ΣΔM, it can be implemented using a (passive or active) RC-filter, an OTA-C filter or an LC resonator(an example is shown in Fig. 2.20(b)). In the former, the frequency response of the amplifier limits the maximum clock

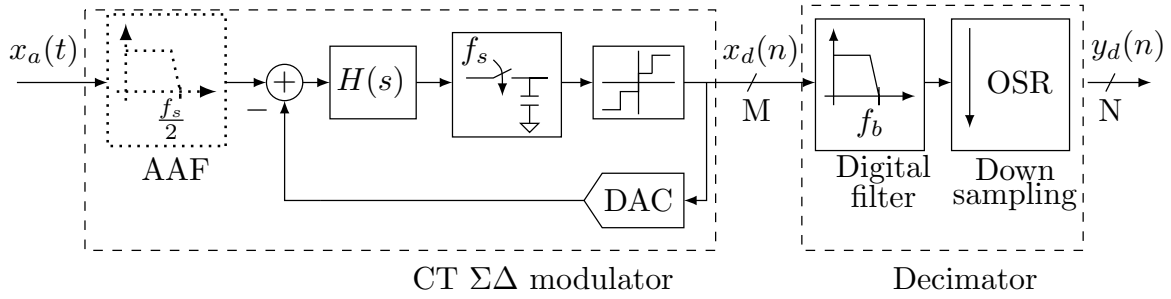


Figure 2.19: Continuous-time ΣΔ ADC.

frequency since the accuracy depends on the complete charge transfer and this commonly requires a small fraction of the clock period. Otherwise, the latter deals with analog signals at the input filter, thus relaxing the frequency specifications of the amplifier because the signal bandwidth is smaller than the clock frequency. Another concern about the filter implementation is the behavior of the virtual ground node. Although the DT-ΣΔM presents large glitches at its virtual ground, this is not relevant as it only matters the final settled value. In contrast, the virtual ground in a continuous time implementation must remain constant so that the linearity of the integration operation is not affected[7].

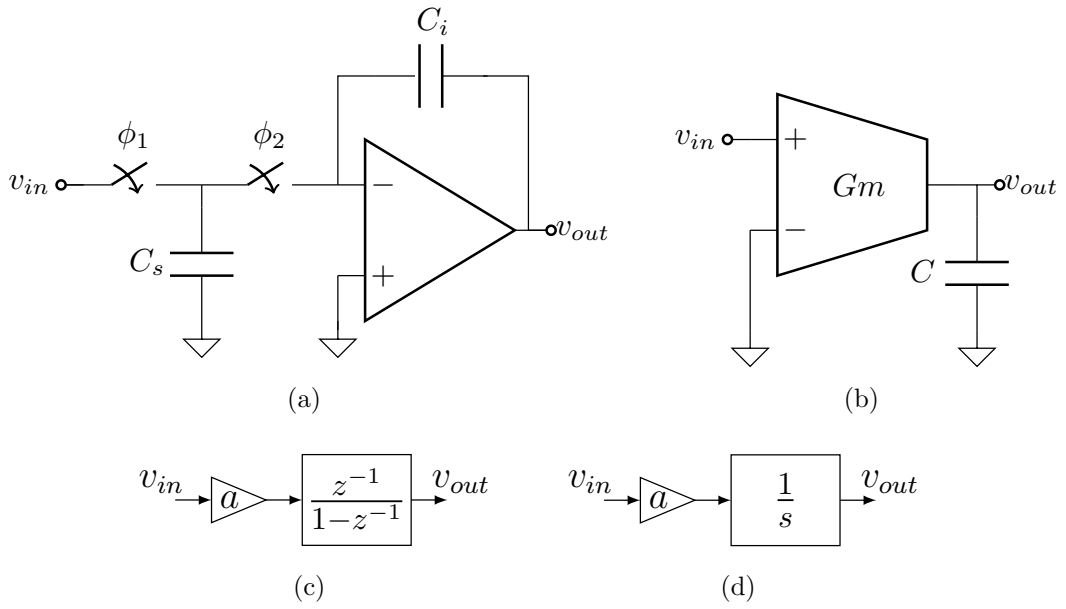


Figure 2.20: (a)SC integrator, (b)OTA-C integrator and (c), (d)their respective linear models.

From figures 2.20(c) and 2.20(d), it can be observed that the linear model of the integrators has a gain which for the SC circuit is

$$a = \frac{C_s}{C_i} \tag{2.31}$$

and, for OTA-C integrator

$$a = \frac{Gm}{C}. \tag{2.32}$$

When the integrators are used to implement a $\Sigma\Delta$ modulator, they are called coefficients and play an important roll in both the performance and stability of the modulator. In a SC implementation, the gain is determined by the ratio between two capacitors, and thus the variation of the coefficients due to fabrication process defects is relative small. By contrast, the coefficient implemented by the continuous-time integrator depends on the absolute values of Gm and C, which may cause substantial performance degradation or system instability.

Furthermore, note that the output in a continuous-time $\Sigma\Delta$ modulator is digital, and must be transformed (by using a DAC) to the analog domain to feed the filter. Therefore the DAC in a CT implementation is a critical block and its performance has a big impact in the behavior of the modulator[14].

2.2.4 Quantizer

It is known that the ADC error is attenuated by the NTF, but this doesn't happen with the DAC errors, which are injected with the input signal. Consequently the linearity of the modulator has a strong dependency on the DAC linearity. In the case of a single-bit modulator, there is no linearity problem since the input-output characteristic of the DAC is inherently linear. The issue is that using only a 1-bit quantizer is not enough when high SNR values are required. This problem can be solved by using a higher filter order or increasing the OSR. However, as mentioned above, a higher filter order has stability problems since the 1-bit quantizer. This turns the system into non-linear and thereby the linear models are not accurate. For the same reason, at high OSR values appears idle tones in the output spectrum. In addition, the white noise model for the quantization noise is not verified when using low resolution quantizers[2].

Another option to increase the resolution of the modulator is to use a multi-bit DAC. This enhances by 6db the SNR for every bit added (see Eq. 2.22). It also makes the system more linear and therefore the theory of linear networks is more accurate to predict the system behavior, and the quantization noise fits better in the white noise approximation. It is worth mentioning that the linearity of the modulator response is different from the linearity of the system. The first one refers specifically to the integral non-linearity (INL) error of the DAC, which is the maximum deviation of the actual output from the ideal output; the second one concerns the accuracy with which a linear model represents a real system. Note that in order to not degrade the $\Sigma\Delta$ converter performance, the accuracy of the DAC

should at least as good as that of the system. Hence, for DAC resolutions greater than one, its INL must be less than 1LSB to preserve the response linearity [2]. This is not easy to accomplish in standard technologies, and thus an extra circuit is needed such as trimming or dynamic matching (more information in this issue can be found in [4]).

An advantage of using a single-bit modulator is that it is implemented with only a comparator as a quantizer and two reference voltages (V_{REF} and $-V_{REF}$) in the DAC. However, since single-bit modulators usually employ large OSR values, the amplifier requires a bandwidth that is three or four times the sampling frequency, which increases power consumption. As a contrast, the use of multilevel quantization improves the equivalent number of bits, but consumes additional power because of the extra circuits. Moreover, since a multi-bit architecture uses a smaller OSR, the specification of the bandwidth of the amplifiers can be relaxed. It can be noted that there is a trade-off between the number of bits and the power consumption of the circuit for a given signal bandwidth. In conclusion, single-bit architectures are a suitable solutions for low power application, and multi-bit architectures are more adequate for high-frequency and wide-band applications.

2.3 Architecture Selection

Since the modulator requirements specify a SNR greater than 96dB, a discrete-time second-order single-bit single-loop full feed-forward architecture was chosen (see Fig. 2.21). Basically a discrete-time single-bit architecture is suitable for the application since the signal bandwidth is located at low frequencies. Also, the architecture leads to an inherent linear circuit without wasting power and complexity to reach stability. In addition, the AAF does not need a high order since the system uses a high OSR.

The second and third order architectures with OSR= 256 and OSR= 128 respectively satisfy the specifications. The bias current of the additional integrator in the third order architecture could be used to reduce noise and extend the bandwidth of the integrators in a second-order modulator while achieving a slightly lower power consumption. Moreover, adding a third integrator implies to occupy more area for the switches and the capacitors. Also, the second-order architecture is more stable, which translates to fewer stability constrains for the integrators coefficients selection thereby facilitating the optimization of their output dynamic range. Consequently, the second-order architecture was chosen since one of the objectives of this dissertation is to optimize the system.

Finally, the full feed-forward topology was chosen since it offers the greater SNR_{peak} among other topologies for input amplitudes near V_{REF}. It is important to note that the values of the coefficients b_1 and b_2 in a distributed feedback topol-

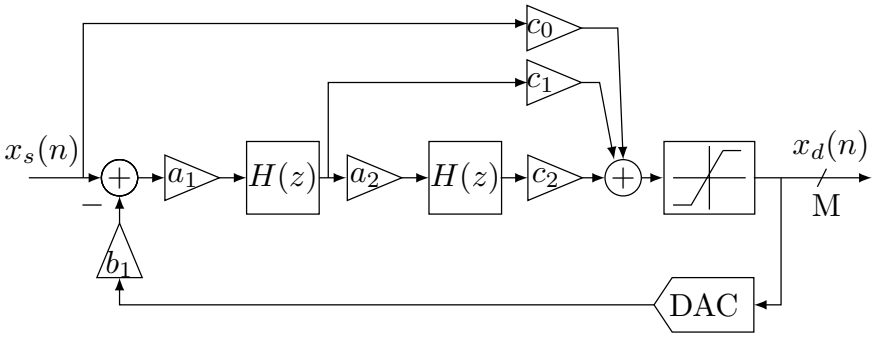


Figure 2.21: 2^{nd}-order fully feed-forward topology.

ogy are defined by the ratio between the output voltage levels of the DAC and the ADC. For instance, if the ADC output levels are $-V_{ADC}$ and V_{ADC} and the DAC reference voltage is V_{REF}, the value of the coefficient is given by V_{ref}/V_{ADC}. When the modulator has differential operation it uses two symmetrical reference voltages (V_{REFP} and V_{REFN}) around the common-mode ($V_{cm} = V_{DDA}/2$). Therefore, in order to avoid using extra reference circuits (that increase area, power consumption and circuit complexity) to implement the feedback coefficients, the full feed-forward is the best option. To conclude, the specifications of the modulator are listed in Table 2.1.

Table 2.1: Modulator Specifications

Parameters	**Value**
SNR_{peak}	$>$ 96dB
BW	40-1.9KHz
OSR	256
f_s	1MHz
V_{DD}	1.8V
Order	2
Loop Topology	Full feed-forward
Domain	DT
ADC levels	2

2.4 Related Works

In the literature there are many implementations of a $\Sigma\Delta$ modulator in low-medium frequencies, specially for audio and bio-potential applications. Neither have similar requirements (except ENG signals) to the present application. As a contrast, in the field of electric energy measurement, it was reported only one paper [16].

Table 2.2 shows relevant works about circuit implementations of a $\Sigma\Delta$ modulator

Table 2.2: Related Works

Ref.	**V_{DD}** [V]	**BW** [KHz]	**OSR**	**f_s** [MHz]	**SNDR** [dB]	**Pow.** [μW]	**FOM_1** [pJ/step]	**FOM_2** [dB]	**ENOB** bit
[17]	1.2	10	128	2.560	87.8	148	0.37	166.1	14.3
[18]	1.6	2	80	0.320	64	96	18.53	137.2	10.3
[19]	1.8	10	64	1.280	95	210	0.23	171.8	15.5
[20]	0.8	10	40	0.800	82	48	0.23	165.2	13.3
[16]	1.2	14	128	3.584	99	316	0.15	175.5	16.2
[21]	0.8	10	128	2.560	80.3	54	0.32	163.0	13.0
[22]	0.9	0.5	250	0.250	76	2.1	0.41	159.8	12.3
[23]	0.25	10	70	1.400	61	7.5	0.41	152.2	9.8
[24]	1.5	1	128	0.256	93	1350	18.49	151.7	15.2
[25]	1.5	1	64	0.128	89.8	20	0.40	166.8	14.6
[26]	1.8	1	16	0.032	80	9	0.55	160.5	13.0
[27]	2.5	1	128	0.256	93.2	2380	31.85	149.4	15.2
[28]	1.8	10	250	5.000	85.8	33	0.10	170.6	14.0
[29]	1	8	40	1.048	92	38	0.07	175.2	15.0
[30]	1	2	64	0.256	60	5	1.53	146.0	9.7
[31]	2	1	128	0.320	77	120	10.37	146.2	12.5
[32]	0.8	5	64	0.640	47.5	180	92.91	121.9	7.6
[33]	0.9	10	256	5.000	80.1	200	1.21	157.1	13.0
[34]	3.3	10	256	5.120	99	1630	1.12	166.9	16.2
[35]	1.8	4	125	1.000	68	400	24.36	138.0	11.0
[36]	1.5	3.9	128	1.000	67.1	90	6.23	143.5	10.9
[37]	0.7	8	64	1.024	67	80	2.73	147.0	10.8

that although are not related with energy measurement, have somewhat similar specifications. It was considered only recent implementations (from 2002 to 2013) with a bandwidth between 500 and 10KHz. This is important since the power consumption and the criteria to chose an specific architecture heavily depends of the signal bandwidth. The comparison is also based on both figure-of-merit (FOM) which are determined by:

$$\text{FOM}_1 = \frac{\text{Power}}{2 \cdot \text{BW} \cdot 2^{\text{ENOB}}} \quad ; \quad \text{FOM}_2 = \text{SNDR}_{peak} + 10log_{10}.\left(\frac{\text{BW}}{\text{Power}}\right) \tag{2.33}$$

In Table 2.3 is detailed the technology and the architecture employed to implement the modulator. It is important to mention that each work improves the modulator response using techniques at circuit-level. The architectures in most of cases are based in the well-known theory. The abbreviations in the architecture field in Table 2.3 refer to the domain, the order of the loop filter, the number of levels of the ADC and the loop topology.

Table 2.3: Related Works (cont)

Ref.	**Tech.** [μm]	**Architecture**	**Year**
[17]	0.13	DT-2o-5ADC-DFB	2013
[18]	0.15	CT-3o-2ADC-FFF	2013
[19]	0.18	SC-2o-17ADC-FFF	2012
[20]	0.13	DT-2o-17ADC-FFF	2012
[16]	0.13	DT-2o-2ADC-FFF	2012
[21]	0.18	DT-3o-2ADC-FFS-LFL	2012
[22]	0.065	DT-2o-2ADC-DFB	2012
[23]	0.13	DT-3o-2ADC-FFF	2011
[24]	0.18	DT-3o-2ADC-FFF	2011
[25]	0.35	DT-4o-2ADC-FFS-LFL	2010
[26]	0.35	DT-5o-17ADC-FFF	2010
[27]	0.18	DT-3o-2ADC-FFS-LFL	2010
[28]	0.18	DT-2o-2ADC-HYB	2010
[29]	0.13	DT-3o-2ADC-FFF	2009
[30]	0.35	CT-2o-2ADC-DFB	2007
[31]	0.35	DT-2o-2ADC-DFB	2007
[32]	0.18	DT-2o-2ADC-DFB	2006
[33]	0.18	DT-2o-2ADC-DFB	2006
[34]	0.18	DT-2o-2ADC-DFB	2005
[35]	0.18	DT-2o-2ADC-DFB	2005
[36]	0.35	DT-2o-2ADC-DFB	2004
[37]	0.18	DT-2o-2ADC-DFB	2002

Chapter 3

System Level Design

The present chapter focuses on the design and definition of the parameters of the blocks of the architecture, which are the DAC, the coefficients and the integrators. Since the DAC is a simple block, the relevant parameter at this design-level is its voltage reference. It is worth noting that this value determines the output swing of the signal at the first integrator and sets the feedback coefficient value. The values of the remaining four coefficients were obtained simulating the ideal model of the modulator for every combination of coefficients, seeking the maximum values of SNR at a given input amplitude. The optimal coefficient values were the ones that provided maximum SNR and occupied the lowest area. Finally, the non-idealities of the first integrator, which is the major source of errors in a single-bit architecture, were characterized and specified in order to not degrade the system performance. The simulations were done using Simulink models based on [1].

3.1 Simulink Models

In order to predict the system level behavior and help in the design procedure, three Simulink models were elaborated: ideal, noiseless non-ideal and noisy non-ideal. The former consists of ideal integrators, coefficients and an ideal quantizer (see Fig. 3.1). Despite the fact that this is an ideal model, the saturation voltage of the integrator was set at the standard supply voltage of the technology ($V_{DD} = 1.8V$) to assure that the output of each integrator does not exceed the maximum allowed voltage. This restriction is the key of the model since it reduces the combinations of coefficients that attain the SNR specified for a given input amplitude. Thus, the model was basically used to iterate the coefficients until the desired response was reached. On the other hand, the output spectrum helps to estimate an accurate quantization noise power in the signal band, since the hand-calculation values are not accurate due to the 1-bit quantizer.

A second model (shown in Fig. 3.2) was elaborated including the non-ideal

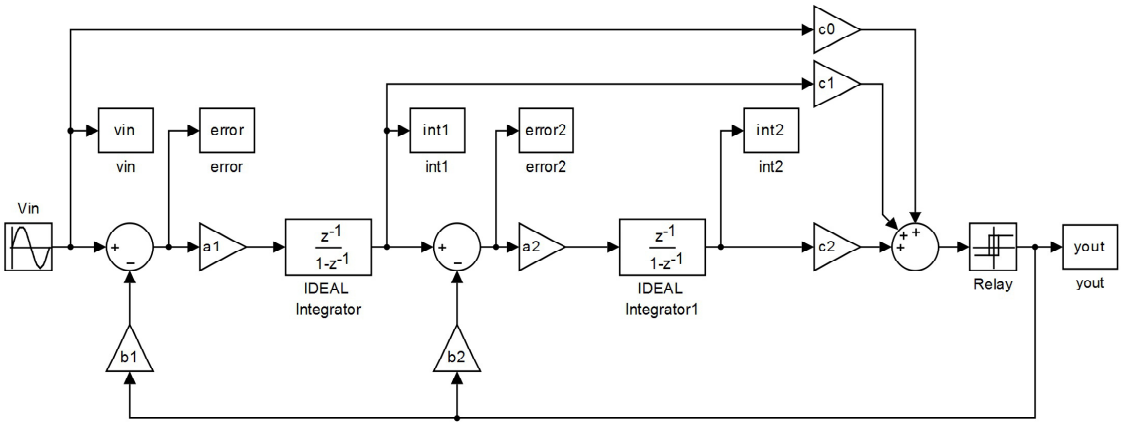


Figure 3.1: Ideal Simulink model of full feed-forward second-order ΣΔ modulator.

integrator developed in [1]. The Simulink block models the GBW, the DC gain, the slew-rate and the saturation voltage of the amplifier (that is part of the integrator), and thereby predicts their effects on the modulator response. The results are used to verify that the specifications of the amplifier do not degrade the SNR of the ideal modulator.

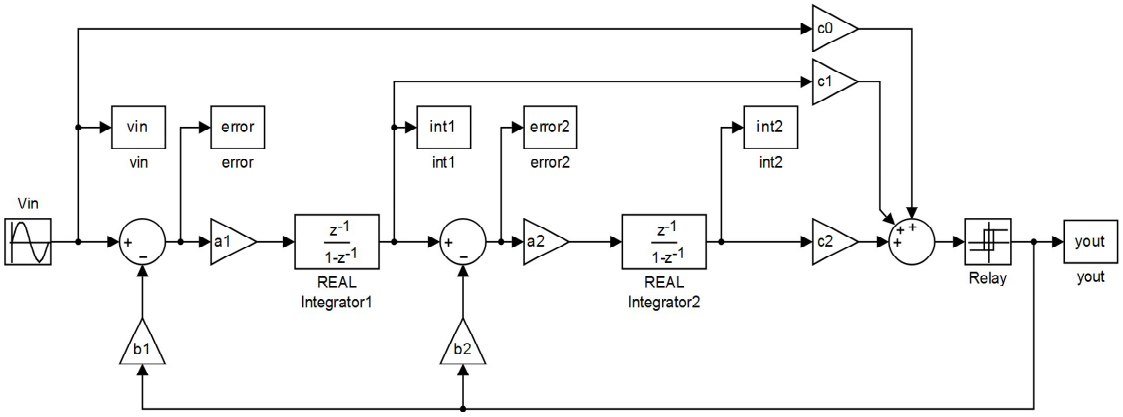


Figure 3.2: Non-ideal Simulink model of full feed-forward second-order ΣΔ modulator.

Another important parameter to take into account is the noise generated by the switching network (kT/C) and the devices (basically the amplifier). Thus, the functions developed in [1] are added to the non-ideal model to elaborate the noisy non-ideal model (see Fig. 3.3). It includes the main noise sources and adds two more inputs which are the first sampling capacitor value and the input root-mean-square (RMS) noise voltage of the amplifier. The capacitor value is used to calculate the power spectral density (PSD) of the switching network and the RMS noise voltage, to calculate the contribution of the amplifier in the total noise power at the output.

Using a circuit simulator is not suitable for a first estimation of noise in ΣΔ modulators because it takes long simulation time due to the fact that it is a nonlinear mixed-signal circuit. Thus, this model was used to predict the final response of the

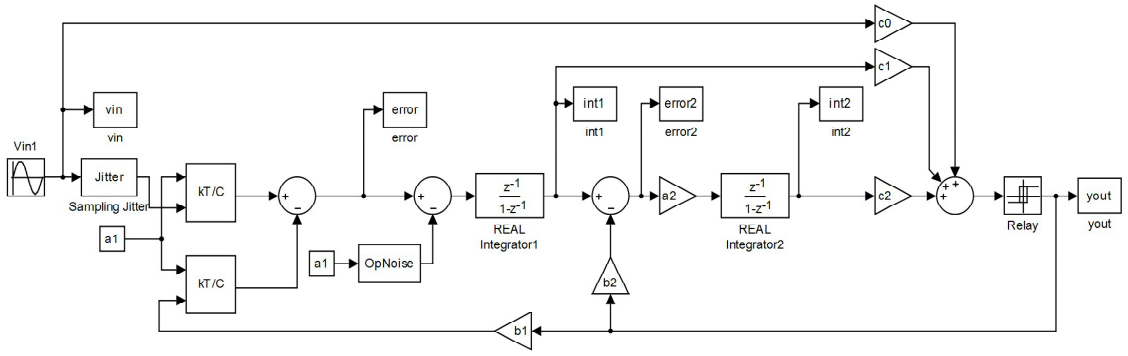


Figure 3.3: Noisy non-ideal Simulink model of full feed-forward second-order $\Sigma\Delta$ Modulator.

modulator in less time than a transistor-based model.

3.2 DAC Reference Voltage

The 1-bit DAC is the simplest DAC and provides an inherent linearity to the modulator. It consists of two reference voltages (V_{REF} and $-V_{REF}$) that switch between them depending on the input. In the modulator, the value V_{REF} defines the feedback coefficient (as mentioned in the previous chapter). It also has a big impact on the output dynamic range of the first integrator since the DAC output is subtracted from the input signal and the result is applied to the integrator.

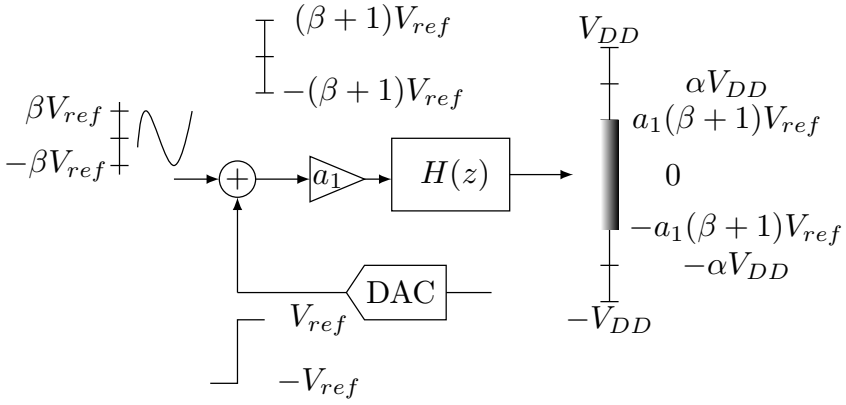


Figure 3.4: Effect of the DAC in the output dynamic range of the first integrator.

Figure 3.4 illustrates the voltage levels at the first integrator. It is observed that the DAC output is subtracted from the input sine with amplitude βV_{REF}. Thus, the voltage range of the difference (also called as error) is the sum of both ($\beta V_{REF} + V_{REF}$) since there is the case in which one reach its maximum while the other attains its minimum. Note that the input amplitude is a fraction of the V_{REF} and it is represented by the factor β. The error is scaled by the coefficient and

processed by the integrator, thereby obtaining a signal that ranges from $-a_1(\beta + 1)V_{REF}$ to $a_1(\beta + 1)V_{REF}$ at the integrator output. Therefore, assuming that the output dynamic range of the integrator is $2\alpha V_{DD}$, the reference voltage is limited to:

$$V_{REF} < \frac{\alpha V_{DD}}{(\beta + 1)a_1} \tag{3.1}$$

Typically, for classical topologies of amplifiers in the present technology (AMS018), the value of α is greater than 0.9. Also, it is known that the coefficient of the first integrator is always less than one. Thus it is assumed that its maximum value is 0.8. The factor β defines the input range of the modulator and it was arbitrarily set to 0.9 to operate in a wide input range. Replacing these values in the Eq. (3.1), the maximum V_{REF} allowed by the technology is 1.07V. Therefore, in order to accomplish this condition, the V_{REF} was set to 1V. Consequently the feedback coefficient was set to $b_1 = 0.56$.

3.3 Modulator Coefficients

In Chapter 2 it was defined that a discrete-time single-bit second-order $\Sigma\Delta$ modulator with full feed-forward topology (see Fig. 3.5) is able to achieve the application requirements. Note that the value of c_0 (see Fig. 2.16) was arbitrarily set to unity for two reasons. The first is that the STF at low frequencies is equal to 1 when $c_0 = 1$. Another is that since 1-bit ADC is used as a quantizer, the relevant information is the signal sign and not the amplitude. This means that the information that provides one coefficient is redundant and thereby it can be set to any value. The feed-forward coefficients and the adder are implemented by a passive circuit that uses one coefficient as reference[5]. Therefore, the STF and NTF of the modulator are given by:

$$STF = \frac{z^{-2}\left(a_1a_2c_2 - a_1c_1 + 1\right) + z^{-1}\left(a_1c_1 - 2\right) + 1}{z^{-2}\left(a_1a_2b_1c_2 - a_1b_1c_1 + 1\right) + z^{-1}\left(a_1b_1c_1 - 2\right) + 1}, \tag{3.2}$$

$$NTF = \frac{\left(1 - z^{-1}\right)^2}{z^{-2}\left(a_1a_2b_1c_2 - a_1b_1c_1 + 1\right) + z^{-1}\left(a_1b_1c_1 - 2\right) + 1} \tag{3.3}$$

where the stability condition of the system is

$$a_2\frac{c_2}{c_1} < 1. \tag{3.4}$$

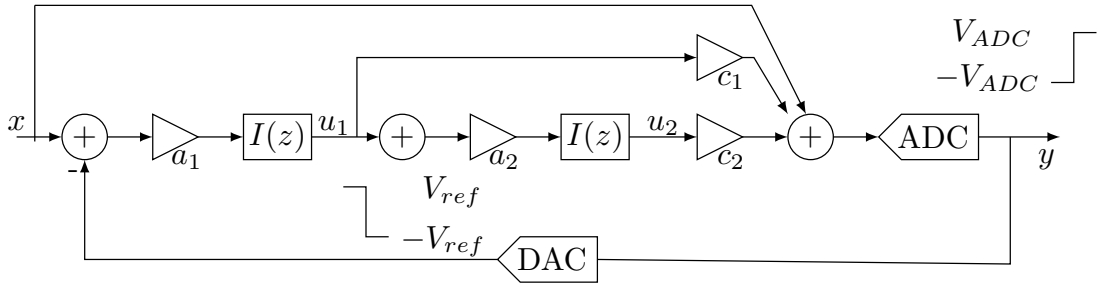


Figure 3.5: Discrete time 2^{nd} order full feed-forward $\Sigma\Delta$ modulator.

3.3.1 SNR Optimization

According to the top-bottom design flow shown in Chapter 1, the architecture was optimized by exploring the design space (a_1, a_2, c_1 and c_2). The goal was to find the SNR maxima for a specific input amplitude which is $A_{in} = 0.9V_{REF}$. With this purpose, the ideal model was simulated for every combination of the coefficients. The coefficients $a1$ and a_2 were varied from 0.1 to 0.9 with steps of 0.1, and c_1 and c_2 were varied from 0.5 to 2.5 with steps of 0.25. The compilation of the maximum values of SNR are listed in Table 3.1, which also shows the absolute value of the swing voltage at the first($int_{out,1}$) and second($int_{out,1}$) integrator outputs.

Table 3.1: SNR maximums

a_1	a_2	c_1	c_2	$int_{out,1}$	$int_{out,2}$	SNR	ENOB	γ
0.6	0.2	0.5	1	0.9	0.9	104.7	17.09	5.42
0.3	0.4	1	1	0.5	0.9	104.7	17.09	6.71
0.7	0.4	1	1	1	1.4	105.1	17.17	4.80
0.3	0.2	1	2	0.45	0.45	104.7	17.09	7.83
0.7	0.2	1	2	1	0.8	105.1	17.17	5.93
0.2	0.6	1.5	1	0.3	0.9	104.7	17.09	8.42
0.2	0.4	1.5	1.5	0.3	0.6	104.7	17.09	8.88
0.2	0.3	1.5	2	0.3	0.45	104.7	17.09	9.33
0.5	0.5	0.75	0.5	0.75	1.6	104.2	17.02	4.88
0.4	0.6	0.75	0.5	0.6	1.7	104.2	17.01	5.29
0.4	0.3	0.75	1	0.6	0.8	104.7	17.09	5.96
0.4	0.2	0.75	1.5	0.6	0.6	104.7	17.09	6.63
0.5	0.2	0.75	1.25	0.7	0.6	104.2	17.02	6.00
0.3	0.9	1.25	0.5	0.4	1.6	104.4	17.04	6.24
0.3	0.3	1.25	1.5	0.4	0.6	104.4	17.04	7.29
0.3	0.2	1.25	2.25	0.4	0.4	104.4	17.04	8.08
0.4	0.7	1.75	1	0.6	1.5	105.1	17.17	5.98
0.4	0.4	1.75	1.75	0.6	0.8	105.1	17.17	6.63
0.4	0.3	1.75	2.25	0.6	0.6	104.5	17.07	7.08
0.2	0.8	2.25	1	0.3	0.8	104.2	17.02	8.69
0.2	0.4	2.25	2	0.3	0.4	104.2	17.02	9.50

The coefficients $a1$ and a_2 are implemented as the ratios of two capacitances: C_{s1}/C_{i1} and C_{s2}/C_{i2}, respectively. On the other hand, the feed-forward coefficients in single-bit architectures are defined by the value of a single capacitor. For instance, if the capacitor that implements $c_0 = 1$ is C_{f0}, the value of C_{f1} and C_{f2} are c_1C_{f0} and c_2C_{f0}, respectively. Thus it can be noticed that the total capacitance of the circuit depends of the coefficients, and it is given by:

$$C_{tot} = C_f(1 + c_1 + c_2) + C_{s1}\left(\frac{a_1 + 1}{a_1}\right) + C_{s2}\left(\frac{a_2 + 1}{a_2}\right) \tag{3.5}$$

Typically the capacitances C_{s2} and C_{f0} are smaller than C_{s1}. Hence, it is arbitrarily assumed that $C_{s2} = 0.25C_{s1}$ and $C_{f0} = 0.5C_{s1}$. Considering these assumptions, the expression of C_{tot} can be rewritten as:

$$C_{tot} = C_{s1}\left(\frac{a_1 + 1}{a_1} + \frac{a_2 + 1}{4a_2} + \frac{1 + c_1 + c_2}{2}\right) = \gamma C_{s1} \tag{3.6}$$

where γ is the factor that indicates the effect on the coefficient values in the total capacitance area. The minimum value of γ in Table 3.1 represents a solution for minimum area and maximum SNR. Therefore, based on data in Table 3.1, the selected coefficients were: $a_1 = 0.7$,$a_2 = 0.4$,$c_1 = 1$,$c_2 = 1$.

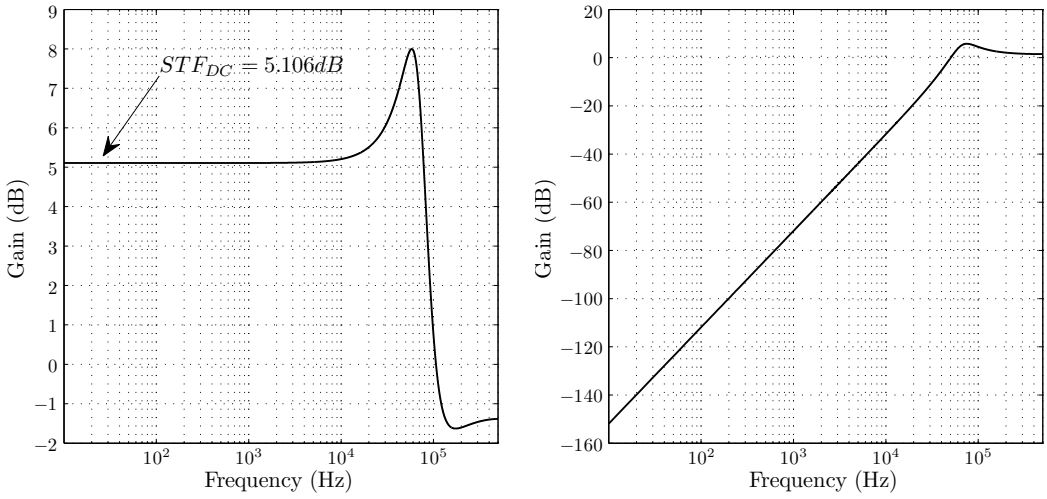
The simulation of the ideal model and the following simulations in this dissertation were done using the parameters listed in table 3.2 unless otherwise indicated. The reference voltage (V_{REF}) and the ADC output voltage (V_{ADC}) are the output voltage levels of the DAC and ADC respectively (see Fig. 3.5). The parameters A_{in} and f_{sin} are the characteristics of the input sine of the modulator. It is important to note that the input frequency is proportionally to the frequency resolution(f_s/N) and near to 1.8KHz (the last frequency component of the electrical signal).

Table 3.2: Simulation Parameters

Parameter	**Symbol**	**Value**
Boltzmann's constant	k	$1.381 \times 10^{-23} J/K$
Temperature	T	$300K$
Number of samples	N	65536
Reference Voltage	V_{REF}	$1V$
Switching Frequency	f_s	1MHz
ADC output voltage	V_{ADC}	$1.8V$
Input amplitude	A_{in}	$0.9V_{ref}$
Input Frequency	f_{sin}	$117\frac{f_s}{N}$
Information bandwidth	Bw	$\frac{f_s/2}{OSR}$
Oversampling ratio	OSR	256

3.3.2 Ideal Modulator Response

The bode plots of the STF and NTF are shown in Fig. 3.6. The STF plot indicates its DC Gain (STF_{DC}) which is $5.106dB$ and is determined by the inverse of the feedback coefficient ($1/b_1 = V_{ADC}/V_{REF} = 1.8$). As expected, the NTF has a second-order high-pass filter response (see Fig. 3.6(b)) which attenuates the quantization noise of the 1-bit ADC at low frequencies. Moreover the NTF only attenuates the quantization noise rather than other noise sources such as the kT/C or the amplifier noise.



(a) STF (b) NTF

Figure 3.6: Frequency responses of the ΣΔ Modulator.

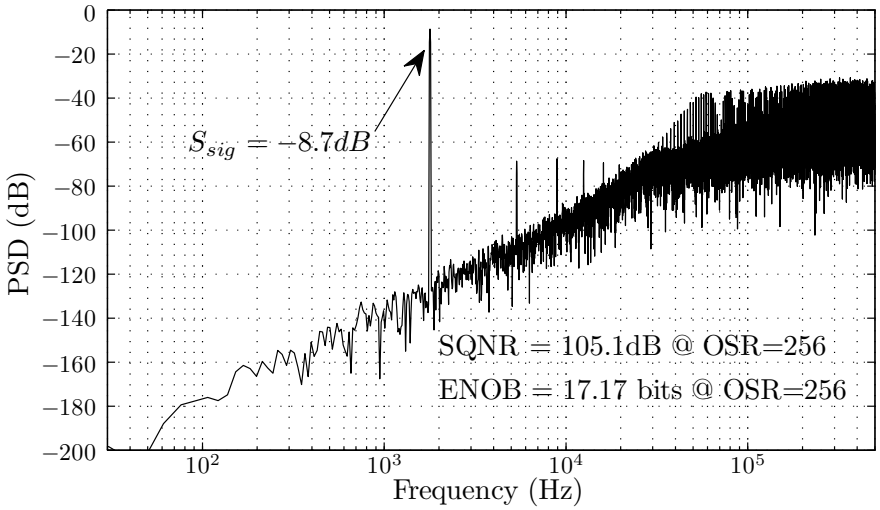


Figure 3.7: PSD of the output signal.

The PSD of the output signal is shown in Fig. 3.7. It indicates that the normalized signal power is $-8.7dB$ and the SQNR is $105.1dB$. Knowing these values and

using the denormalized signal power ($1.18dB$), we can compute the mean square voltage of the quantization noise ($\bar{v^2}_{n,q}$) using the following equation:

$$\bar{v^2}_{n,q} = \bar{v^2}_{sig} - SQNR = -103.92dB, \tag{3.7}$$

which is equivalent to:

$$\bar{v^2}_{n,q} = 40.55pV^2. \tag{3.8}$$

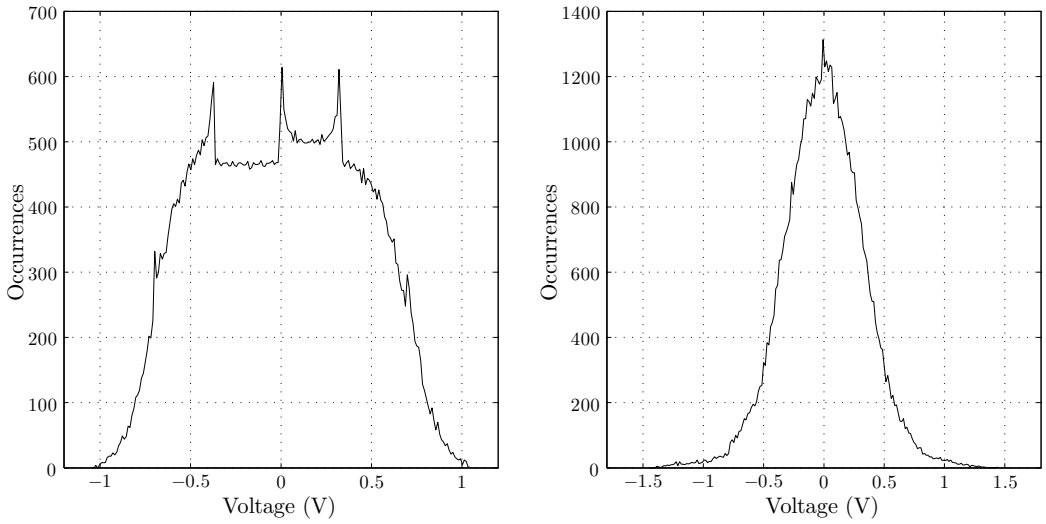
Since the minimum ENOB requirement of the modulator is 16 bits, which is equivalent to a minimum SNR (SNR_{min}) of $98.08dB$, the maximum allowable noise power in the modulator (considering all the noise sources) is restricted to the following value:

$$\bar{v^2}_{n,out} = \bar{v^2}_{sig} - SNR_{min} = -96.9dB, \tag{3.9}$$

which is equivalent to:

$$\bar{v^2}_{n,out} = 204.17pV^2. \tag{3.10}$$

From these values, it can be observed that the quantization noise is equivalent to 20% of the maximum noise allowable by the system. Indeed, this percentage cannot be reduced since it is inherent of the modulator loop. Hence, other noise sources such as the switching network and the amplifier must not surpass the remaining 80%.



(a) First Integrator (b) Second Integrator

Figure 3.8: Histogram of the integrators outputs.

The histograms of the integrator outputs are shown in Fig. 3.8. It can be

observed that the output voltage of the first integrator swings from -1 to 1 and of the second integrator goes from -1.4 to 1.4. Both are in the range of a typical amplifier response which means that special circuit techniques are not needed.

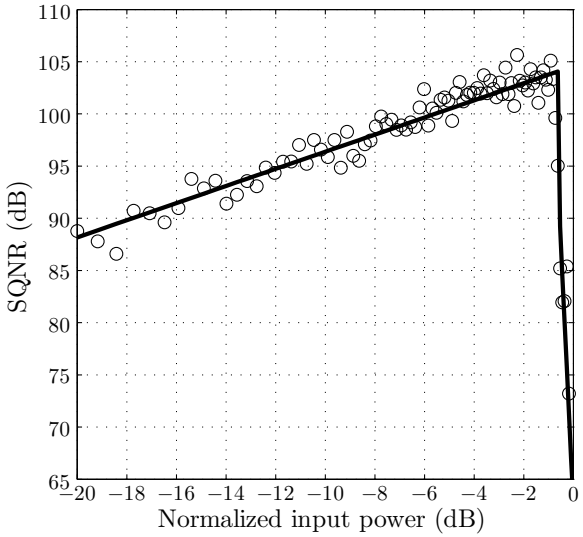


Figure 3.9: SQNR as a function of the input power.

Figure 3.9 shows the behavior of the SQNR with the input power. As expected, the plot attains its maximum for amplitudes near to $0.9V_{REF}$. The circles represent the values obtained from simulations and the solid line is a linear approximation of the data.

3.4 Non-ideal Integrator

The amplifier non-idealities such as finite DC gain (A_{DC}), slew-rate (SR), gain-bandwidth product (GBW) and saturation voltage (V_{SAT}) are the causes of the incomplete transfer of charge in a switched-capacitor integrator (see Fig. 3.10). Moreover, the noise of the integrator is the major cause of the SNR degradation in the $\Sigma\Delta$ modulator. It is important to note that the first four non-idealities can be specified considering the preservation of the ideal response of the circuit. On the other hand, the noise sources cannot be avoided, and hence have a big impact on the SNR of the system. Those effects were analyzed and modeled in [4],[1],[38] and [39].

3.4.1 Finite DC Gain

The transfer function of an ideal switched-capacitor integrator is given by the following expression:

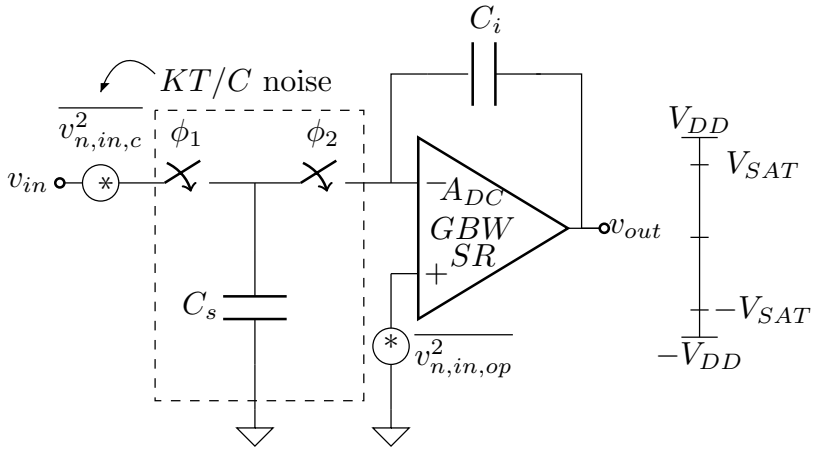


Figure 3.10: Non-idealities of a discrete-time integrator.

$$H(z) = b\frac{z^{-1}}{1 - z^{-1}}. \tag{3.11}$$

It can be observed that besides the implementation of the forward-Euler integrator, the circuit also implements a coefficient which is represented by b. The DC gain of the amplifier affects both, the coefficient and the frequency response. Thus, in order to model this effect, a factor $\alpha = 1 - b/A_{DC}$ is introduced and the transfer function is rewritten as:

$$H(z) = b\alpha\frac{z^{-1}}{1 - \alpha z^{-1}}. \tag{3.12}$$

If the maximum allowable error due to the DC gain of the amplifier is 0.1%, then the value of b/A_{DC} (part of the factor α) is limited to the following condition:

$$\frac{b}{A_{DC}} < 0.001, \tag{3.13}$$

which restricts A_{DC} to

$$A_{DC} > 56.9dB. \tag{3.14}$$

In [38], this effect was modeled using Simulink blocks in which the frequency response was separated from the integrator coefficient. The factor α was modeled as a leakage in the frequency response and the effect of the DC gain in the coefficient was introduced in the slew-rate and GBW model (see Figure 3.11).

3.4.2 Slew-Rate and Gain-Bandwidth Product

The settling-time of the integrator is affected by the SR and GBW of the amplifier. The former is the maximum rate of change of the output voltage for a linear response, and the latter determines the time constant (τ) of the amplifier [40]. The effects of

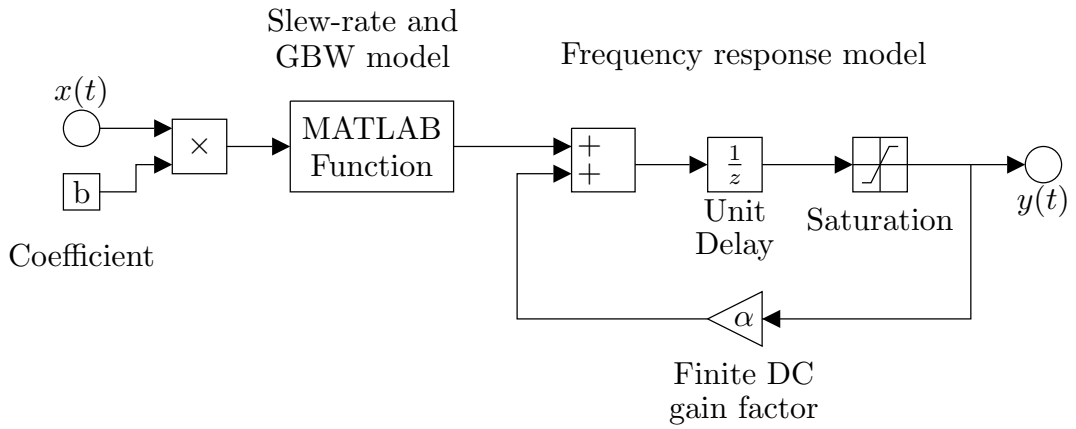


Figure 3.11: Non-ideal integrator developed in [1].

these parameters in a $\Sigma\Delta$ modulator were analyzed in [38] and more extensively in [39].

Considering that $V_s = V_{in}(nT - T/2)$ is the sampling voltage stored in C_s when ϕ_1 was on, the expression of the integrator output in ϕ_2[1] is given by:

$$v_{out}(t) = v_{out}(nT - T) + b\alpha V_s \left(1 - e^{-\frac{t}{\tau}}\right), 0 < t < \frac{T_s}{2}, \tag{3.15}$$

where τ is determined by $1/(2\pi GBW)$. It is important to mention that the GBW is not the same for both clock phases. It depends on the effective load capacitance at each phase. The maximum slope of the output voltage occurs at $t = 0$ and is shown in the following equation:

$$\left.\frac{dv_{out}(t)}{dt}\right|_{max} = b\alpha\frac{V_s}{\tau}. \tag{3.16}$$

This expression represents the minimum slew-rate required by the amplifier to attain a linear output response. In the case that the amplifier has a slew-rate lower than Eq. (3.16), the settling-time is only affected by the GBW. Otherwise, the amplifier is in slewing and the time response is influenced by this non-linear effect. If the maximum permissible settling-time is arbitrarily set to 5% of the clock period, then the maximum settling time is given by:

$$t_{set,max} = \frac{0.05}{f_s} = 50nsec. \tag{3.17}$$

Consequently, the GBW is conditioned to:

$$GBW > 3.2MHz. \tag{3.18}$$

[1] between $nT_s - T_s/2$ and nT_s

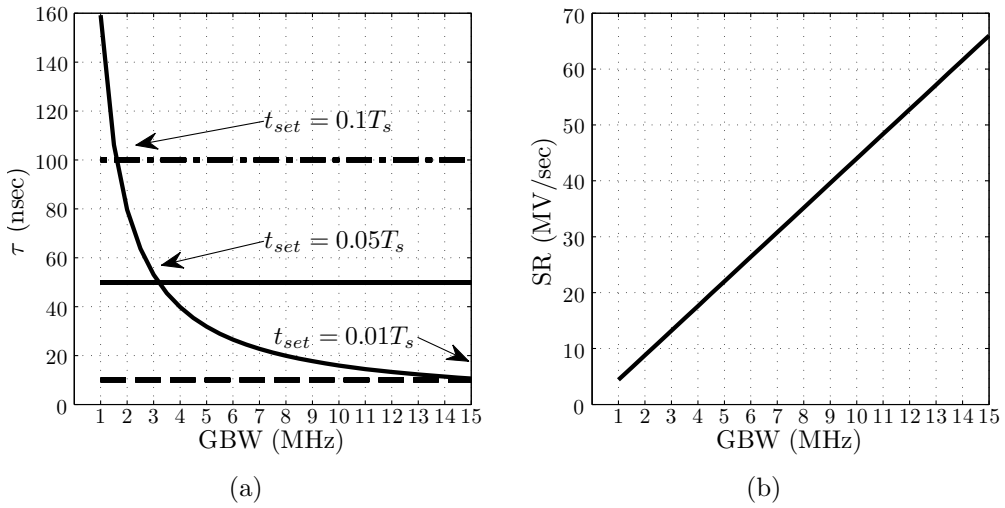


Figure 3.12: SR_{min}(a) and τ(b) vs. GBW.

Figure 3.12(a) shows the minimum GBW required for different settling-times. It is worth mentioning that a larger GBW is equivalent to a higher power consumption. Also, in Fig. 3.12(b), it can be observed that the minimum SR increases proportionally to the GBW. Depending on the equivalent output capacitance of the amplifier, reaching a high SR value may require a considerable power consumption. Therefore, the parameters must be keep as small as possible such that the SNR of the modulator is preserved and the power consumption is not wasted.

It is known that the amplifier response is affected by variations of the fabrication process, temperature and supply voltage variations. This means that the GBW has a nominal, a minimum and a maximum value. Thus, considering a maximum GBW of $5MHz$, the SR is conditioned to:

$$SR > 21MV/sec. \tag{3.19}$$

3.4.3 Saturation Voltage

The minimum output swing of the first and second integrators can be deduced from Fig. 3.8, wherein the output voltage is lower than 1.2V and 1.6V, respectively. As mentioned above, this was modeled in [38] using a Simulink saturation block (see Fig. 3.11). It is worth mentioning that when the output voltage is closer to the limits, the response is distorted.

3.4.4 Noise

The Simulink model of the noisy integrator developed in [1] was used to simulate the $\Sigma\Delta$ modulator at this design stage. It considers the capacitor and amplifier noise

assuming ideal switches (see Fig. 3.13). The inputs of the model are the values of the capacitor and the RMS noise voltage of the amplifier integrated in the signal band. Thus, the following analysis was done according to these entries.

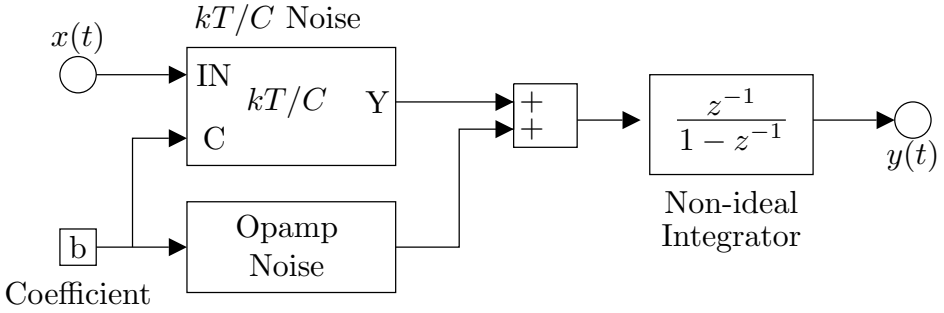


Figure 3.13: Noisy integrator developed in [1].

The sum of the quantization noise and the noise contribution of the integrator is limited to the following condition:

$$\overline{v_{n,tot_{max}}^2} > \overline{v_{n,out,int}^2} + \overline{v_{n,q}^2}. \tag{3.20}$$

which entails that the output power noise of the modulator due to the first integrator is restricted to:

$$164pV^2 > \overline{v_{n,out,int}^2}. \tag{3.21}$$

As it mentioned above, the switch noise was not considered at this level stage, and therefore the output power noise of the integrator is composed only by the following noise sources:

$$\overline{v_{n,out,int}^2} = \overline{v_{n,out,c}^2} + \overline{v_{n,out,op}^2}, \tag{3.22}$$

where $\overline{v_{n,out,c}^2}$ and $\overline{v_{n,out,op}^2}$ are the integrated power noise of the switching network and the amplifier, respectively. The former is the integral (from 0 to $\frac{f_s/2}{OSR}$) of the product of the capacitor noise PSD ($S_{n,in,c}$) and the square of the transfer function from the first integrator input towards the modulator output (NTF_{i1}) divided by the Nyquist frequency. The expression is shown in the following equation[4]:

$$\overline{v_{n,out,c}^2} = \frac{1}{f_s/2} \int_0^{\frac{f_s/2}{OSR}} S_{n,in,c} \left| NTF_{i1} \right|^2 df \tag{3.23}$$

where $S_{n,in,c}$ is determined by kT/C_{s1} and NTF_{i1} is given by:

$$NTF_{i1} = \frac{0.7z^{-1}\left(1 - 0.6z^{-1}\right)}{0.767z^{-2} - 1.61z^{-1} + 1}. \tag{3.24}$$

Using Eqs. (3.24) in (3.23) and solving the integral, the following relation is obtained:

$$\overline{v_{n,out,c}^2} = 12.4 \times 10^{-3} S_{n,in,c}. \tag{3.25}$$

The second component of the integrator noise is the integrated noise at the output of the modulator due to the amplifier. Since the input of the noisy integrator model is a RMS noise voltage and the NTF_{i1} is almost constant at low frequencies $(1/b_1)$, the integrated output power noise due the amplifier can be expressed as:

$$\overline{v_{n,out,op}^2} = |NTF_{i1}|^2 \, \overline{v_{n,in,op}^2} = \frac{1}{b^2} \overline{v_{n,in,op}^2}. \tag{3.26}$$

Therefore, the RMS input noise voltage is given by the square root of the noise power as shown in the following equation:

$$v_{n,in,op}^{rms} = \sqrt{\overline{v_{n,in,op}^2}} = b\sqrt{\overline{v_{n,out,op}^2}} \tag{3.27}$$

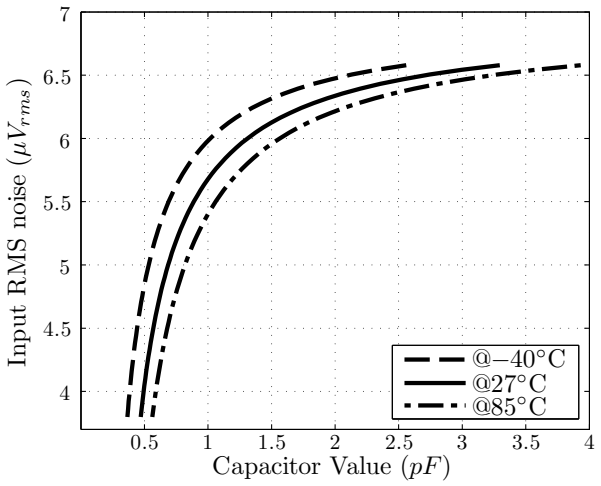


Figure 3.14: Maximum RMS noise voltage vs. minimum capacitor value.

The maximum allowable RMS noise voltage of the amplifier to achieve a SNR of 98.08dB depends on the sampling capacitor value and the temperature[2] (see Fig. 3.14). As expected for the highest temperature, the noise specification of the amplifier becomes tighter especially for capacitor values below $1pF$. This typically implies higher power consumption and larger transistors. Therefore, a capacitor value of $1.5pF$ is selected since it keeps the noise specification of the amplifier below $6\mu V_{rms}$ even at the maximum temperature. Only 95% of $164pV^2$ was considered as integrator noise power since the remaining 5% was attributed to fabrication process variations (which increase the amplifier noise), and external noise sources.

[2]It was considered a range of temperature of an industrial application from −40°C to 85°C.

3.4.5 Specification of the Analog Blocks

Table 3.3 summarizes the requirements of the amplifiers of the first and second integrators. It also shows the values used in the noise-less and noisy Simulink models.

Table 3.3: Amplifier Requirements

Parameter	**Condition INT1**	**Condition INT2**	**Simulink INT1**
A_{DC}	> 56.9dB	> 52.04dB	80dB
GBW	> 3.2MHz	> 3.2MHz	5MHz
SR	$> 21\text{MV}/sec$	$> 14.7\text{MV}/sec$	$30\text{MV}/sec$
V_{sat}	$> 1.2V$	$> 1.6V$	$1.6V$
$v_{n,in,op}^{rms}$	$< 6\mu V_{rms}$	–	$6\mu V_{rms}$

3.4.6 Noiseless Non-ideal Model Simulation

The noiseless non-ideal simulink model was simulated using the values listed in Table 3.3. The PSD of the output signal is shown in Fig. 3.15. It should be noted that there is not a significant difference between the ideal and the real-noiseless response. The SNR of the noiseless model differs from the ideal by only $0.6dB$. The histogram of each integrator output is not presented since it has the same response as the one of the ideal model. This is an expected response because the non-ideal parameters of the amplifier were chosen such that the ideal response of the modulator would not be affected.

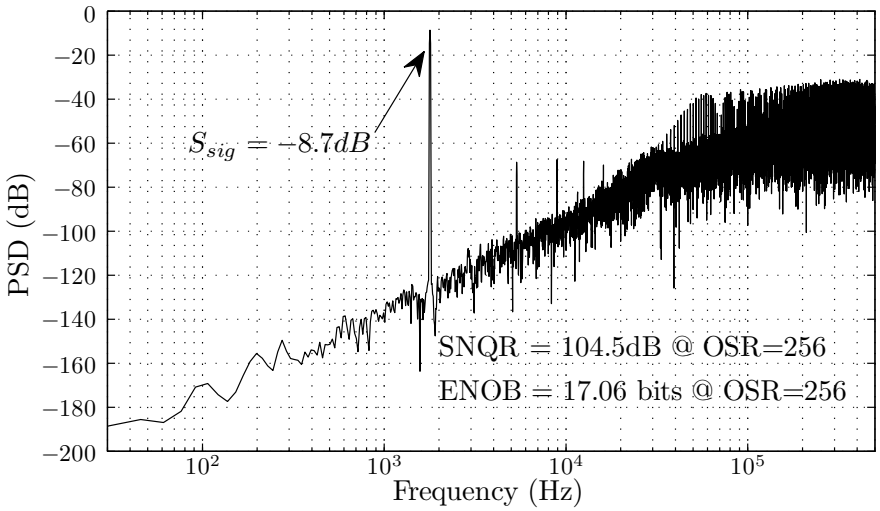


Figure 3.15: PSD of the output signal using the real-noiseless model.

3.4.7 Noisy Non-ideal Model Simulation

The noisy non-ideal model of the modulator was simulated using the values listed in Table 3.3. Furthermore, the inputs of the noisy integrator were $C_{s1} = 1.5pF$ and $v_{n,in,op}^{rms} = 6\mu V_{rms}$. The PSD of the output signal is shown in Fig. 3.16 where the SNR and ENOB values are given. As can be noted, the results agree with the theoretical analysis, and the main objective was achieved which is to reach an ENOB of 16 bits.

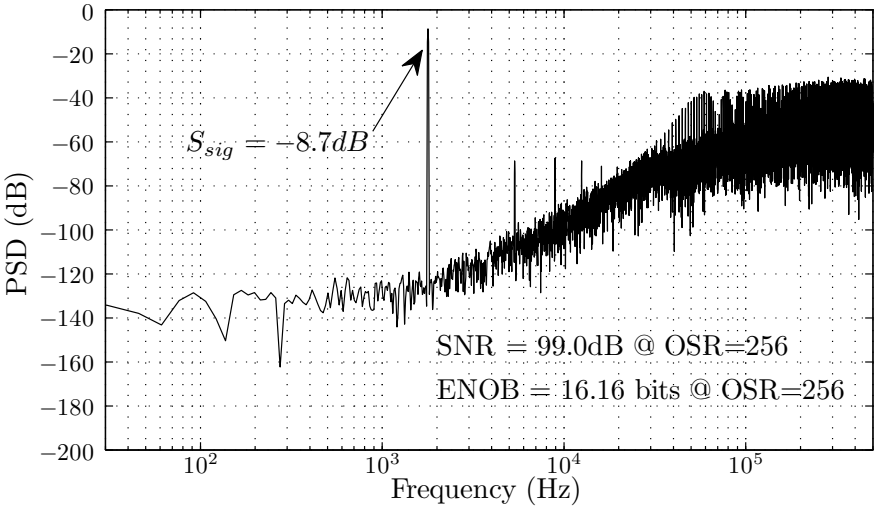
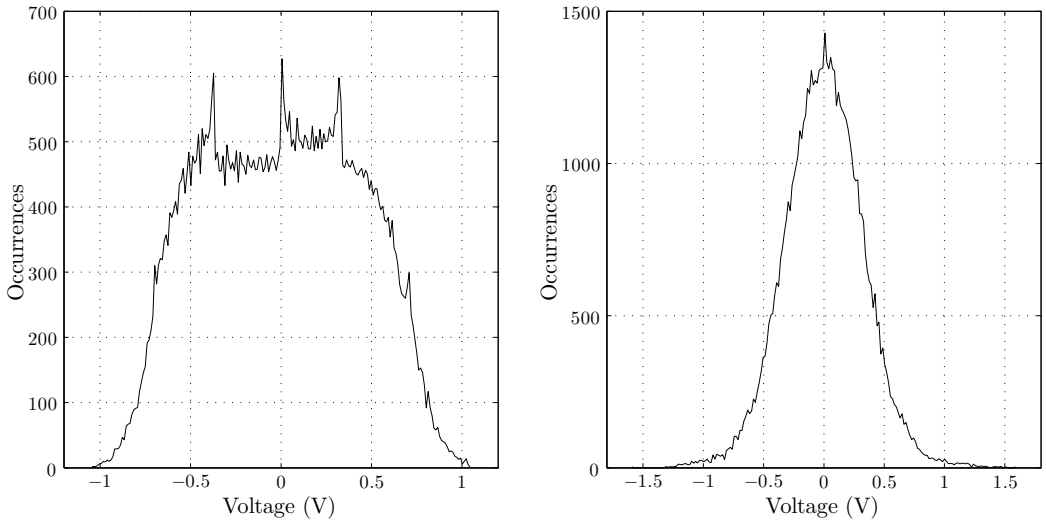


Figure 3.16: PSD of the output signal using a noisy non-ideal model.

The histogram of each integrator output is shown in Fig. 3.17, where it can be observed that the voltage ranges remains equal to that of the ideal model.



(a) First Integrator (b) Second Integrator

Figure 3.17: Histogram of the integrators output for noisy non-ideal simulation.

Finally, Fig. 3.18 shows the behavior of the SNR with of the input power. It can be observed that the modulator only achieves a SNR greater than 98.08dB for

values near to $0.9V_{REF}$. Thus, the PGA that preceded the $\Sigma\Delta$ ADC is unavoidable since it conditioned the input signal amplitude.

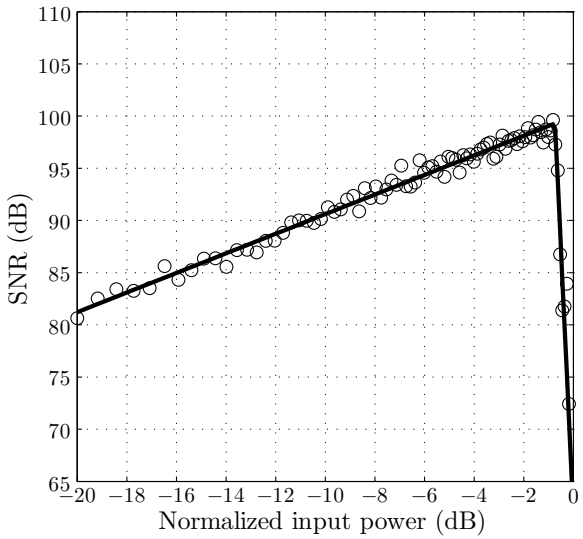


Figure 3.18: SNR as a function on the input power.

Chapter 4

Circuit Design

The present Chapter describes the analog circuits used in the ΣΔ modulator for the AMS technology 018 μm with six metal layers. The standard voltage supply was $V_{DD} = 1.8V$. Moreover, the design was done using standard transistors of the technology and prioritizing the power efficiency over the area. The procedure to obtain the final transistor dimensions was based on simulations, since the equations of the SPICE level 1 are not accurate.

4.1 Introduction to Switched-Capacitor Circuits

The key idea of the switched-capacitor (SC) circuits is placing switches and capacitors instead of resistors. Figure 4.1 shows equivalent circuits that have a current flow from node A to node B. The resistor current is given by $I_{AB} = (V_A - V_B)/R_1$. In the case of Fig. 4.1(b), the capacitor C_s alternates between node A and node B at a clock rate f_s. Thus, the average current is given by the charge moved in one clock period[40]:

$$\overline{I_{AB}} = \frac{C_s\,(V_A - V_B)}{f_s^{-1}} \tag{4.1}$$

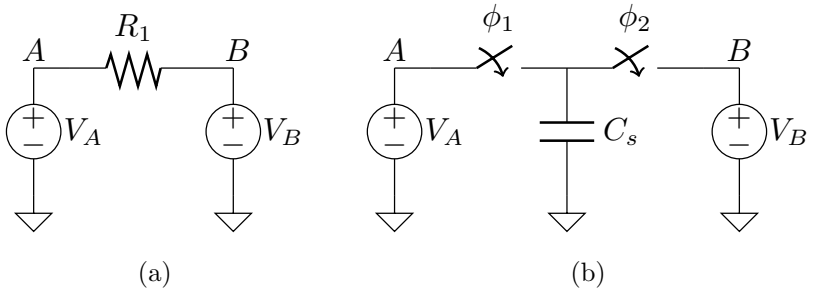


Figure 4.1: (a) Resistor and (b) switched-capacitor resistor.

Comparing both expressions, it can be observed that the scheme of Fig. 4.1(b) emulates a resistance that is given by $(C_s f_s)^{-1}$. One advantage of this kind of circuits is the possibility to implement large resistances values. Note that the switches are implemented using transistors, and its non-idealities degrade the SC circuit performance.

4.1.1 Channel Charge Injection

Let us consider a sampling circuit as shown in Fig. 4.2, where the switch is implemented by a single NMOS transistor. When the switch is *on*, there is a charge present in the inversion layer (called channel charge Q_{ch}) that permits the current flow from V_{in} to the capacitor. When the signal clock (V_{clk}) is down, a certain amount of the channel charge is injected to the capacitor C_s introducing an error in the input signal reading. In [40] this effect and the body effect of the NMOS switch are characterized by the following equation:

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_s}\right) + \gamma\frac{WLC_{ox}}{C_s}\sqrt{2\phi_B + V_{in}} - \frac{WLC_{ox}}{C_s}\left(V_{DD} - V_{TH0} + \gamma\sqrt{2\phi_B}\right). \tag{4.2}$$

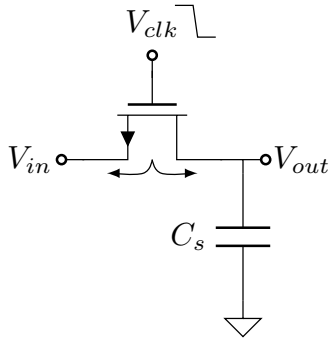


Figure 4.2: Charge injection in a sampling circuit.

4.1.2 Clock Feedthrough

The overlap capacitances (C_{ov}) of the NMOS transistor form paths from the gate to the source and drain (see Fig. 4.3). Thus, the gate transitions are coupled to the output voltage introducing another error source. Assuming a constant overlap capacitance, the voltage error is given by [40]

$$\Delta V = V_{clk}\frac{WC_{ov}}{WC_{ov} + C_s}. \tag{4.3}$$

where W is the transistor width and WC_{ov} is the total overlap capacitance.

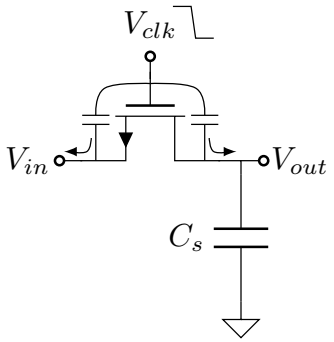


Figure 4.3: Clock feedthrough in a sampling circuit.

4.1.3 kT/C Noise

The noise generated by the *on*-resistance of the switch is sampled in the capacitor C_s and then filtered by the RC equivalent circuit. Thus, the total noise power is obtained by integrating the power spectral density in the whole frequency range as shown in the following expression:

$$P_{n,ktc} = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_s)^2} df = \frac{kT}{C_s}. \tag{4.4}$$

It can be observed that the total power does not depend on the *on*-resistance of the switch. This occurs because as the PSD noise increases, the pole of the RC network decreases resulting in a total power exclusively dependent on the capacitance.

4.2 Integrator

The integrator shown in Fig. 4.4 is a well-known circuit for its insensitivity to the parasitic capacitances of the sampling capacitor (C_s). When $S1$ and $S3$ are closed, the input source charges the capacitor C_s and the parasitic capacitance at node P (C_p). The parasitic capacitance at node Q (C_q) is connected to ground and therefore does not stores any charge. When $S2$ and $S4$ are closed, the charge stored in C_p is discharged to ground and hence does not affect the charge transferred from C_s to C_i. Also, at this phase, the capacitor C_q remains connected to ground since the inputs of the amplifier are in virtual short-circuit.

The clocking scheme of the integrator is shown in Fig. 4.5. It corresponds to a non-inverting integrator with the following transfer function:

$$H(z) = \frac{C_s}{C_i}\frac{z^{-1}}{1-z^{-1}}. \tag{4.5}$$

Note that ϕ_1 and ϕ_2 are the two phases of a non-overlapping clock signal. This assures the correct operation of the SC circuits. Also, it can be observed that the clock signals of the switches $S1$ and $S2$ are delayed from with respect to $S3$ and

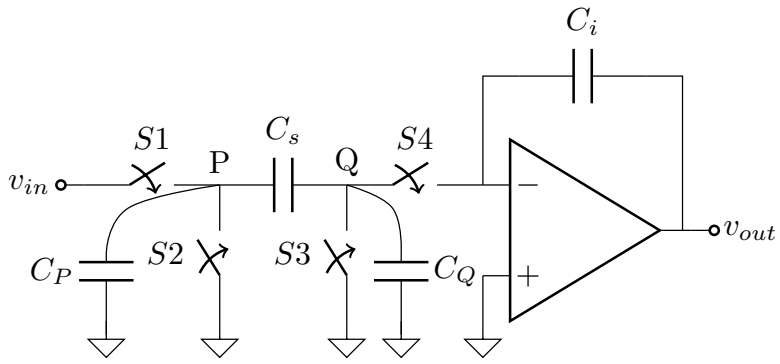


Figure 4.4: Parasitic-insensitive integrator.

$S4$, respectively. This technique is called bottom-plate sampling and is employed to make the charge injection of $S1$ and $S2$ independent of the input signal[41]. The switch $S3$ is opened slightly before $S1$ is, so that a high impedance is sensed through C_s. Thus, the charge injection from $S1$ flows towards the input source. A similar principle is applied to switches $S2$ and $S4$. It is important to note that the switches $S3$ and $S4$ always operate at the same potential and consequently their charge injection is constant.

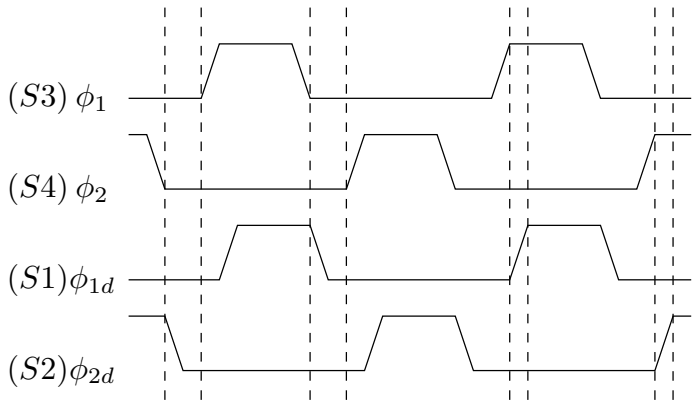


Figure 4.5: Clocking scheme of the integrator.

Therefore, in order to cancel both charge injection and clock feedthrough errors, a differential version of Fig. 4.4 was used (see Fig. 4.6). The bottom plate of the capacitors are connected to the output amplifier or to the input source since this connection reduces the effect of the substrate noise in the circuit operation[41].

The value of the sampling capacitor of the first integrator was specified to $1.5pF$ in Chapter 3. In a differential implementation, this value must be doubled since each path of the integrator generates an independent noise source. Thus, with the coefficient values $a_1 = 0.7$ and $a_2 = 0.4$, the capacitances were calculated as listed in Table 4.1. The dimensions of the unit capacitor (C_u) are $W = 10\mu m$ and $L = 11\mu m$ and its capacitance is $C_u = 0.22pF$.

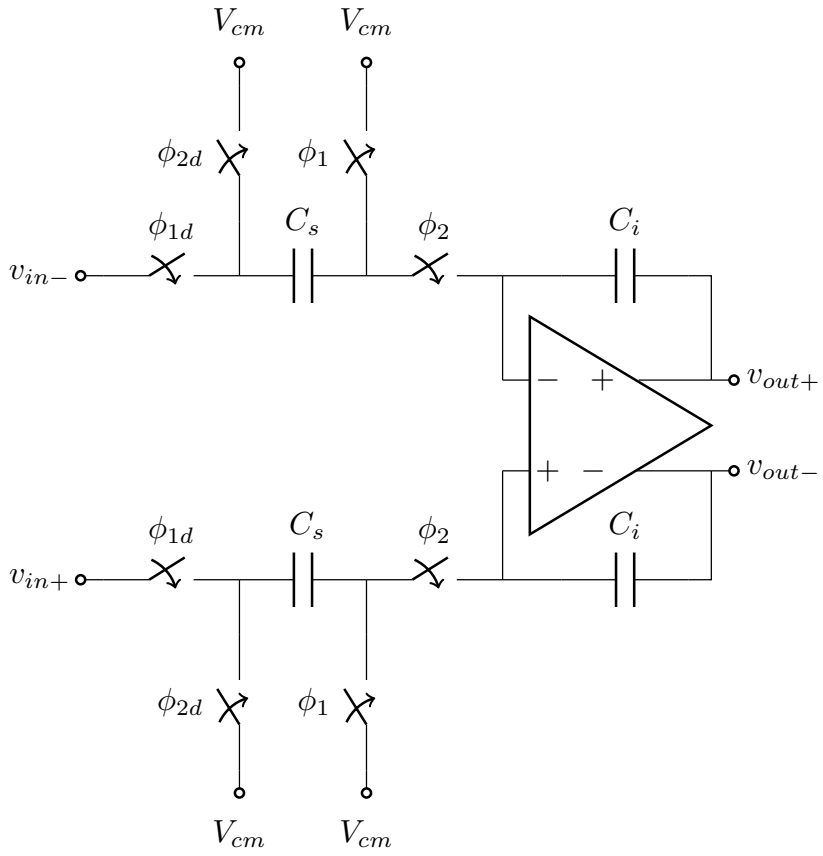


Figure 4.6: Fully differential parasitic-insensitive integrator.

Table 4.1: Integrator capacitance values

Capacitor	**Value**	**Value**$[pF]$
C_{s1}	$14C_u$	3.09
C_{s2}	$4C_u$	0.88
C_{i1}	$20C_u$	4.41
C_{i2}	$10C_u$	2.21

4.3 Switches

The common alternatives for switch implementation are: a NMOS transistor, a PMOS transistor and a transmission gate. The *on*-resistance of single-device implementations depends on the input signal, leading to time-constants that increase for more positive (NMOS) or negative (PMOS) inputs. Another drawback is that their operation is restricted to a given input swing: lower than $V_{DD} - V_{thn}$ for a NMOS transistor and greater than V_{thp} for a PMOS transistor The transmission gate employs NMOS and PMOS transistors using a complementary signal clock as shown in Fig. 4.7. Thus, the *on*-resistance of both devices are connected in parallel, thereby compensating the effect of the input signal[40]. Another advantage of this

topology is that it allows rail-to-rail operation making it appropriate for differential implementations where the operating point of the nodes are at the common mode voltage ($V_{CM} = V_{DD}/2$).

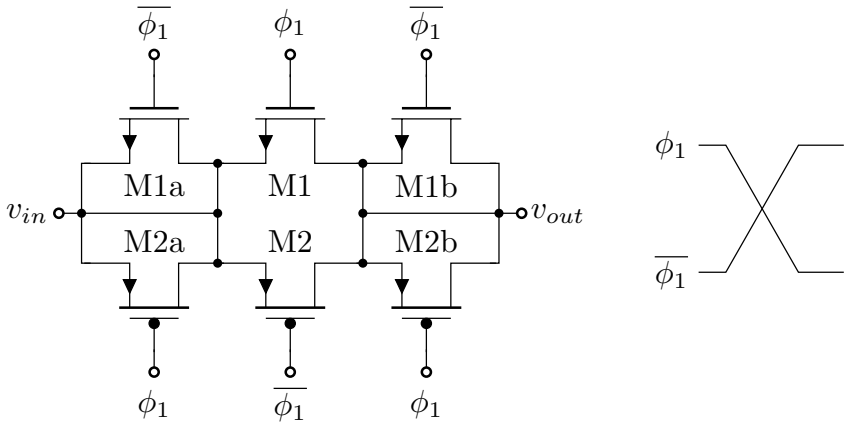


Figure 4.7: Circuit implementation of a switch.

The dimensions of the transistors of the transmission gate implemented in the modulator are listed in Table 4.2. In order to reduce charge injection and clock feedthrough effects, the transistors M1 and M2 must have minimum dimensions as Eqs. (4.2) and (4.3) indicate. Morover, the dimension of M2 must be greater than M1 as well as the ratio between the NMOS (μ_n) and PMOS (μ_p) mobility. This is a rule of thumb that makes the *on*-resistance less dependent of the input voltage. The devices M1a, M1b, M2a and M2b are dummy transistors that reduces charge injection and clock feedthrough. Typically their dimensions are half those of M1 and M2. It is important to noted that both transistors must be turned off simultaneously to avoid any distortion in the sampled value[40].

Table 4.2: Switch transistor dimensions

Device	**W** [μm]	**L** [μm]
M1	1	0.18
M1a	0.5	0.18
M1b	0.5	0.18
M2	3.2	0.18
M2a	1.6	0.18
M2b	1.6	0.18

4.4 Amplifier

The amplifier is the main block of the single-bit modulator. Its specifications define the performance of the integrator and hence of the whole system. An important

characteristic of this analog block (in this application) is that it does not require a high voltage gain, since the modulator is not sensitive to small variations of the coefficients. Typically, a voltage gain greater than 60dB is enough to produce a good performance [2]. The major drawback is that the speed and noise strongly depend on the power consumption, which is critical in low power designs.

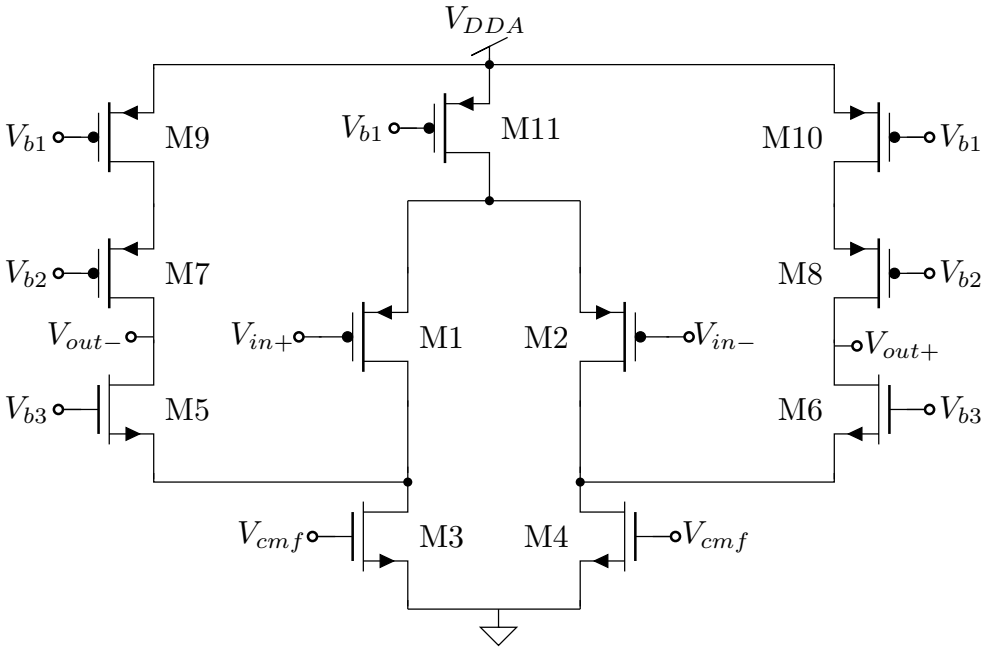


Figure 4.8: Folded cascode OTA.

In SC circuits, the amplifiers are often operational transconductance amplifiers (OTA) because the output signal is a current that charges the load capacitor (C_L). There are many alternatives to implement the OTA, and these can be classified as two-stage and single-stage amplifiers. A classical two-stage amplifier is the miller configuration which commonly needs a class AB stage to enhance its speed[5],[42]. Its drawback is that the compensation capacitors inevitably end up consuming a considerable current. The most common single-stage amplifiers are the current mirror and the folded cascode topologies. The former is more appropriate for applications that require low voltage gain and operates at low voltage supply. Typically the voltage gain is around 50dB which is not desired for discrete-time modulators. Hence, extra techniques are used to improve the amplifier performance [5]. The classical folded cascode topology (see Fig. 4.8) has many advantages, such as the first pole is defined by the output capacitor, high output resistance and high voltage gain. Its main disadvantage is that the SR depends directly on the current of M10-M9. For instance, for SR of $20MV/sec$ and a load capacitance of $2pF$, the current of M9 and M10 is

$$I_{d10} = I_{d9} = C_L SR = 2pF \times 20MV/sec = 40\mu A \tag{4.6}$$

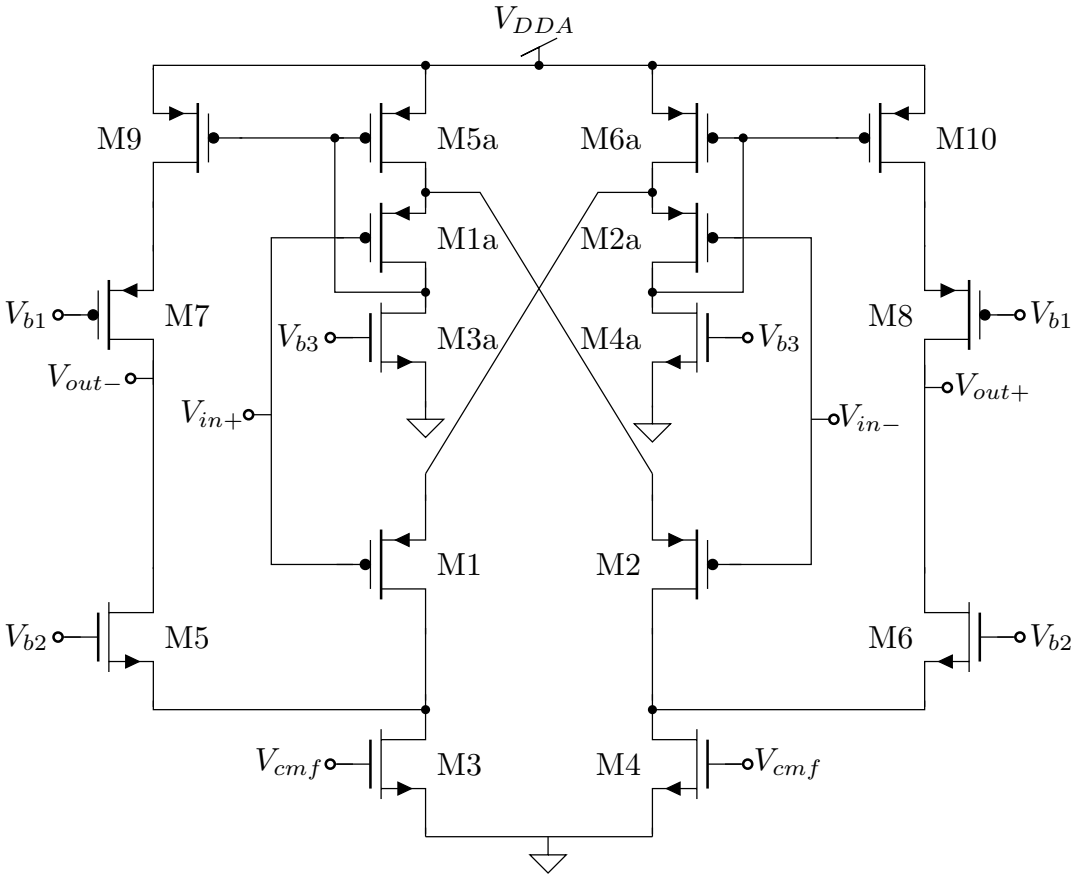


Figure 4.9: Folded cascode OTA with adaptive bias.

By replacing transistor M11 with an adaptive bias circuit[43], the folded cascode OTA improves its power efficiency and operates in class AB. The resulting topology (see Fig. 4.9) is a pseudo differential circuit where transistors M1 and M2 are a cross-coupled differential pair that are biased by two flipped voltage follower (FVF) cells[44]. Hence, for a nonzero differential input signal, the current of M5a or M6a increases, thereby allowing high SR values with a low quiescent current. Also, the current in M5a and M6a are copied to M9 and M10 respectively. The transconductance of the circuit is given by

$$Gm \approx 2gm_1 \tag{4.7}$$

and the GBW is determined by:

$$GBW = \frac{Gm}{2\pi C_L} \tag{4.8}$$

From the equations, it can be observed that the folded cascode OTA and its adap-

tive bias version consume the same current for a given GBW. Another important parameter of the amplifier is its equivalent input noise power. The noise power generated by the adaptive bias circuit is determined by

$$\overline{V_{n,IN}^2}\Big|_{FVF} = 2\frac{\overline{I_{n,M5a}^2} + \overline{I_{n,M1a}^2} + \overline{I_{n,M3a}^2}}{gm_{FVF}} \tag{4.9}$$

where $gm_{FVF} = gm_{1a}gm_{5a}rds_{1a}$. Furthermore, the noise power generated by the folded cascode is given by:

$$\overline{V_{n,IN}^2}\Big|_{FC} = 2\frac{\overline{I_{n,M1}^2} + \overline{I_{n,M3}^2} + \overline{I_{n,M9}^2}}{Gm} \tag{4.10}$$

By superposition, the input equivalent noise power is

$$\overline{V_{n,IN}^2} = \overline{V_{n,IN}^2}\Big|_{FVF} + \overline{V_{n,IN}^2}\Big|_{FC} \tag{4.11}$$

The equations derived above were used as a criteria to calculate the dimensions of the OTA transistors. The final values were set by simulations and are listed in Table 4.3. The design accomplished the requirements mentioned in Table 3.3 for each corner of the technology, which considers process(corner models), temperature(industrial range) and voltage($\pm 5\% V_{DD}$) variation. Furthermore, the power consumption and the noise power were the main concern of the design. In order to assure the OTA stability, the minimum OTA load capacitance must be $2.5pF$.

Table 4.3: OTA transistor dimensions

Device	**W** [μm]	**L** [μm]	**M**	**W**$_{tot}$ [μm]
M1	10	1	10	100
M2	10	1	10	100
M3	23	1.5	15	345
M4	23	1.5	15	345
M5	10	1	20	200
M6	10	1	20	200
M7	10	1	20	200
M8	10	1	20	200
M9	4.5	1.5	5	22.5
M10	4.5	1.5	5	22.5
M1a	10	1	10	100
M2a	10	1	10	100
M3a	15	2.5	3	45
M4a	15	2.5	3	45
M5a	4.5	1.5	5	22.5
M6a	4.5	1.5	5	22.5

4.4.1 Bias Circuit

The OTA bias circuit is shown in Fig. 4.10 and the transistor dimensions are listed in Table 4.4[1]. Power consumption was the primary concern in the design of this circuit. The reference current has a low value of $I_{REF} = 100nA$, that was copied to establish the bias voltages V_{b1}, V_{b2}, V_{b3} and V_{cmfi}.

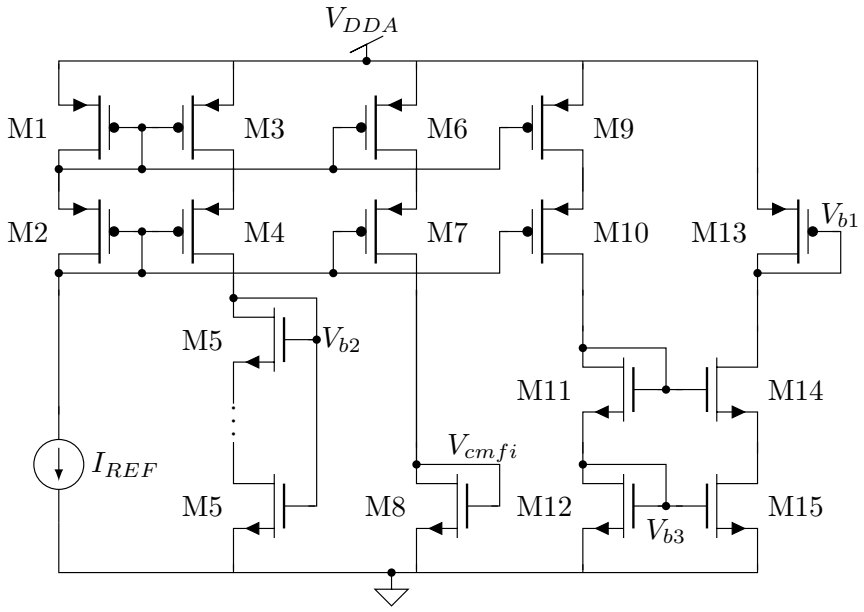


Figure 4.10: Bias circuit of the OTA.

Table 4.4: Transistor dimensions of the OTA bias circuit

Device	**W** [μm]	**L** [μm]	M	$\mathbf{W}_{tot}$ [μm]	$\mathbf{I}_D$ [μA]
M1	10	1	1	10	0.1
M2	10	1	1	10	0.1
M3	10	1	1	10	0.1
M4	10	1	1	10	0.1
M5	1	10	5	0.2	0.1
M6	10	1	5	50	0.5
M7	10	1	5	50	0.5
M8	23	1.5	1	23	0.5
M9	10	1	5	50	0.5
M10	10	1	5	50	0.5
M11	10	1	1	10	0.5
M12	15	2.5	1	15	0.5
M13	1	4	1	1	0.5
M14	10	1	3	30	0.5
M15	15	2.5	1	15	0.5

[1]Only in the case of M5, the parameter M means a series connection as indicated in Fig. 4.10. In other cases this parameter indicates parallel connection

4.4.2 Common Mode feedback block

The common mode feedback block is shown in Fig. 4.11 and the capacitance values for the first (INT1) and second (INT2) integrators are listed in Table 4.5. These values were determined by simulation such to assure the stability of the common mode. It was noted a correlation between the C_{c2} capacitor and the input noise power. As well as this capacitance increases, the input noise power decreases.

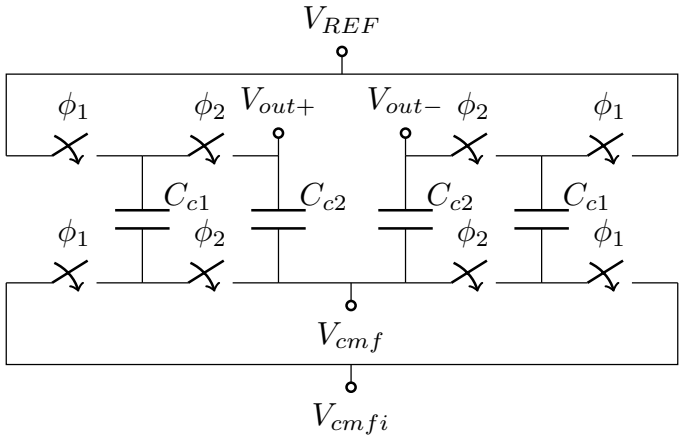


Figure 4.11: Common mode feedback block.

Table 4.5: CMFB capacitance values

	INT1		**INT2**	
Capacitor	**Value**	**Value [pF]**	**Value**	**Value [pF]**
C_{c1}	$7C_u$	1.54	$3C_u$	0.66
C_{c2}	$5C_u$	1.10	$10C_u$	2.21

4.5 Quantizer

Since the $\Sigma\Delta$ modulator suppresses the non-idealities such as the offset of the the 1-bit quantizer, the requirements of this block are relaxed and the power consumption can be optimized. A power efficient topology is shown in Fig. 4.12, which consists of a dynamic comparator and a SR latch[5]. This circuit is purely dynamic and consumes power only at the rising edge of the clock (Clk).

The dynamic comparator consists of transistors M1, M2, M3, M4, M5, M6, M7a(b) and M8a(b). When the signal Clk is low, transistors M3 and M4 are off and the nodes P and Q are clamped to V_{DD}. At the rising of the clock, the parasitic capacitances of the nodes P (C_p) and Q (C_q) are discharged through transistors M1

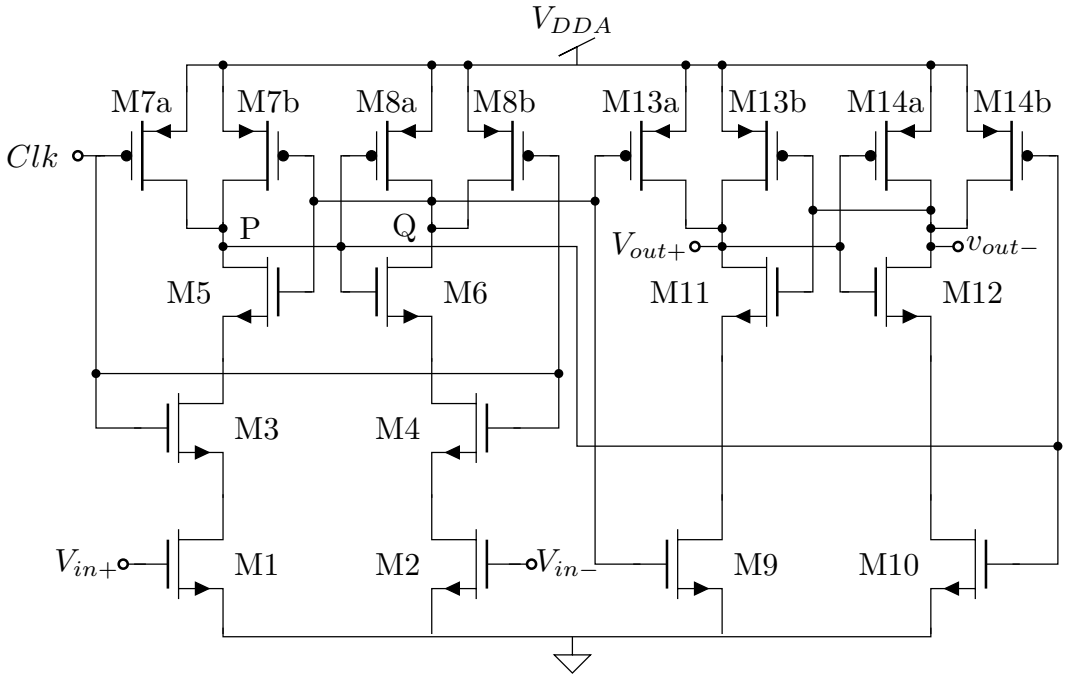


Figure 4.12: Quantizer circuit: clocked comparator and latch.

Table 4.6: Transistor dimensions of 1-bit quantizer

Device	**W** $[\mu m]$	**L** $[\mu m]$	**M**	$\mathbf{W}_{tot}$ $[\mu m]$
M1	1	1	1	1
M2	1	1	1	1
M3	0.5	0.18	1	0.5
M4	0.5	0.18	1	0.5
M5	0.5	0.18	1	0.5
M6	0.5	0.18	1	0.5
M7a	0.5	0.18	2	1
M7b	0.5	0.18	2	1
M8a	0.5	0.18	2	1
M8b	0.5	0.18	2	1
M9	0.5	0.18	1	0.5
M10	0.5	0.18	1	0.5
M11	0.5	0.18	1	0.5
M12	0.5	0.18	1	0.5
M13a	0.5	0.18	2	1
M13b	0.5	0.18	2	1
M14a	0.5	0.18	2	1
M14b	0.5	0.18	2	1

and M2 at the rate of its drain value. For instance, if V_{in+} is greater than V_{in-}, the drain of M2 is greater and the parisitic capacitance C_q discharges faster than C_p. The crosscoupled inverter (M5, M7b, M8b and M6) regenerates the signal and the values at node P and Q are set to ground and V_{DD}, respectively. These values are

stored in the latch (M9, M10, M11, M12, M13a, M13b, M14a, M14b) until the next rising clock.

Note that the circuit has a purely digital behavior with exception of transistors M1 and M2 that amplify the input signal. Hence, the devices that operate as a switch have minimum dimensions. Transistors M1 and M2 have a larger length (L=1μm) to avoid mismatch effects in the comparison operation. Table 4.6 lists the complete transistor dimensions.

4.6 DAC

The 1-bit DAC is a simple circuit that consist of two switches controlled by one digital signal as shown in Fig. 4.13. When the input assumes logic value '1', the output is connected to the reference voltage; otherwise the output is connected to ground. In a differential implementation, the reference voltage must be centered at the analog ground (V_{CM}). Hence, two reference voltages (see Table 4.7) that are symmetric with respect to V_{CM} must be implemented such that the difference between the two is V_{REF}.

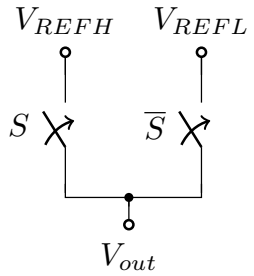


Figure 4.13: 1-bit DAC.

Table 4.7: DAC reference voltages

Reference Voltage	**Value [V]**
V_{REFH}	1.4
V_{REFL}	0.4

4.7 Feed-forward Coefficients

The circuit shown in Fig. 4.14 shows the switched-capacitor implementation of the feed-forward coefficients and the adder. The output is[5]

$$V_{out} = \frac{\sum_{j=0}^{2} V_{Ij} C_{fj}}{\sum_{j=0}^{2} C_{fj}} \tag{4.12}$$

where C_{fj} is the capacitance of the j-th feed-forward path. The output can be written in terms of a unitary capacitance (C_u) as

$$V_{out} = \frac{\sum_{j=0}^{2} V_{Ij} c_j C_u}{\sum_{j=0}^{2} c_j C_u} = \frac{\sum_{j=0}^{2} V_{Ij} c_j}{\sum_{j=0}^{2} c_j} \tag{4.13}$$

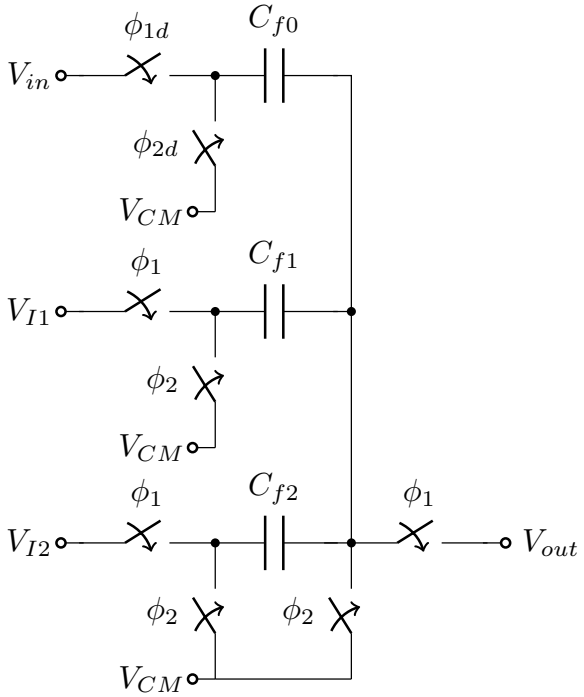


Figure 4.14: Feed-forward circuit.

Therefore, the output voltage is the sum of the inputs weighted by the feed-forward coefficients but attenuated by a constant value that is the sum of all the coefficients. Since the modulator is a single bit architecture, the only relevant information is in the sign and hence the attenuation does not affect the modulator operation. Table 4.8 lists the capacitance values.

4.8 Non-overlapping clock

The clock generator is shown in Fig. 4.15. It is a classical two-phase non-overlapping circuit. The dead-time between ϕ_1 and ϕ_2 is the sum of t_{d1} and t_{d2}. The logic gates

Table 4.8: Capacitance values of the feed-forward circuit

Capacitor	**Value**	**Value** $[pF]$
C_{f0}	$6C_u$	1.32
C_{f1}	$6C_u$	1.32
C_{f2}	$6C_u$	1.32

were implemented using minimum dimensions (L=0.18μm and W=0.5μm) and the widths of the PMOS devices are 3-fold those of the NMOS ones.

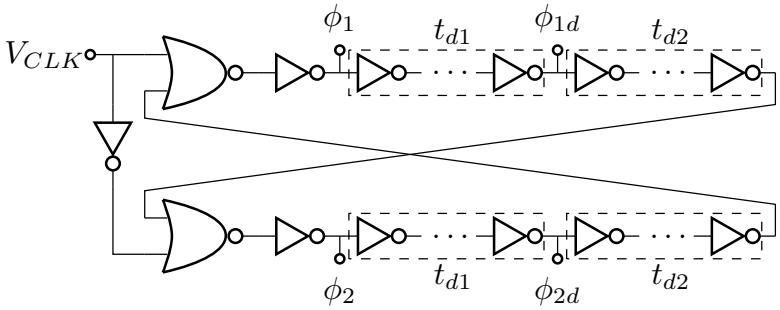


Figure 4.15: Non-overlapping clock generation.

Since the switches are transmission gates, each phase needs a complementary signal for proper operation. Hence, the circuit shown in 4.16 was placed at each phase of the non-overlapping clock (ϕ_1, ϕ_2, ϕ_{1d} and ϕ_{2d}) to generate its complementary signal ($\overline{\phi_1}$, $\overline{\phi_2}$, $\overline{\phi_{1d}}$ and $\overline{\phi_2 d}$). The dummy devices (NMOS and PMOS) have the same dimensions as those of the transistors of the inverter since they duplicate the delay of the inverter cell[40].

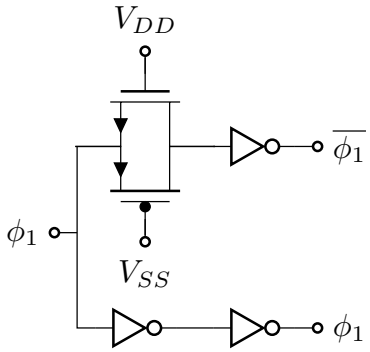


Figure 4.16: Generation of the complementary signals for the switches.

4.9 Modulator

The entire modulator circuit is shown in Fig. 4.17.

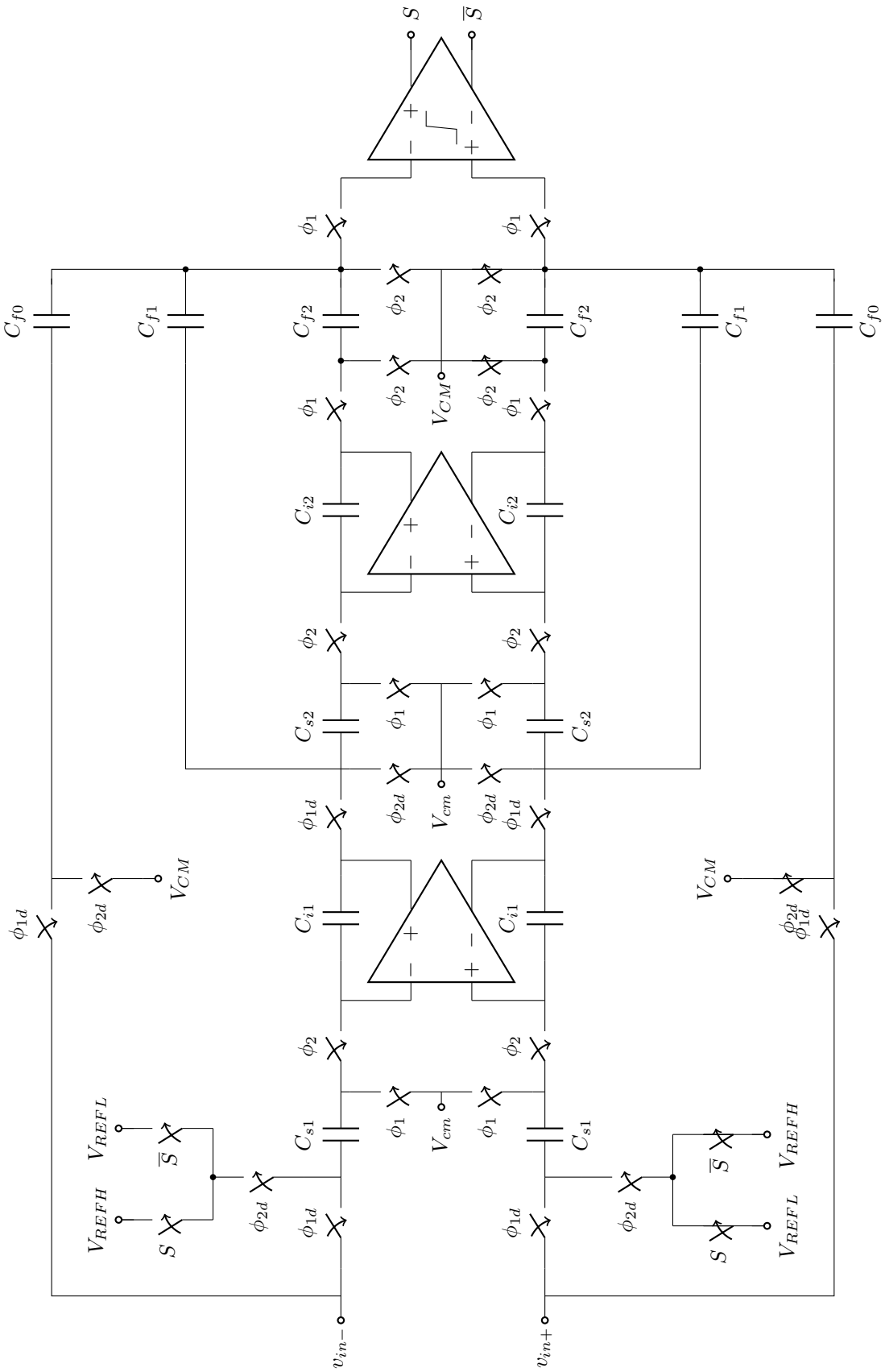


Figure 4.17: Circuit implementation of the entire modulator.

Chapter 5

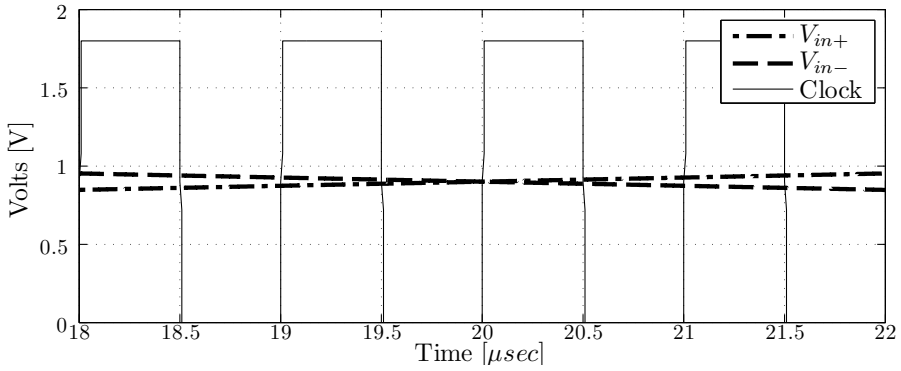
Simulations and Results

The analog blocks were simulated using the simulators spectre and spectreRF from CADENCE. In case of transient analysis, the simulator APS (Advanced Parallel Simulator) was used since it accelerates the simulation time.

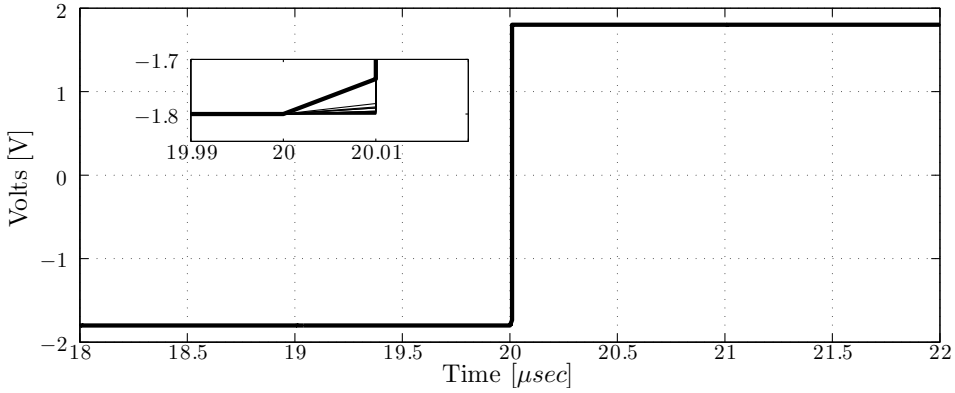
The operation of the modulator and the functionality of the analog blocks were validated using three types of simulations: Nominal, Process-Voltage-Temperature (PVT) and Monte Carlo. The former consists on classical simulation of the typical transistor model at room temperature and standard voltage supply. The PVT simulations are the combinations of the corner models of the process: maximum, nominal and minimum temperature; and maximum, nominal and minimum voltage supply. The latter consists on performing many simulations based on the statistical model of the transistor. The design kit provides the corner models of the transistor, which are *worst to zero* (*wz*), *worst to one*(*wo*), *worst power*(*wp*) and *worst speed*(*ws*). The range of temperatures are according to the industrial standard (-40° to 85°) and the maximum allowable variation of V_{DD} was 5%.

5.1 Quantizer

The quantizer was simulated using three entries: V_{in+}, V_{in-} and V_{clk} (see Fig. 5.1(a)). The positive and negative input voltages are signals that vary from ground to V_{DD} and from V_{DD} to ground, respectively. The output is only updated at the rising edge of the clock (V_{clk}), as shown in Fig. 5.1(b) where it can be observed that the typical responses at 27°C and 40°C do not have a significant variation. Also, in Fig. 5.1(b) is depicted the output voltage for every combination of the corner models and temperature(-40°C, 27°C, 40°C and 85°C). The simulation regarding the corner model *wz* at 85°C was the only one that presents a slight difference (see the thickest curve in 5.1(b)). Nevertheless, this does not compromise the modulator operation. Monte Carlo simulations were not performed since the offset of the comparator is canceled out by the system loop.



(a) Input Signals: V_{in+}, V_{in-} and V_{clk}



(b) Differential Output

Figure 5.1: Input/Output signals of the quantizer.

5.2 Non-overlapping clock

The output signals are shown in Fig. 5.2. The dead-time is about 1 *nsec* between ϕ_1 and ϕ_2 and 500 *psec* between ϕ_1 and ϕ_{2d}. It is important to note that the inherent behavior of this circuit assures that the delays are always present even when experiencing mismatch effects and process variations.

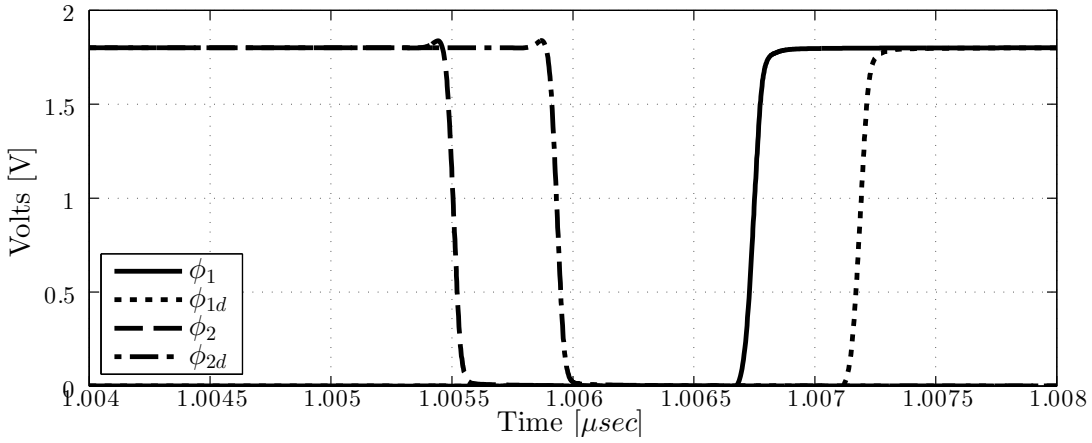


Figure 5.2: Clock phases.

5.3 OTA

The results of the simulation of this analog block are based on the requirements set in Table 3.3. The frequency, noise and time response were validated with PVT and Monte Carlo simulations.

5.3.1 Nominal simulation

The frequency response of the OTA is shown in Fig. 5.3. It can be observed that the OTA possesses a high DC gain ($A_{DC} = 90.29$dB), a unity gain frequency (UGF) of 6.8MHz and a phase margin of 54.59°. The GBW of this circuit (7.8MHz) is a little larger than the UGF since this circuit is not an ideal one-pole system. Additionally, the power consumption including the bias circuit was around $30\mu W$.

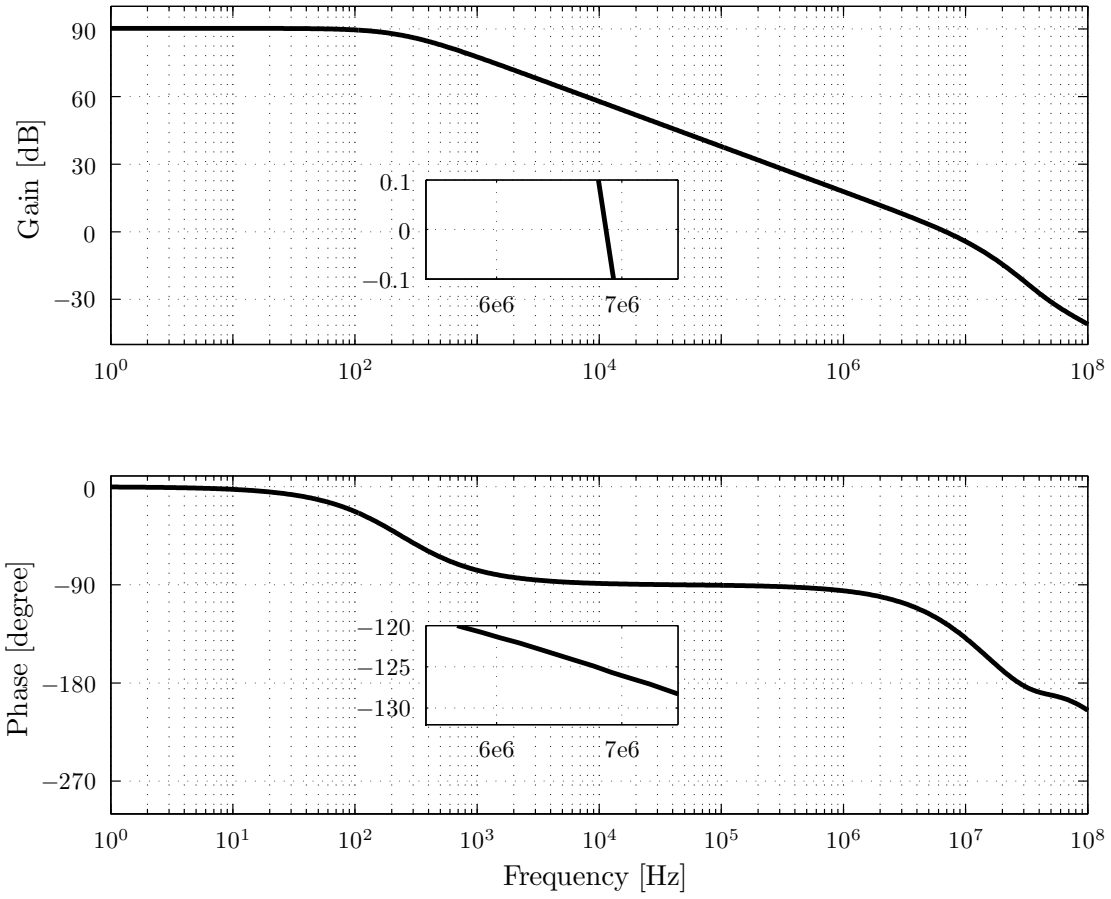


Figure 5.3: Nominal frequency response of the OTA.

The PSD of the equivalent input noise is shown in Fig. 5.4. It can be noted that in the signal-band, the flicker noise is larger than the thermal component, as expected. The equivalent RMS input noise voltage was around $4V_{rms}$, and the contribution of the flicker noise is 94% of the total value. As expected, the transistors M3, M4, M9 and M10 are the ones that generate more noise, that is almost 60% of

the total noise. Furthermore, the differential pair (M1 and M2) and transistor M3a and M4a (from the adaptive bias circuit) contribute with 18% and 16%, respectively.

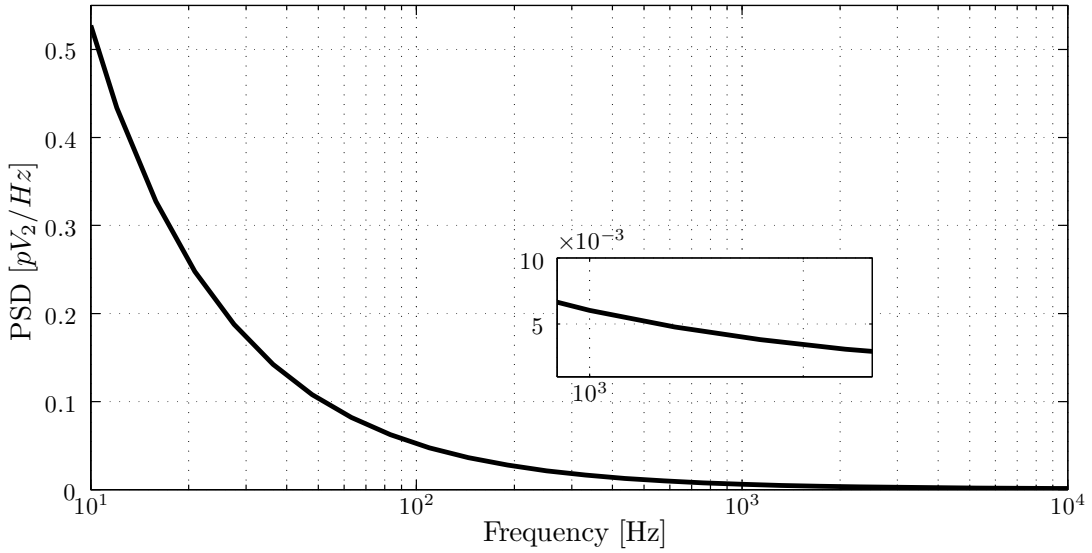


Figure 5.4: Nominal PSD of the equivalent input noise of the OTA.

The step response of the amplifier is depicted in Fig. 5.5. The maximum and minimum output voltages are almost V_{DD} and $-V_{DD}$ since the transistors M3, M4, M9 and M10 operates at weak inversion. The settling time of the circuit is in close agreement with the GBW shown above, because the large signal response takes into account other effects of the amplifier. However, this settling time value is not critical since the output attains its steady value within the integration time ($500nsec$).

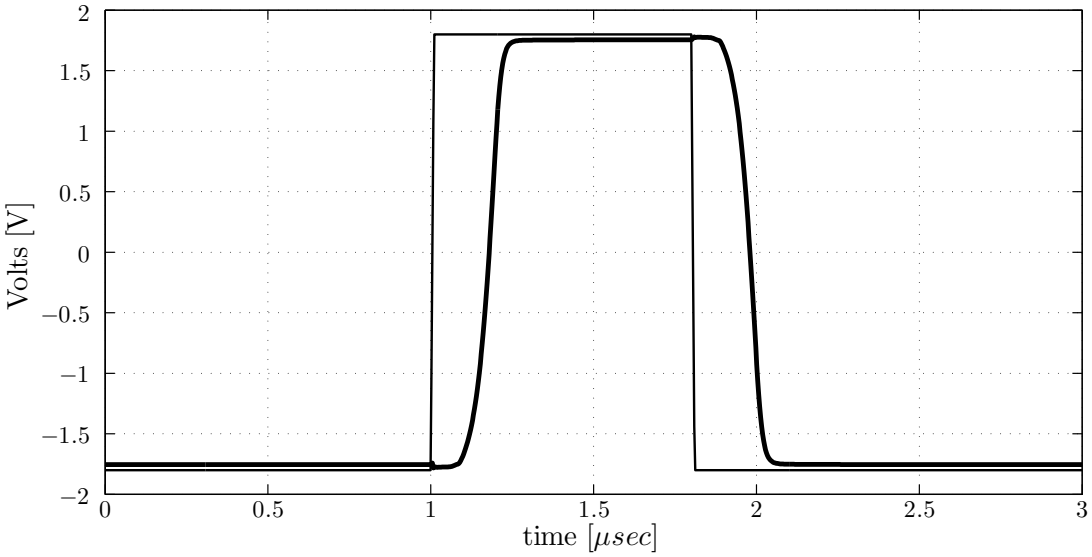


Figure 5.5: Step response.

The main results of the nominal simulations are summarize in Table 5.1. It can be observed that the circuit reaches the requirements set in Chapter 3. The

exception is the settling time which, as mentioned above, is not a critical value.

Table 5.1: Nominal results of the OTA

Specification	Values
GBW	7.8 MHz
DC Gain	90.29 dB
Phase Margin	54.59°
RMS input noise voltage	$4.46\mu V_{RMS}$
Power	$30.4\mu W$
Positive SR	31.8MV/sec
Negative SR	31.7MV/sec
Settling time	$242nsec$
Maximum output voltage	V_{DD}-45.7mV
Minimum output voltage	-(V_{DD}-46mV)

5.3.2 PVT simulation

Table 5.2 summarizes the maximum and minimum values of the OTA parameters considering PVT variations. It can be seen that the results satisfy the requirements of the amplifier.

Table 5.2: PVT results of the OTA

Specification	Mininum		Maximum	
	Corner	**Value**	**Corner**	**Value**
GBW	Corner 1	5.75 MHz	Corner 2	12.1 MHz
Phase Margin	Corner 2	40.02°	Corner 3	66.84°
RMS input noise voltage	Corner 4	$3.72\mu V_{RMS}$	Corner 1	$5.81\mu V_{RMS}$
Power	Corner 5	26.8 μW	Corner 1	$68.6\mu W$
Positive SR	Corner 6	25.5 MV/sec	Corner 7	39.1 MV/sec
Settling time	Corner 8	216 nsec	Corner 9	267nsec

The most critical environment is the called **corner 1** where the amplifier attains minimum GBW and maximum RMS input noise voltage. However, the RMS input noise voltage is lower than the maximum allowed value to reach the specified SNR, and the GBW value is higher than the minimum required to assure a complete charge transfer. Furthermore, this environment presents the worst power consumption which is more than twice that of the nominal value. The environment of **corner 2** achieves the minimum phase margin. Nevertheless, a phase margin of 40° still assures the stability of the amplifier. In case of **corner 9**, the settling time is slightly greater than half of the integration time. This can be critical since it affects directly

the integrator charge transfer. Table 5.3 lists the conditions of the environments mentioned in Table 5.2.

Table 5.3: Corners of the OTA

Corners	Transistor Model	Temperature	Supply Voltage
Corner 1	*wp*	85°	1.89 V
Corner 2	*wo*	-40°	1.89 V
Corner 3	*wo*	85°	1.89 V
Corner 4	*wp*	-40°	1.89 V
Corner 5	*ws*	-40°	1.71 V
Corner 6	*wo*	85°	1.71 V
Corner 7	*wz*	-40°	1.89 V
Corner 8	*wp*	-40°	1.89 V
Corner 9	*ws*	85°	1.71 V

Figure 5.6 illustrates the plots of the best and worst frequency responses. The lowest value of UGF (3.5MHz) occurs in **corner 1** but it still satisfies the requirement of Table 3.3.

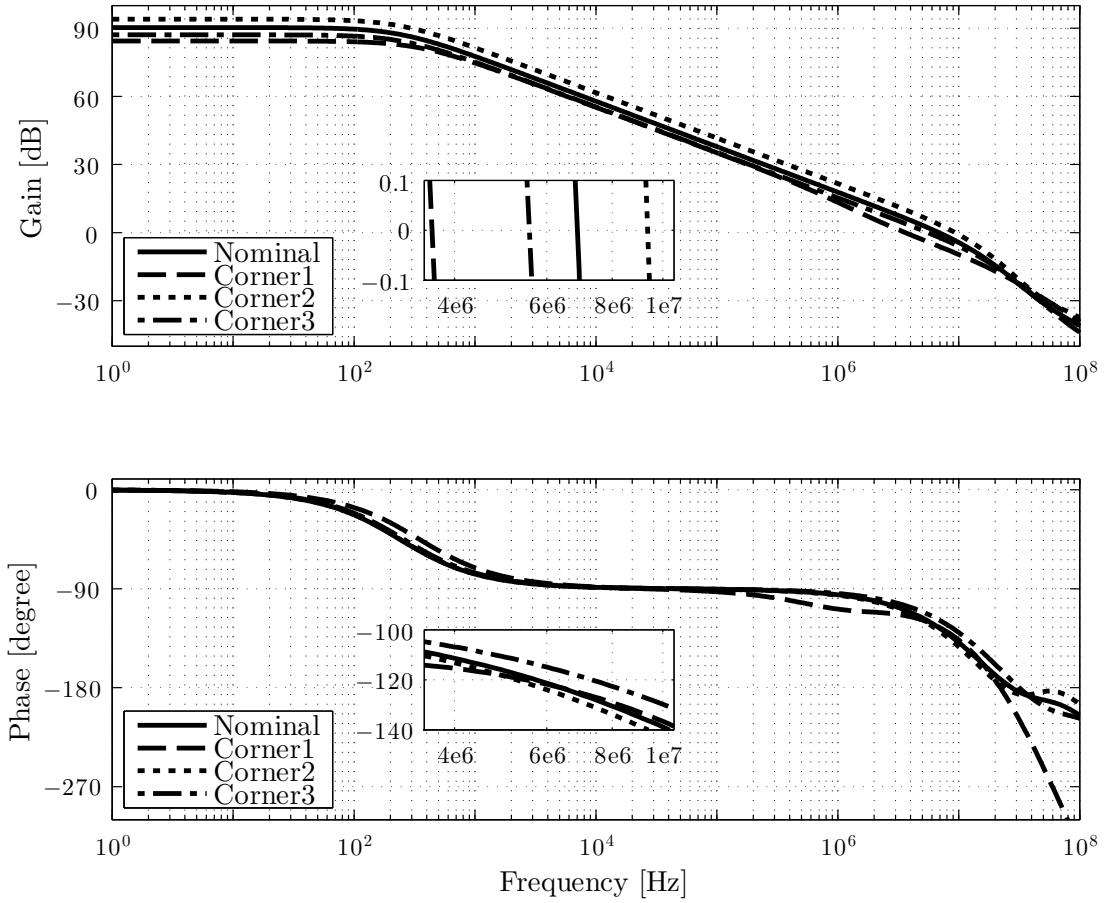


Figure 5.6: Corner simulations of the OTA frequency response.

The PSD of the input noise is depicted in Fig. 5.7. It can be observed that

for the conditions of **corner 1**, the noise has a significant increment. However, the input noise RMS voltage still remains lower than $6\mu V_{RMS}$ which is the limit to assure 16 bits.

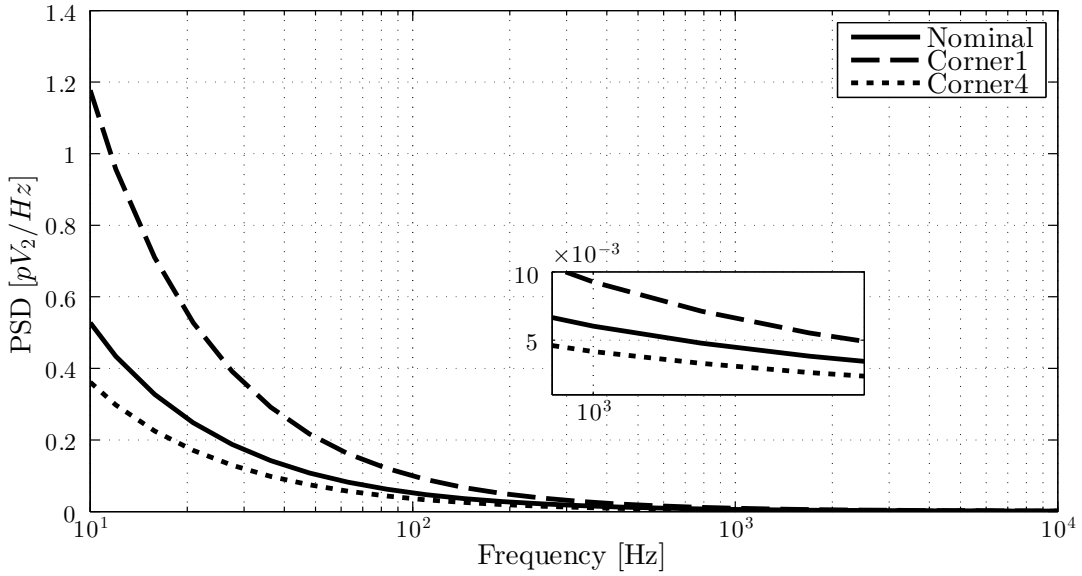


Figure 5.7: Corner simulations of the PSD of the OTA equivalent input noise.

Figure 5.8 illustrates the step response of the OTA for the most critical conditions of the transient parameters. The output for the simulations of **corner 8** has maximum and minimum values greater than the rails, which can cause device degradation. Nevertheless, as predicted by the system-level simulations, the output of the first integrator ranges between -1.4 V to 1.4 V.

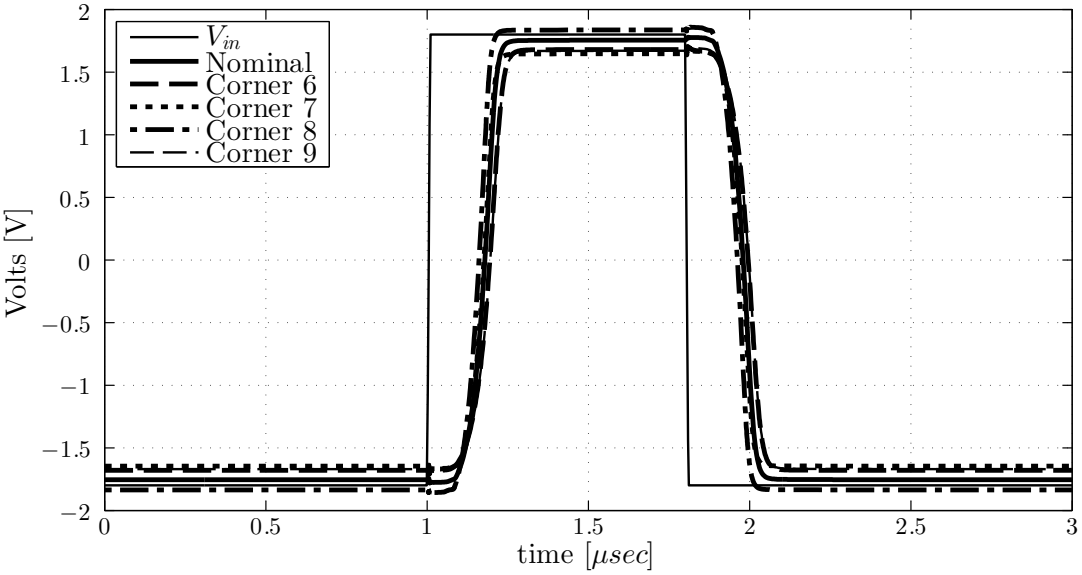


Figure 5.8: Corner simulations of the OTA step response.

5.3.3 Montecarlo Simulations

Monte Carlo simulations were performed for 500 samples at 27°C. The histograms of the main parameters of the OTA are shown in Fig. 5.9.

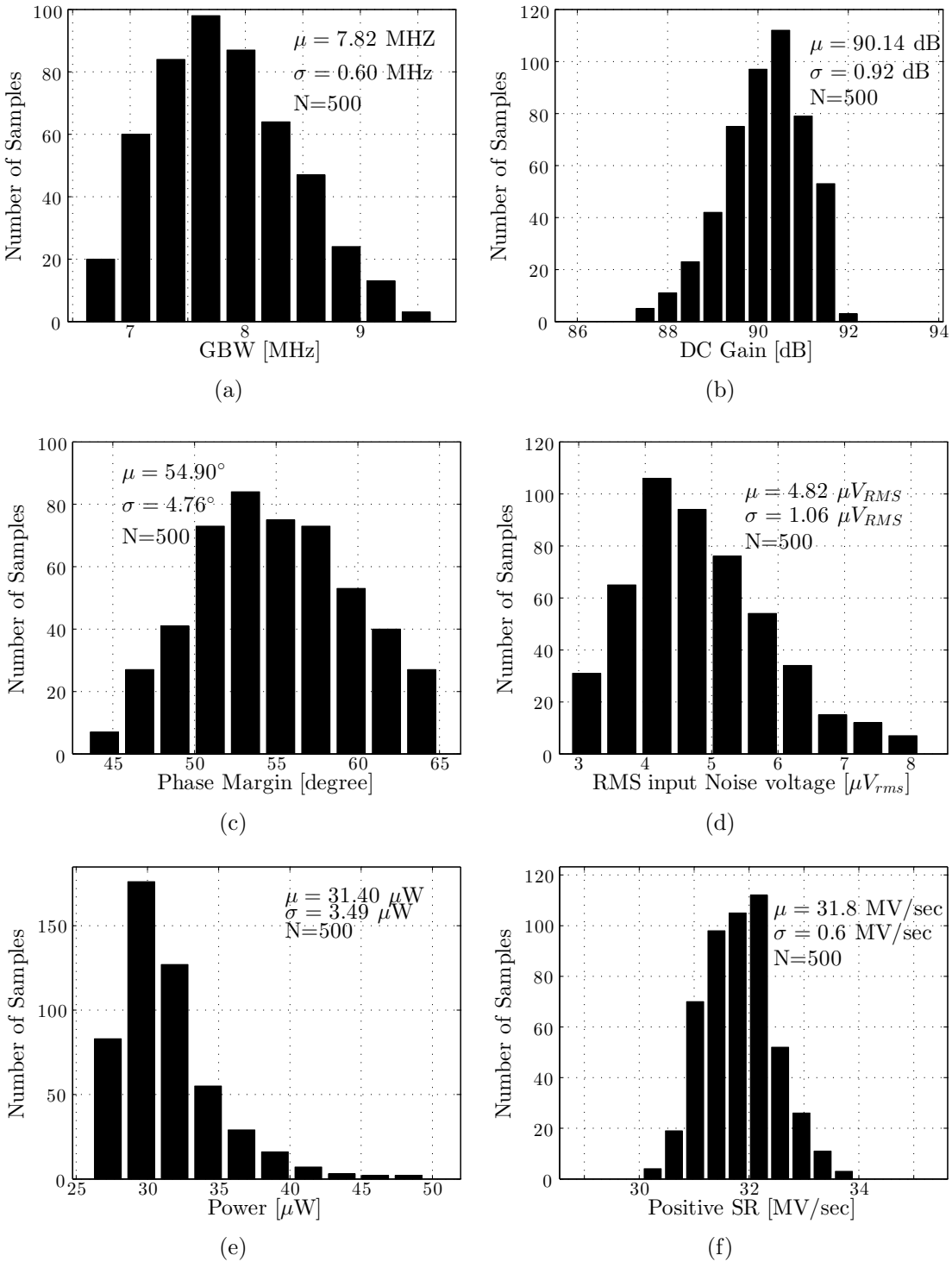
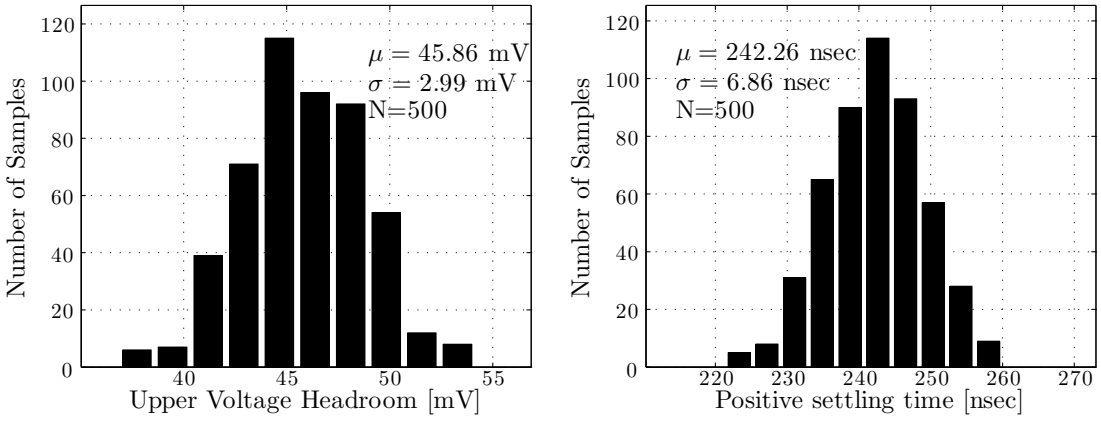


Figure 5.9: Histograms of the GBW, DC gain, phase margin, input noise RMS voltage, power and SR.

Figure 5.10 illustrates the histograms of the upper headroom voltage and settling

time values. It is worth mentioning that the histogram of lower headroom voltage values is equal to that of the upper voltage headroom.



(a) (b)

Figure 5.10: Histograms of the upper headroom voltage and settling time.

The main results of the Monte Carlo simulations are summarized in Table 5.4. The most critical parameters are the input noise RMS voltage and the power consumption. The former only assures that 95% (2σ) of the samples accomplished the specification set in Table 3.3. The latter has a strong sensitivity to mismatch and process variations effects, which may lead a power consumption of $50\mu W$ at maximum current (considering 2σ).

Table 5.4: Statistical results of the Monte Carlo simulations of the OTA

Parameter	**Mean**	σ	**3**σ
GBW	7.82 MHz	0.6 MHz	1.8MHz
DC Gain	90.14 dB	0.92 dB	2.76 dB
Phase Margin	54.9°	4.76°	14.28°
RMS input noise voltage	4.82 μV_{RMS}	1.06 μV_{RMS}	3.2 μV_{RMS}
Power	31.4 μW	3.49 μW	10.5 μW
SR	31.8 MV/sec	0.6 MV/sec	1.8 MV/sec
Upper voltage headroom	45.86 mV	3 mV	9 mV
Settling time	242.26 nsec	6.86 nsec	20.58 nsec

5.4 Modulator

The circuit simulation of the modulator takes too much time which makes it impractical Monte Carlo simulations of the entire circuit. Hence the response of the modulator was validated using nominal and PVT simulations. Since the performance of the modulator depends directly on the OTA behavior, the modulator was simulated using the conditions given in Table 5.3.

5.4.1 Noiseless simulations

The modulator was simulated using a classical transient analysis which does not consider the devices noise. The PSD of the output signal is shown in Fig. 5.11. The response reaches 103.9dB of SQNR where the only noise source was that produced by the quantizer.

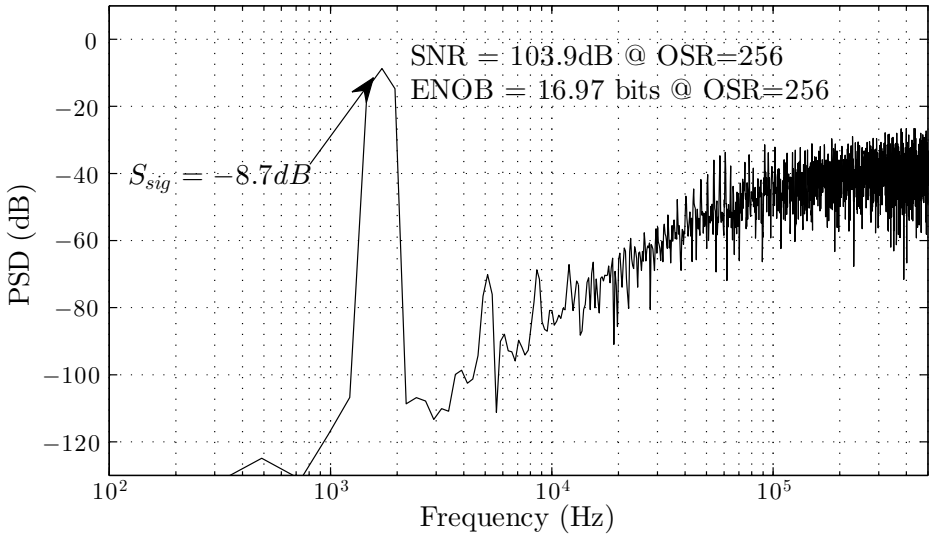


Figure 5.11: Nominal PSD of the modulator output.

Table 5.5 lists the quantization noise power values for each PVT simulation (see Table 5.3). It can be observed that in almost all the cases more than 17 bits were achieved, with the exception of **corner 5**, which is the environment that corresponds to the lowest power consumption of the OTA.

Table 5.5: Results of the PVT simulations of the noiseless modulator.

Simulation	**SNR [dB]**	**ENOB [bits]**	$\mathbf{P_{n,q,out}}$ **[dB]**	$\mathbf{P_{n,q,out}}$ **[pV^2]**
Typical 27C	103.9	17.0	-102.72	53.46
Corner 1	109.3	17.9	-108.12	15.42
Corner 2	107	17.5	-105.82	26.18
Corner 3	109.3	17.9	-108.12	15.42
Corner 4	104.1	17.0	-102.92	51.05
Corner 5	101	16.5	-99.82	104.23
Corner 6	104.5	17.1	-103.32	46.56
Corner 7	106.2	17.4	-105.02	31.48
Corner 8	104.5	17.1	-103.32	46.56
Corner 9	108.3	17.7	-107.12	19.41

5.4.2 Noise simulation using SpectreRF

In order to estimate the total output noise generated by the devices, the modulator was simulated using the scheme proposed in [45]. Since the OTA is the highest noise source of the circuit, the output noise of the modulator was measured using the conditions listed in Table 5.3. The simulations of **corners 1, 3 and 9** are the the ones that have more output noise and are depicted in Fig. 5.12.

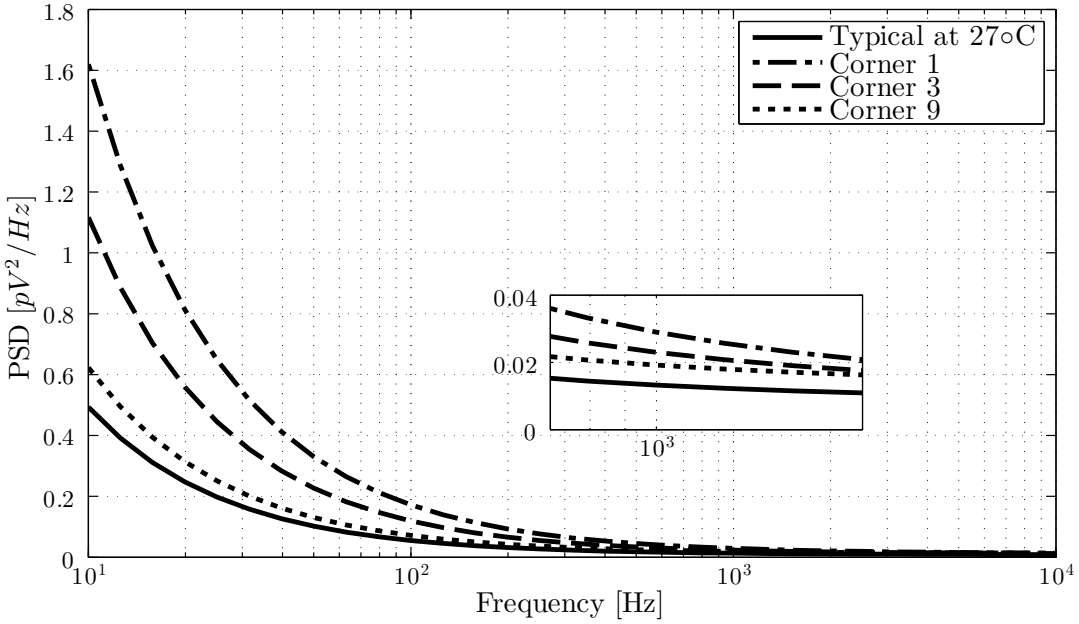


Figure 5.12: PVT simulation of the PSD of the modulator.

The results of the PVT simulations are listed in Table 5.6, where $P_{n,dev,out}$, $P_{n,q,out}$ and $P_{n,out}$ are the noise powers at the output of the devices, the quantizer and the modulator, respectively. It can be seen that in each case, the SNR surpasses the 99dB which assures an ENOB 16 bits.

Table 5.6: Results of the PVT simulations of the noisy modulator.

Simulation	$\mathbf{P_{n,dev,out}[pV^2]}$	$\mathbf{P_{n,q,out}[pV^2]}$	$\mathbf{P_{n,out}[pV^2]}$	**SNR**	**ENOB**
Typical 27C	32.36	53.46	-100.66	101.84	16.6
Corner 1	84.66	15.41	-100.00	101.18	16.5
Corner 2	27.79	26.18	-102.68	103.86	17.0
Corner 3	63.75	15.42	-101.01	102.19	16.7
Corner 4	26.74	51.05	-101.09	102.27	16.7
Corner 5	29.29	104.23	-98.74	99.92	16.3
Corner 6	45.05	46.56	-100.38	101.56	16.6
Corner 7	25.89	31.48	-102.41	103.59	16.9
Corner 8	26.74	46.56	-101.35	102.53	16.7
Corner 9	47.67	19.41	-101.73	102.91	16.8

5.4.3 Noise simulation using transient noise

The modulator was simulated using the *transient noise* feature of the simulator. The PSD of the output signal is shown in Fig. 5.13. It can be appreciated that the results agree with the value shown in Table 5.6. This simulation was performed to demonstrate that similar results were obtained by two different methods. The PVT simulations were not performed since the *transient noise* simulation takes very long times.

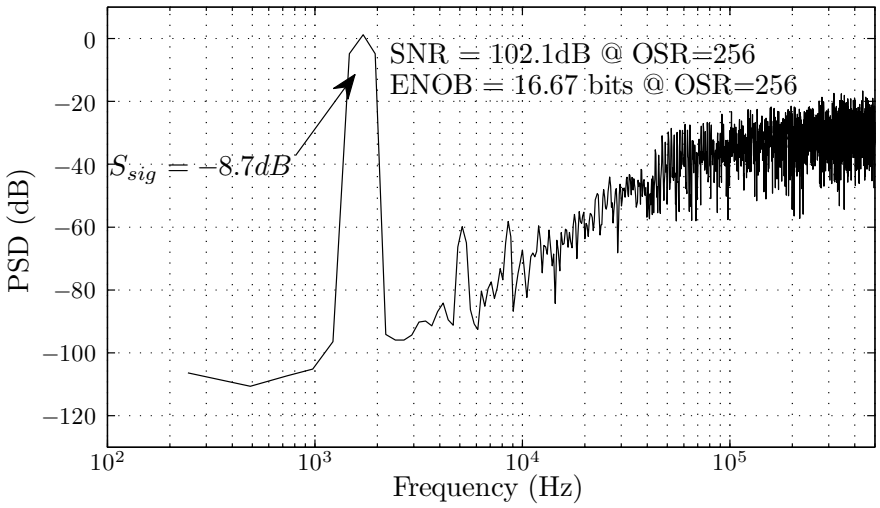


Figure 5.13: Nominal transient noise simulation of the modulator.

5.5 Comparison and performance summary

Tables 5.7 and 5.8 show the main results[1]. It can be seen that the figure of merit (pJ/step) of the present work is among the lowest values. It is only largely overcome by the technique proposed in [29], where the design was specially focused in power consumption reduction.

[1]The results were obtained from the nominal simulation of the transient noise

Table 5.7: Comparisons with other approaches proposed in the literature.

Ref.	**Tech.** $[\mu m]$	**Supply** **[V]**	**BW** **[KHz]**	**OSR**	**fs** **[MHz]**
[17]	0.13	1.2	10.0	128	2.560
[18]	0.15	1.6	2.0	80	0.320
[19]	0.18	1.8	10.0	64	1.280
[20]	0.13	0.8	10.0	40	0.800
[16]	0.13	1.2	14.0	128	3.584
[21]	0.18	0.8	10.0	128	2.560
[22]	0.065	0.9	0.5	250	0.250
[24]	0.18	1.5	1.0	128	0.256
[25]	0.35	1.5	1.0	64	0.128
[26]	0.35	1.8	1.0	16	0.032
[28]	0.18	1.8	10.0	250	5.000
[29]	0.13	1	8.0	40	1.048
[30]	0.35	1	2.0	64	0.256
[31]	0.35	2	1.0	128	0.320
[33]	0.18	0.9	10.0	256	5.000
[34]	0.18	3.3	10.0	256	5.120
[35]	0.18	1.8	4.0	125	1.000
[36]	0.35	1.5	3.9	128	1.000
This work	0.18	1.8	2.0	256	1.000

Table 5.8: Comparisons with other approaches proposed in the literature (cont).

Ref.	**SNDR** **[dB]**	**Power** $[\mu W]$	**FOM** $[p\mathbf{J/step}]$	**FOM** **[dB]**	**ENOB** **bit**
[17]	87.8	148.0	0.37	166.1	14.3
[18]	64	96.0	18.53	137.2	10.3
[19]	95	210.0	0.23	171.8	15.5
[20]	82	48.0	0.23	165.2	13.3
[16]	99	316.0	0.15	175.5	16.2
[21]	80.3	54.0	0.32	163.0	13.0
[22]	76	2.1	0.41	159.8	12.3
[24]	93	1350.0	18.49	151.7	15.2
[25]	89.8	20.0	0.40	166.8	14.6
[26]	80	9.0	0.55	160.5	13.0
[28]	85.8	33.0	0.10	170.6	14.0
[29]	92	38.0	0.07	175.2	15.0
[30]	60	5.0	1.53	146.0	9.7
[31]	77	120.0	10.37	146.2	12.5
[33]	80.1	200.0	1.21	157.1	13.0
[34]	99	1630.0	1.12	166.9	16.2
[35]	68	400.0	24.36	138.0	11.0
[36]	67.1	90.0	6.23	143.5	10.9
This work	102.1	60.9	0.14	177.3	16.7

Chapter 6

Conclusions

6.1 General Conclusions

- The entire design of a single-bit second-order $\Sigma\Delta$ modulator was presented in this dissertation. The circuit satisfies the main requirement of an electric energy measurement application which is a SNR greater than 99dB. The design features relatively low power consumption and robustness that were verify by PVT simulations. Although the design reaches the desired SNR, the circuit only performs proper operation within 2σ range, which means that 5% of the circuits are out of the specifications. The issue is that the input power noise of the OTA is affected by mismatch effects that have direct impact in the modulator response.

- This dissertation introduced a simple procedure to optimize the coefficients of the second-order $\Sigma\Delta$ modulator based on the iteration of the ideal Simulink model. In this specific design, the coefficients were optimized to achieve maximum SNR using minimum capacitance values by exploiting the output swing of the integrators. However, other designs could use the same principle to optimize the output range of the integrators or the DAC reference voltage always assuring high SNR.

- The OTA folded cascode with adaptive bias circuit was used to implement the integrator. It presents more advantages than the classical class AB amplifiers since it does not require an extra stage to drive current. The use of transistors in weak inversion avoid problems about the limited output swing. Additionally, the circuit requires low quiescent current and allow the achievement of a high SR.

6.2 Future Work

6.2.1 System level

- It would be useful to develop a modulator model that includes the statistical variation of the parameters. It would help in both ways. The first is to find the statistical specifications of the integrator. The second is to verify that the mismatch effects and process variations -observed in the circuit simulations- do not affect the modulator performance.

- The procedure to optimize the coefficients is based on the simulation of every possible combination of the variables (coefficients). If the procedure is applied to a third-order modulator, the number of variables increase and the time to obtain every possible combination becomes too long. Hence, the first proposal is developing an analytic model of the $\Sigma\Delta$ modulator that includes the output limits of the integrators. Thus, the optimization procedure can be extended to other modulator orders and topologies. The second proposal is using optimization methods to find the maximum SNR without exploring all the design space.

6.2.2 Circuit level

- In order to complete the design flow, the layout should be realized to verify that the parasitic capacitors do not affect the modulator response. This stage should be done considering that the noise of the digital circuit does not interfere with the analog signals. Subsequently, the chip should be fabricated and measured.

- An interesting idea is the entire characterization of the folded cascode OTA with adaptive bias circuit. This would allow the optimization of the amplifier, and hence the power consumption could be reduced without degrading its performance.

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