INTEGRATED CIRCUIT DESIGN OF A REACTIVE POWER MEASUREMENT SYSTEM USING A SWITCHED-CURRENT HILBERT TRANSFORMER

Eduardo Vilela Pinto dos Anjos

Dissertação de Mestrado apresentada ao Programa de Pós-graduação em Engenharia Elétrica, COPPE, da Universidade Federal do Rio de Janeiro, como parte dos requisitos necessários à obtenção do título de Mestre em Engenharia Elétrica.

Orientador: Fernando Antônio Pinto Barúqui

Rio de Janeiro
Abril de 2016

INTEGRATED CIRCUIT DESIGN OF A REACTIVE POWER MEASUREMENT SYSTEM USING A SWITCHED-CURRENT HILBERT TRANSFORMER

Eduardo Vilela Pinto dos Anjos

DISSERTAÇÃO SUBMETIDA AO CORPO DOCENTE DO INSTITUTO ALBERTO LUIZ COIMBRA DE PÓS-GRADUAÇÃO E PESQUISA DE ENGENHARIA (COPPE) DA UNIVERSIDADE FEDERAL DO RIO DE JANEIRO COMO PARTE DOS REQUISITOS NECESSÁRIOS PARA A OBTENÇÃO DO GRAU DE MESTRE EM CIÊNCIAS EM ENGENHARIA ELÉTRICA.

Examinada por:

Prof. Fernando Antônio Pinto Barúqui, D.Sc.

Prof. Antônio Carlos Moreirão de Queiroz, D.Sc.

Prof. Marcio Nogueira de Souza, D.Sc.

RIO DE JANEIRO, RJ – BRASIL
ABRIL DE 2016

Anjos, Eduardo Vilela Pinto dos

Integrated Circuit Design of a Reactive Power Measurement System using a Switched-Current Hilbert Transformer/Eduardo Vilela Pinto dos Anjos. – Rio de Janeiro: UFRJ/COPPE, 2016.

XIX, 173 p.: il.; 29, 7cm.

Orientador: Fernando Antônio Pinto Barúqui

Dissertação (mestrado) – UFRJ/COPPE/Programa de Engenharia Elétrica, 2016.

Referências Bibliográficas: p. 128 – 135.

1. Reactive Power Measurement. 2. Switched-Current. 3. Hilbert Transformer. 4. Current Memory Cell. I. Barúqui, Fernando Antônio Pinto. II. Universidade Federal do Rio de Janeiro, COPPE, Programa de Engenharia Elétrica. III. Título.

Aos meus avós
Reynaldo e Violeta.

Agradecimentos

Primeiramente, gostaria de agradecer a minha mãe, Maria Verônica Vilela Pinto, por todo o carinho e suporte que me foi dado durante esta nova empreitada. Agradeço todo o carinho que recebi durante toda minha vida e a liberdade para traçar meu próprio futuro. Você é a grande responsável pelo engenheiro e pelo ser humano que me formei. Sem você, nada disso seria possível.

Ao meu professor e orientador, Fernando Antônio Pinto Barúqui, por toda a ajuda e direcionamento durante este projeto de pesquisa. Desafios foram enfrentados e vencidos graças ao seu apoio e disposição. Muito obrigado pela consideração e pelas oportunidades conseguidas.

To Kanako Matsuyama, my amazing love and partner. Thank you for your support, patience and advices. No matter how far you can be, you always make me feel close to you. Your support makes me stronger and makes me push myself further.

Ao meu pai, Jackson Gonçalves dos Anjos, por sua amizade e por seus conselhos e palavras de sabedoria, que levarei por toda minha vida.

Ao meu irmão Henrique Vilela Pinto dos Anjos, por sua amizade e parceria em vários momentos especiais da minha vida.

Gostaria de agradecer também aos professores Antônio Carlos Moreirão de Queiroz e Marcio Nogueira de Souza por terem aceitado participar da banca de defesa desta dissertação.

Aos membros do laboratório PADS, professores e alunos, em especial ao João Alberto de França Ferreira e Allan Bides de Andrade, pela caminhada conjunta em direção ao título de mestre.

E finalmente aos muitos amigos que compartilho meu dia-a-dia e fazer desta vida muito mais alegre e divertida, cujos nomes são muitos e faltaria espaço para tantos. Vocês sabem quem são.

Resumo da Dissertação apresentada à COPPE/UFRJ como parte dos requisitos necessários para a obtenção do grau de Mestre em Ciências (M.Sc.)

SISTEMA DE MEDIDA DE POTÊNCIA REATIVA UTILIZANDO UM TRANSFORMADOR DE HILBERT EM CORRENTE CHAVEADA INTEGRADO NA TECNOLOGIA CMOS

Eduardo Vilela Pinto dos Anjos

Abril/2016

Orientador: Fernando Antônio Pinto Barúqui

Programa: Engenharia Elétrica

Sistemas de Medida de Potência Reativa são uma parte fundamental dos medidores de energia modernos, e com a crescente demanda por fontes de energia renovável e geração distribuida, a procura por sistemas de medida sob condições não-senoidais aumentou na última decada. Porém, soluções em domínio analógico representam uma possibilidade de implemetação de baixo custo e não foram exploradas por trabalhos anteriores. Nesta dissertação, a teoria da medida de potência reativa é apresentada e um sistema de medida de potência reativa em domínio analógico é desenvolvido. A técnica de medida proposta emprega um transformador de Hilbert em corrente chaveada que utiliza sessões de passa-tudo estruturais para obter baixa sensibilidade ao descasamento de transistores. Para avaliar a estrutura proposta, um circuito integrado é projetado baseado em padrões internacionais estabelecidos pela Comissão Eletrotécnica Internacional (IEC). A implemetação final é testada a partir de simulação de circuitos utilizando ferramentas de *software* do estado da arte e simulações de Monte Carlo são executadas para observar a sensibilidade da medida ao descasamento de transistores.

Abstract of Dissertation presented to COPPE/UFRJ as a partial fulfillment of the requirements for the degree of Master of Science (M.Sc.)

INTEGRATED CIRCUIT DESIGN OF A REACTIVE POWER MEASUREMENT SYSTEM USING A SWITCHED-CURRENT HILBERT TRANSFORMER

Eduardo Vilela Pinto dos Anjos

April/2016

Advisor: Fernando Antônio Pinto Barúqui

Department: Electrical Engineering

Reactive Power Measurement Systems (RPMS) are a fundamental part of modern smart meters, and with the increasing demand for renewable sources and distributed generation, the search for measurement systems under non-sinusoidal conditions grew in the last decade. However, analog domain solutions were not explored by previous works and it represents a possibility for a low-cost implementation. In this thesis, the theory of reactive power measurement is studied and an analog domain RPMS is developed. The proposed measurement technique employs a switched-current Hilbert transformer that uses structurally all-pass section to achieve low-sensitivity to transistor mismatch. To evaluate the proposed structure, an integrated circuit is designed based on international standards from the International Electrotechnical Commission (IEC). The final implementation is evaluated through circuit simulation using state-of-the-art software tools and Monte Carlo simulations are performed to observe measurement sensitivity to transistor mismatch.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

During the turnover of the 19th century, an intensive dispute was drawn between two brilliant scientists: Thomas Edison and Nikolas Tesla. Both rivals proposed different ideas to provide electrical energy to the population. Edison's idea was to transmit the energy using direct current (DC), which he claimed to be superior since it maintained a lower voltage for the consumer, making it safer. Tesla, on the other hand, proposed a concept of transmission using alternate current (AC), which was more practical, on that time, to transmit a higher quantity of energy, as required by big cities and factories [1]. The result of the famous "War of Currents" is widely known: until today, the electrical energy is transmitted - with few exceptions [2] - using alternate current.

The main challenge faced by AC power transmission arise from AC circuits. Reactive elements, such as capacitors and inductors, can store energy and provoke reversals of the direction of the energy flow. Therefore, AC power is analyzed by dividing it into two quantities, active and reactive power. The active power is the 'conventional energy', responsible to generate heat, movement and light. The reactive power does not perform these tasks directly, but it is fundamental to keep the control of the grid as well as to generate electromagnetic fields for the operation of motors, transformers and generators.

Since the reactive power is important to grid's stability, the electricity provider must measure the amount consume by its loads - i.e energy consumers. However, reactive power measurement is a difficult task, so many providers charge only for the active power consumed by small users, such as households, and impose a fine when the reactive power surpasses a limit on large users, which must keep control of its own consumption [3]. Therefore, the measurement of reactive power by the electricity provider would improve its billing methods [4] and improve grid control.

The demand for continuous power measurement only tend to increase with the spread of distributed generation, renewable energy sources and smart grids. A recent example shows this demand: in 2010 the main electricity provider of Italy, ENEL,

concluded the modernization of more than 30 million energy meters, to improve energy efficiency, billing methods and introduce automatic billing [5].

Reactive power measurement is also essential for quality control of the electrical grid and its becoming more important in recent years since the major part of electrical loads in power systems became non-linear or time-varying. This happened due to proliferation of power electronic equipment, such as induction furnaces, adjustable speed drivers and clusters of personal computers [6]. This change not only emphasize the need to measure reactive power consumption, but also makes it even more challenging due to the number of harmonics introduced into the grid.

The presence of harmonic distortion into the grid obsolete the definitions and measurement methods utilized by the industry and new solutions were developed towards reactive power measurement. A wide variety of works were presented in the literature to perform the measurement, from which we highlight the Hilbert transformer based methods [7–9], FFT algorithms [10, 11] and others [12–14]. Although these are different techniques, they are all executed in digital domain, employing expensive circuits such as DSPs and FPGAs.

Analog domain implementations was not explored to implement the measurement under non-sinusoidal conditions, and it represent a possibility of low-cost, low-power consumption and low-complexity, which are key aspects on a massive renovation of energy meters as it was done by ENEL. In this context, it will be proposed an analog implementation of a reactive power measurement system. The system will employ a discrete-time Hilbert transformer implemented using switched-current techniques. The Hilbert transformer design will be implemented using a half-band filter design procedure [15]. The design process will be detailed, from a system perspective to the circuit design using a CMOS $0.35\mu m$ process. The proposed system is validated using a wide variety of simulations on Cadence analog design flow.

1.1 Switched-Current Circuits

Switched-current circuits were initially proposed in 1988, and it arised with the need to implement analog discrete-time signal processing in VLSI circuits [16]. Since fabrication process for digital circuits are not optimized to implement capacitors, the use of switched-capacitors to perform discrete-time signal processing suffered from performance issues. Furthermore, in VLSI process, the power supply voltage is limited, which reduces the dynamic range of switched-capacitor circuits directly.

To overcome the challenge, Hughes [17] proposed the use of current-mode signal processing and introduced the 'current memory cell' presented in Fig. 1.1. When the switch is closed, the input current is introduced into the current mirror and the gate-source voltage of M_1 changes according to the input current. This current is

copied to transistor M_2 since it works as a current mirror. When the switch opens, the gate-source capacitor of M_2 holds the voltage correspondent to the input current until the switch closes again. Therefore, the current value is indirectly stored by the gate-source capacitance of M_2. This way, a half-unit delay is implemented, which is the base of a discrete-time filters.

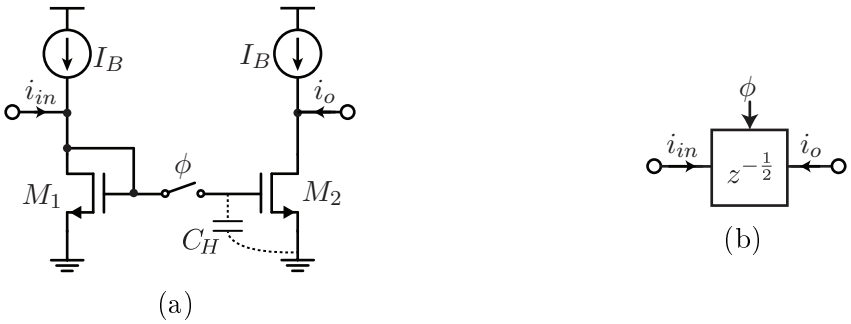


Figure 1.1: Second generation current memory cell. (a) Circuit and (b) Block representation.

The current memory cell, also known as current sample and hold and current copier cell, had some performance issues due to mismatch between transistors, since it was design based in the current mirror. When implementing a discrete-time analog filter, Hughes' memory cell introduced losses. To address this issue, Tsividis [16] proposed a single-transistor current memory cell, presented in Fig. 1.2. During sampling phase (ϕ_1), the transistor is diode-connected and an input current is introduced at its drain. The gate-source voltage set depends only on the transistor itself, and therefore during holding phase (ϕ_2), no losses occur due to mismatch.

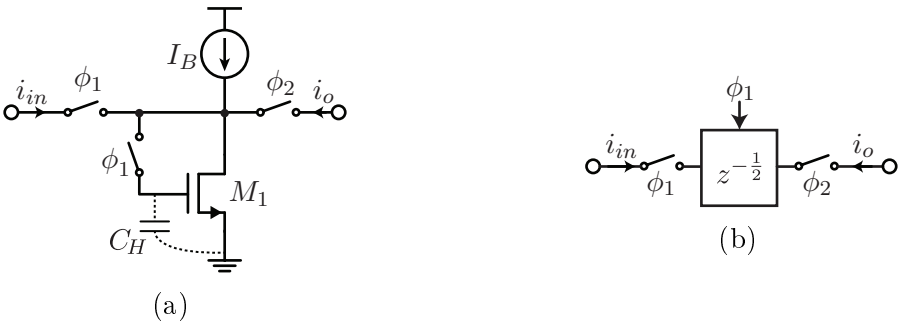


Figure 1.2: Second generation current memory cell. (a) Circuit and (b) Block representation.

In the literature, Hughes' copier cell is usually referred as first generation current memory cell and Tsividis' one as second generation current memory cell. Although both of them seem very simple circuits, they are very sensitive to charge injection from the switch. Also since the $I_D - V_{GS}$ curve of MOS transistors is non-linear, charge injection potentially introduce distortion. Therefore, the search for charge

injection improvements on both first and second generation current memory cells was intense for the last 25 years. Many techniques were proposed to mitigate charge injection, from which we can highlight the dummy replica [18], S^2I [19], common-mode feedforward structures [20] and zero-voltage switching [21]. In this work, we also introduce an improved version of the zero-voltage switching current memory cell, with a high-linearity operation [22] to allow a high-precision measurement system.

1.2 Work Outline and Contributions

This thesis is divided as follows: In **Chapter 2**, the theory and switched-current implementation of a Hilbert transformer is presented. **Chapter 3** addresses the reactive power measurement system theory and literature review. We explore the usage of one Hilbert transformer to execute the measurement and the use of a pair of Hilbert transformer for the same task. A technique is also proposed to employ the switched-current Hilbert transformer and eliminate systematic errors. In **Chapter 4**, an overview of the system design is presented, considering the standards from regulatory agencies. **Chapter 5** presented the theory and design of the current memory cell utilized in this work. **Chapter 6** presents the complementary circuits necessary for the system implementation. In **Chapter 7**, the final system is presented and extensively validated through circuit simulation. Finally, in **Chapter 8** the conclusions and future works are addressed. Process characterization and some mathematical derivations were addressed in the Appendix.

The main contribution in this work are: the development of a low-sensitivity Hilbert transformer using switched-current techniques [23] using structurally all-pass sections to achieve low variation with transistor mismatch; the development of a high-linearity zero-voltage switching current memory cell for measurement applications [22] which allowed the proper operation of the system to achieve IEC requirements; a coefficient sharing method to allow perfect matching between two Hilbert transformers and reduce phase errors into the measurement result.

Chapter 2

The Hilbert Transformer

The Hilbert Transformer is a widely used block in many important applications of electronics, such as single side-band (SSB) modulation [24], reactive power measurement [7] and many others [25]. We start this chapter briefly reviewing its basic concepts and also reviewing an implementation based on an IIR half-band filter. We then propose a switched-current implementation of the Hilbert transformer.

2.1 Hilbert Transform

The Hilbert transform of a function $f(t)$ is defined by

$$H\left\{f(t)\right\}(t) = \frac{1}{\pi}\int_{-\infty}^{\infty}\frac{f(\tau)}{t-\tau}d\tau \tag{2.1}$$

which is a convolution integral, therefore it can be represented by

$$H\left\{f(t)\right\}(t) = \frac{1}{\pi t} * f(t) \tag{2.2}$$

The relationship in 2.2 can be described in the frequency domain as

$$H\left\{f(t)\right\}(\omega) = -j\mathrm{sgn}(\omega)F(\omega) \tag{2.3}$$

where $F(\omega)$ is the Fourier transform of $f(t)$ and $\mathrm{sgn}(\omega)$ is the *signum* function. If we define $H_{HT}(\omega)$ as

$$H_{HT}(\omega) = -j\mathrm{sgn}(\omega) = \begin{cases} -j, & \omega > 0 \\ 0, & \omega = 0 \\ j, & \omega < 0. \end{cases} \tag{2.4}$$

the Hilbert transform of a signal can be obtained using a filter with $H_{HT}(\omega)$ as its transfer function, as shown in Fig. 2.1a. The frequency response of $H_{HT}(\omega)$ is shown

in Fig. 2.1b.

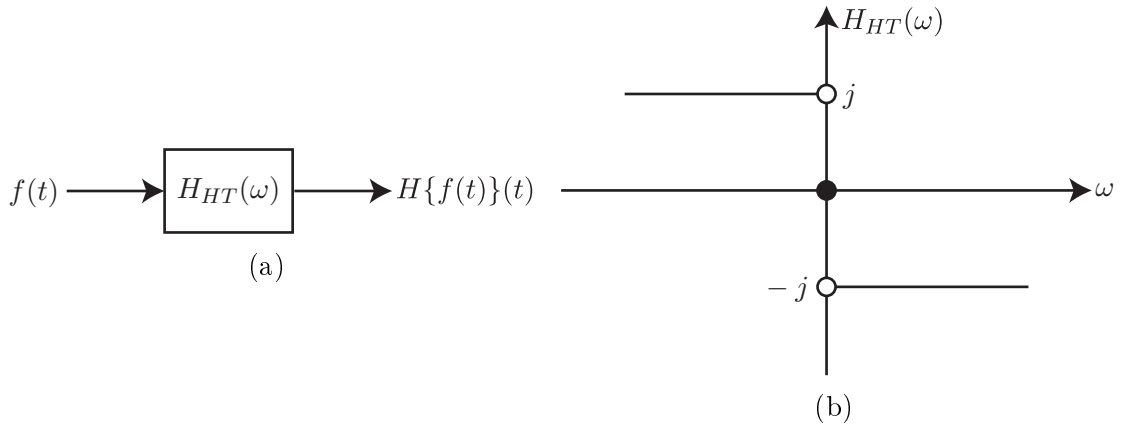


Figure 2.1: (a) Hilbert transformer filter. (b) Frequency response of the Hilbert transformer.

Because of this property, a filter with frequency response equal to $H_{HT}(\omega)$ is called a **Hilbert transformer**. Also, one can notice that $|H_{HT}(\omega)| = 1$ for $\omega \neq 0$ and its phase response is given by

$$\angle H_{HT}(\omega) = \begin{cases} -90°, & \omega > 0 \\ 0, & \omega = 0 \\ 90°, & \omega < 0. \end{cases} \tag{2.5}$$

Therefore, the Hilbert transformer is also known as a **90 degrees phase shifter**. It can also be extended to discrete-time systems, which is explored in the next section.

2.2 Discrete-Time Hilbert Transformer

A discrete-time Hilbert transformer (DHT) is a linear-shift discrete-time invariant system with ideal frequency response given by [1]

$$H_{HT}(e^{j\omega}) = \begin{cases} -j, & 0 < \omega < \pi \\ j, & -\pi < \omega < 0. \end{cases} \tag{2.6}$$

where its impulse response is non-causal, and therefore it cannot be physically realized. However, it is possible to approximate its ideal behavior using a well known design procedure based on half-band filter [15].

Let us first consider the discrete-time complex half-band filter $Q(e^{j\omega})$, described by

[1] For simplicity, the zero in the origin is neglected.

$$Q(e^{j\omega}) = \begin{cases} 1, & 0 \leq \omega \leq \pi \\ 0, & -\pi < \omega < 0. \end{cases} \tag{2.7}$$

which is related to the Hilbert transformer by

$$Q(e^{j\omega}) = \frac{1}{2}\left(1 + jH_{HT}(e^{j\omega})\right) \tag{2.8}$$

The complex half-band filter can be realized by shifting a real half-band filter $R(e^{j\omega})$ in the frequency domain by $\frac{\pi}{2}$

$$R(e^{j\omega}) = Q\left(e^{j(\omega+\frac{\pi}{2})}\right) = \begin{cases} 1, & 0 \leq |\omega| < \frac{\pi}{2} \\ 0, & \frac{\pi}{2} \leq |\omega| < \pi. \end{cases} \tag{2.9}$$

The relationships in (2.8) and (2.9) can be extended to the z-domain by using $z = e^{j\omega}$, leading to

$$Q(z) = \frac{1}{2}\left(1 + jH_{HT}(z)\right) \tag{2.10}$$

and

$$\begin{aligned} R\left(e^{j\omega}\right) &= Q\left(e^{j\omega}e^{j\frac{\pi}{2}}\right) \\ R\left(z\right) &= Q\left(jz\right) \\ R\left(-jz\right) &= Q\left(z\right) \end{aligned} \tag{2.11}$$

As described in [26], a large class of stable IIR half-band filters can be decomposed into a sum of two all-pass transfer functions. Therefore, $R(z)$ can be approximated by $\hat{R}(z)$, which is given by

$$\hat{R}(z) = \frac{1}{2}\left[A_1(z^2) + z^{-1}A_2(z^2)\right] \tag{2.12}$$

where $A_1(z)$ and $A_2(z)$ are stable all-pass transfer functions, and the right side of (2.12) is an equiripple aproximation of the half-band filter [27]. To obtain $\hat{R}(z)$, it will be used the algorithm proposed in [28], which is already implemented in the Signal Processing Toolbox from MATLAB. This toolbox will be used in Chapter 4 to obtain the coefficients for the measurement system.

Applying equation (2.12) to the relationship in (2.11) we obtain

$$\hat{Q}(z) = \frac{1}{2}\left[A_1(-z^2) + jz^{-1}A_2(-z^2)\right] \tag{2.13}$$

which shows that the complex half-band filter can be realized by inverting the signal of the transfer function coefficients of the all-pass sections. Also, since the half-band

filter is designed to have very small atenuation in the passband, it means that $A_1(-z^2)$ and $z^{-1}A_2(-z^2)$ are approximately out of phase by 90 degrees [27].

A simple way to observe this is to trace the frequency response of (2.13). Let

$$A_1(-z^2)\big|_{z=e^{j\omega}} = 1e^{j\theta_1(\omega)} \tag{2.14}$$

and

$$z^{-1}A_2(-z^2)\big|_{z=e^{j\omega}} = 1e^{j\theta_2(\omega)} \tag{2.15}$$

then the frequency response of $Q(z)$ is given by

$$\begin{aligned} 2\hat{Q}(e^{j\omega}) &= 1e^{j\theta_1(\omega)} + 1e^{j\frac{\pi}{2}}1e^{j\theta_2(\omega)} \\ 2\hat{Q}(e^{j\omega}) &= 1e^{j\theta_1(\omega)} + 1e^{j\left(\frac{\pi}{2}+\theta_2(\omega)\right)} \\ 2\hat{Q}(e^{j\omega}) &= 1e^{j\theta_1(\omega)}\left[1 + 1e^{j\left(\frac{\pi}{2}+\theta_2(\omega)-\theta_1(\omega)\right)}\right] \end{aligned} \tag{2.16}$$

Since the frequency response of $Q(e^{j\omega})$ is known from (2.7), it is possible to find the relationship between $\theta_1(\omega)$ and $\theta_2(\omega)$. For $0 \leq \omega \leq \pi$, we have

$$\left[1 + 1e^{j(\frac{\pi}{2}+\theta_2(\omega)-\theta_1(\omega))}\right] = 2 \rightarrow \frac{\pi}{2} + \theta_2(\omega) - \theta_1(\omega) = 0 \tag{2.17}$$

which leads to

$$\theta_2(\omega) = -\frac{\pi}{2} + \theta_1(\omega). \tag{2.18}$$

However, for $-\pi < \omega < 0$, we have

$$\left[1 + 1e^{j(\frac{\pi}{2}+\theta_2(\omega)-\theta_1(\omega))}\right] = 0 \rightarrow \frac{\pi}{2} + \theta_2(\omega) - \theta_1(\omega) = \pi \tag{2.19}$$

which leads to

$$\theta_2(\omega) = \frac{\pi}{2} + \theta_1(\omega). \tag{2.20}$$

Therefore, the complete relationship between $\theta_1(\omega)$ and $\theta_2(\omega)$ is given by

$$\theta_2(\omega) = \begin{cases} -\frac{\pi}{2} + \theta_1(\omega), & 0 \leq \omega \leq \pi \\ \frac{\pi}{2} + \theta_1(\omega), & -\pi < \omega < 0. \end{cases} \tag{2.21}$$

which means that a filter with transfer function $z^{-1}A_2(-z^2)$ approximates the Hilbert transform of the output of a filter with transfer function $A_1(-z^2)$ when both have same inputs.

In other words, if we apply a signal $X(z)$ through $A_1(-z^2)$, obtaining $Y_{IP}(z)$,

and through $z^{-1}A_2(-z^2)$, getting $Y_{QP}(z)$, as shown in Fig. 2.2, and adopt $Y_{IP}(z)$ as a reference, $Y_{QP}(z)$ is an approximation for the Hilbert transform of $Y_{IP}(z)$.

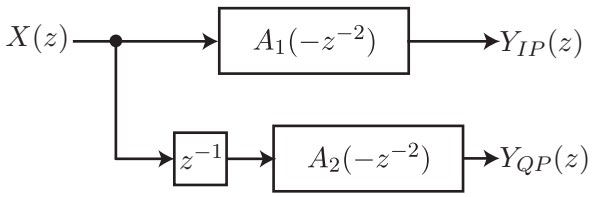


Figure 2.2: Hilbert transformer implementation using all-pass transfer functions.

In many telecommunication applications, the reference signal is said to be *in-phase* and the 90 degree phase-shifted one is on *quadrature phase*. Thus the subscripts for each filter path output.

2.2.1 Phase Imbalance and Bandwidth

Since the Hilbert transformer is designed indirectly through a half-band filter, it is important to relate the design constraints from the transformer with the design constraints of the half-band filter.

Because of an equirriple design, the cutoff frequency of the half-band filter can be related to the bandwidth of the Hilbert transformer. From Fig. 2.3, one can see that

$$BW = 2\omega_p \tag{2.22}$$

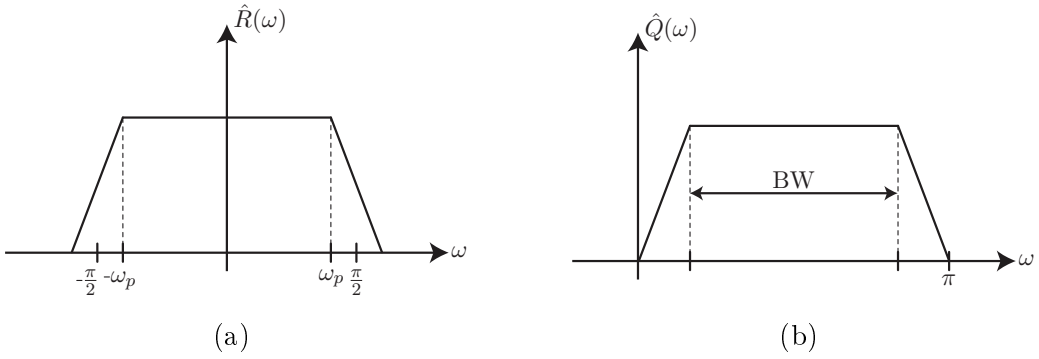


Figure 2.3: Relationship between (a) half-band filter cutoff frequency ω_p and (b) Hilbert transformer bandwidth BW.

Petraglia derived in [27] a relationship between the phase imbalance of the Hilbert transformer and the half-band filter stop-band magnitude. The upper-bound for the phase imbalance is given by

$$\Delta\theta(\omega) \leq 2\varepsilon_s \tag{2.23}$$

where $\Delta\theta(\omega)$ is the phase imbalance in radians, inside the bandwidth BW, and ε_s is the stop-band magnitude of the half-band filter.

2.3 Structurally All-Pass Filters

In the last section, we introduced a Hilbert transformer realization with all-pass transfer functions. Therefore, our goal in this section is the design of transfer functions using switched-current techniques.

Both all-pass transfer functions from (2.12) can be mathematically described as a cascade of first order all-pass sections [29], leading to

$$A_i(z) = \prod_{j=1}^{N_i} \frac{k_{ij} + z^{-1}}{1 + k_{ij} z^{-1}}, \text{ for i=1,2.} \tag{2.24}$$

where the order N_i of each filter path is defined by the design constrains of the half-band filter, as shown by Ansari [15]. This configuration is interesting from an analog design viewpoint because it allows to reuse the structure to implement a long filter, therefore simplifying the schematics and layout design. Moreover, one-coefficient sections simplifies the implementation of structurally all-pass networks.

Structurally all-pass sections (SAPS) are transfer functions which both numerator and denominator coefficient are realized by the same building block (e.g. a current mirror), so that if there is a variation on the coefficient value, the transfer function keeps all-pass. The use of SAPS provides circuits with very low sensitivity to parameters variations, such as transistor mismatch and process gradient [30].

An example of a SAPS block diagram is presented in Fig. 2.4. It is easy to see that only one gain block is responsible to realize both numerator and denominator coefficient.

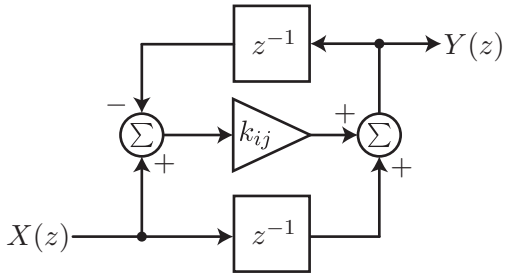


Figure 2.4: Block diagram of a first-order structurally all-pass section.

2.3.1 Switched-Current Implementation

To implement the SAPS with switched-current, a transformation from z to $-z^2$ must be applied into (2.24), resulting in

$$A_i(-z^2) = \prod_{j=1}^{N_i} \frac{k_{ij} - z^{-2}}{1 - k_{ij} z^{-2}}, \text{ for i=1,2.} \tag{2.25}$$

Therefore, the circuit must implement the transfer function

$$\frac{i_o}{i_{in}} = \frac{k_{ij} - z^{-2}}{1 - k_{ij} z^{-2}} \tag{2.26}$$

which can be rewritten as

$$i_o = -i_{in} z^{-2} + k_{ij}(i_{in} + i_o z^{-2}) \tag{2.27}$$

Using the second generation current memory cell presented in the previous chapter, a block diagram of the circuit can be developed, as shown in Fig. 2.5.

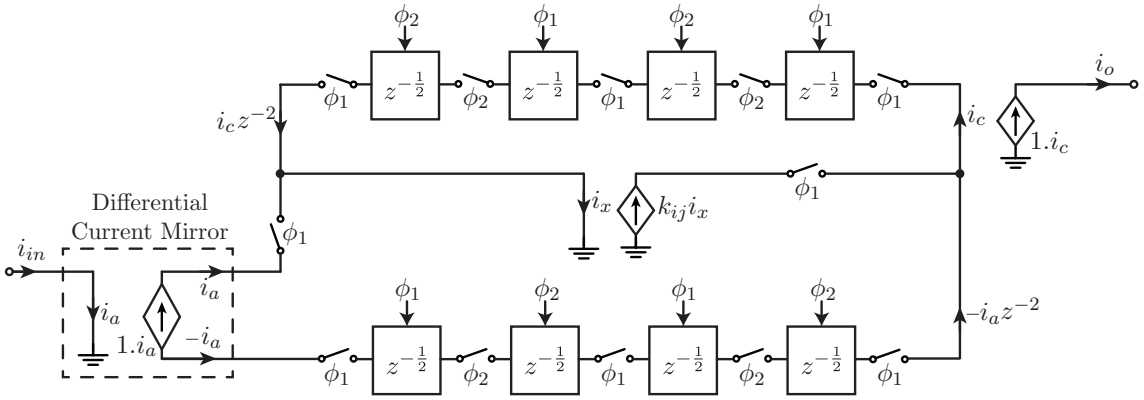


Figure 2.5: Block diagram of an one-coefficient switched-current structurally all-pass section.

The coefficient is implemented by only one current mirror with a gain equal to k_{ij}. The output is obtained by a current copier. Since both positive and negative copies of the input current are needed to implement the circuit, we developed a differential current mirror, shown in Fig. 2.6.

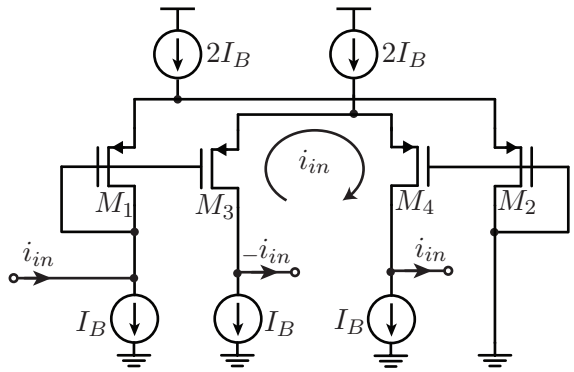


Figure 2.6: Differential Current Mirror implementation.

This circuit is composed by two identical differential amplifiers, M_1-M_2 and M_3-

M_4, with differential inputs connected together. The differential amplifier M_1-M_2 have both transistors diode-connected. The input current i_{in} of M_1-M_2 determines the input differential voltage, which is the same for M_3-M_4. So, a copy of i_{in} is generated in M_3-M_4, but with opposite directions, thus different polarities. The complete circuit for the switched-current structurally all-pass section (SI-SAPS) is presented in Fig. 2.7. We emphasize that, in a real circuit implementation, as will be presented in Chapter 6, more sophisticated current memory cells will be used.

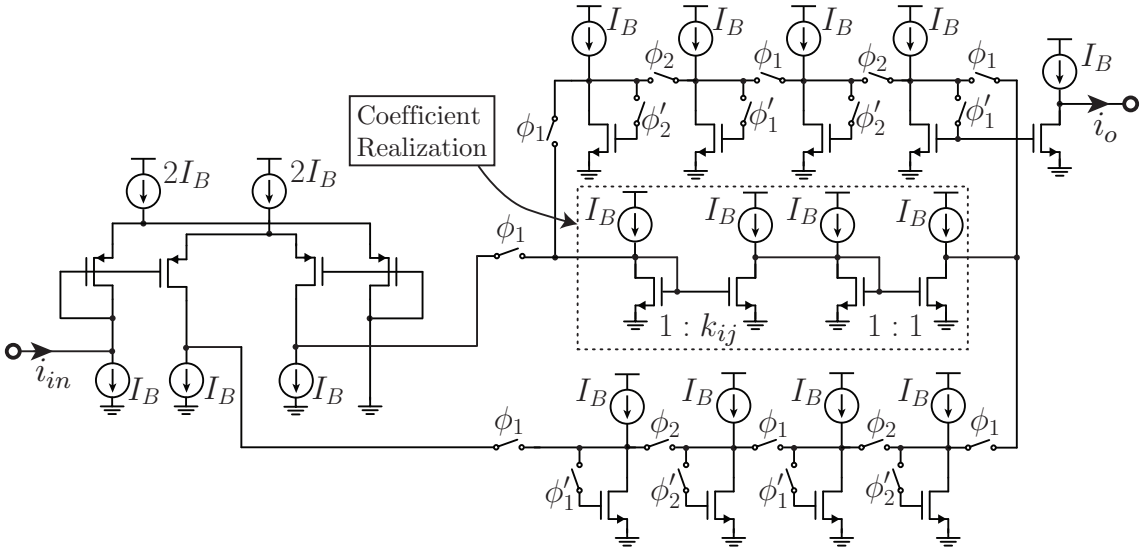


Figure 2.7: Switched-current circuit implementation of a Structurally All-Pass Section.

2.4 Switched-Current Hilbert Transformer Design Example

As an example, we will implement the Hilbert transformer proposed in [27] with bandwidth between 0.05π and 0.95π and maximum phase-error equal to $\theta_{err} = 0.02rad$. This specifications result into the above transfer functions

$$A_1(-z^2) = \frac{-z^{-2} + 0.1907}{1 - 0.1907z^{-2}} \times \frac{-z^{-2} + 0.8607}{1 - 0.8607z^{-2}} \tag{2.28}$$

$$A_2(-z^2) = \frac{-z^{-2} + 0.5531}{1 - 0.5531z^{-2}} \tag{2.29}$$

Using the SI-SAPS developed in the last section, the implementation for this Hilbert transformer is shown in Fig. 2.8 [23]. The delay line z^{-1} before the all-pass transfer function $A_2(-z^2)$ was taken from inside of the first SI-SAPS in order to save hardware.

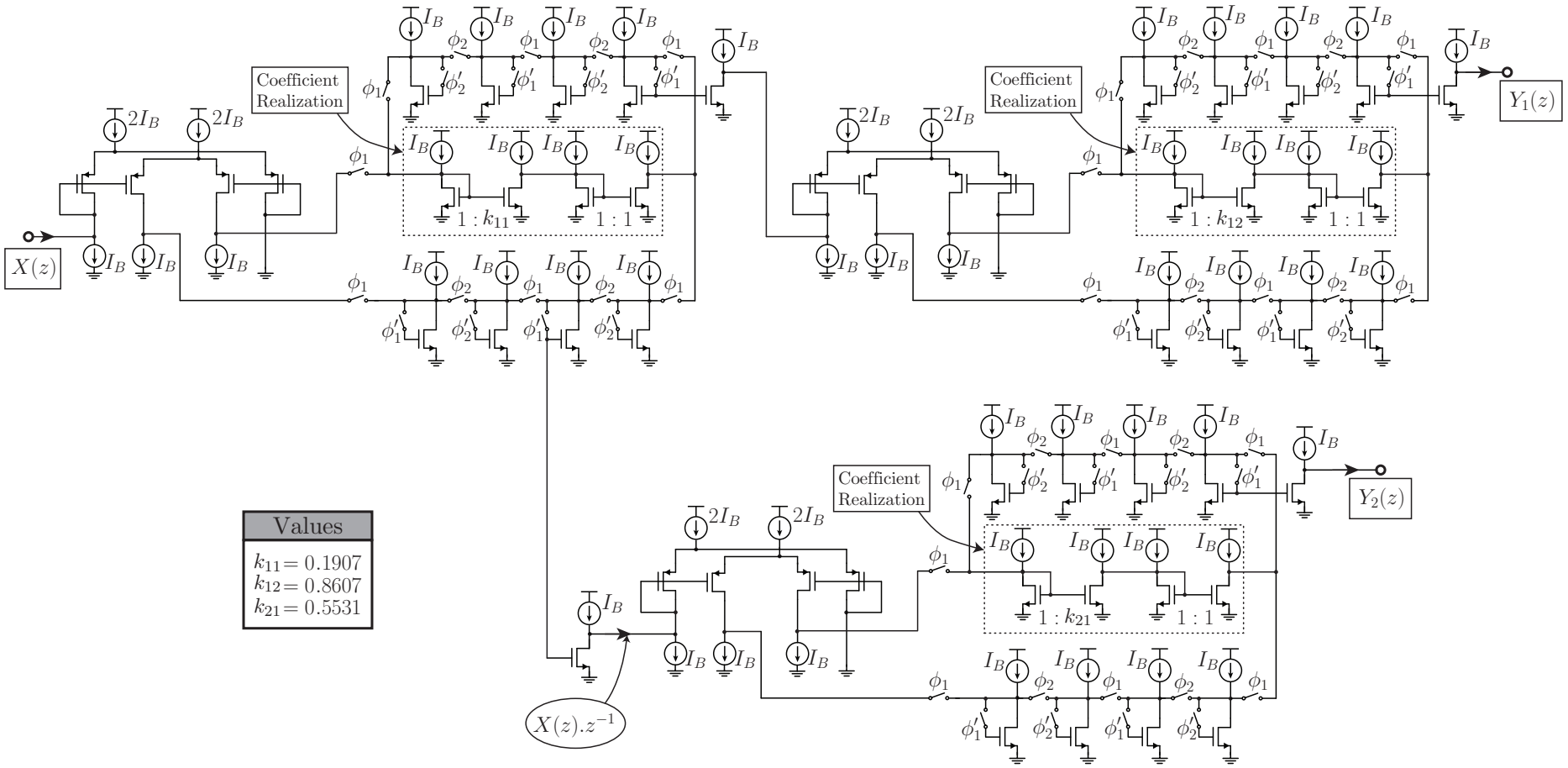


Figure 2.8: Switched-current implementation of the Hilbert transformer.

The proposed implementation was simulated to verify its behavior. Since analog circuits are subject to non-ideal effects during manufacture, such as transistor mismatch and process gradients, it is important to observe the circuit sensitivity to this non-ideal effects. To perform this analysis, we used the ASIZ program, developed by de Queiroz [31]. Simulation results are shown in Fig. 2.9. In the top-right corner, one can see the detailed response inside the frequency range of the Hilbert transformer [23].

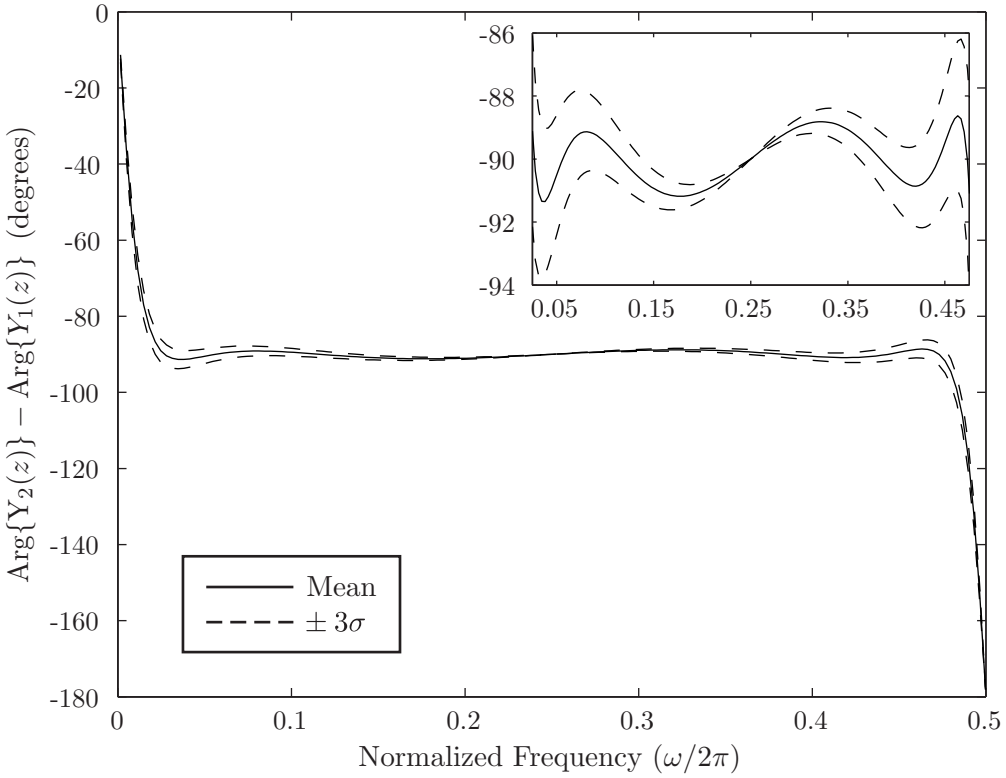


Figure 2.9: Phase response of the Hilbert transformer.

For the sensitivity analysis, it was adopted 1% of mismatch error between the current mirrors. The statistical variation of phase response shows the total effect of mismatch errors between transistors. The solid lines are the mean response and the dashed lines represent the its statistical variation.

One can see that the overall frequency response presents a very small variation in the desired frequency range, mainly due to the use of SAPS. The maximum phase-error due to mismatch effects is ± 2.9 degrees within the transformer frequency range.

Chapter 3

Reactive Power Measurement Systems

Since the wide spread of electrical energy distribution in the United States, in the early 20th century, it began a search for energy and power measurement methods and until today it has not reach to an end. The first developments towards power measurement are dated from the decade of 1910, using electrostatic elements to execute the readings of active and reactive power values. Further, the first measurement procedures using electronic devices are dated from the 50's decade and utilize vacuum tubes as main components [32].

With the advance of electronics, new methodologies in the analog domain [33, 34] and also in digital domain [35] were developed, focusing only in sinusoidal systems, since very low distortion was introduced into the grid by its users. However, with the modern era of power electronics, the load profile changed and became highly non-linear and time varying, which introduces high distortion into the power grid and created the necessity to study reactive power measurement under non-sinusoidal conditions [6].

In this Chapter, we first present a bibliography review of the main proposed methods for reactive power measurement under non-sinusoidal conditions. In addition, we will review the Hilbert transformer based method and proposed a new method using analog design. Simulation results and comparison between similar methods are also presented.

3.1 Literature Review

A wide range of works were presented in the context of reactive power measurement systems under non-sinusoidal conditions and they can be separated into three groups, according to the measurement procedure used in each work. The first group

decided to use a Hilbert transformer to achieve a 90 degrees phase shift [7–9] but using different algorithms and implementation methods. The second group measured the reactive power using a Fast Fourier Transform (FFT) algorithm in different forms [10, 11]. The third group is a miscellaneous of various methods that does not fit the previous groups [12–14]. In the next sub-sections the details of each work will be presented.

3.1.1 Hilbert transformer based methods

The Hilbert transformer is a building block which introduces a 90 degrees phase shift in the input signal. The measurement is performed by phase shifting the current or the voltage signal and then multiplying both signals to obtain the reactive power. There are many ways to implement the Hilbert transformer, such as IIR filters [7] and FIR filters [8, 9], which leads to different precision and complexity. More details on the Hilbert transformer measurement method will be presented in the next section.

The research made by Hao [7] is the main reference for this dissertation. His work implemented a digital Hilbert transformer using the half-band filter design procedure explained in Chapter 2. Its physical implementation was made using a Digital Signal Processor (DSP) rather than a application specific integrated circuit (ASIC). However, most of his results were obtained from behavioral models in MATLAB and not from the physical implementation. The filter used as a Hilbert transformer is his work has a 13^{th} order transfer function, or six all-pass sections, which is a smaller complexity when compared with other works.

The work presented in [8] used a Hilbert transformer implemented by a FIR Chebyshev equiripple filter with 31 taps, which is much higher order when compared with the previous work. Its implementation was made in a FPGA, which represents a high cost of manufacturing, therefore is not viable for commercial applications. Moreover, very few details were given about its performance.

Another research made using FIR filters was presented in [9]. This work implemented an application specific integrated circuit (ASIC) where the reactive power measurement system was a block in a solid state electrical energy meter. The filter used as a Hilbert transformer was a coefficient optimization filter with 31 taps. It was integrated using a AMI $0.35\mu m$ CMOS process and was synthesized using VHDL. The reactive power measurement block alone occupied an area of $0.83mm^2$.

3.1.2 Fast Fourier Transform based methods

The reactive power measurement using Fourier transform is perform by evaluating each harmonic components of both voltage and current signals, therefore obtaining

active and reactive power. However, the Fast Fourier Transform (FFT) algorithm is complex and hardware demanding. To overcome this high-cost, the work presented in [10] used the Goertzel algorithm, which is a high-efficient implementation of the FFT, saving area and computational resources. However, the filter described by the authors is quite simple, but also quite limited, since it only measures the power of the fundamental component. The main advantage of the proposed system is its physical implementation on a Microcontroller, which has low cost and still achieved good precision when compared with more expensive methods.

The research presented in [11] was straight-forward about its implementation, using an FPGA and standardized blocks from the FPGA manufacturer. Thus, it resulted in a system with a high switching frequency and a very high hardware complexity. The system used a 512-point FFT for both voltage and current signals, resulting in an usage of 23% of the FPGA space but also achieving good measurement precision. The authors also presented a compact version of the system, which occupied just 3% of the FPGA space, but compromising the measurement precision. Also, as said before, the use of FPGA is not viable commercially because of its high cost.

3.1.3 Alternative Methods

Another group of works proposed different structures to measure reactive power, from which we can highlight a Wavelet transform based [12], a technique based on Walsh functions [13] and also a system based on Adaptative Notch Filters [14].

The Wavelet transform based work presented by Yoon [12] is very similar to the Hilbert transform based methods, since it also uses a 90 degree phase shifter, but instead of multiplying in-phase and quadrature components, a Wavelet transform is performed in each of them. As a result, this method does not measure instantaneous reactive power. Moreover, the use of Wavelet transform represents a bigger amount of processing power. On the other hand, his method showed simplicity and high precision. This work used a filter with ten all-pass sections, or 21^{st} order.

Another interesting work was presented by Abiyev [13], which uses Walsh functions to measure the reactive power. After a long mathematical development, the authors reached a simple final result, which consist in multiplying the input signals by 1, -1 or 0 in a specific order. Besides its simplicity, the proposed method allowed measurement of the fundamental and the harmonics separately and it does not require a 90 degree phase shift. However, their method achieved a inferior precision when compared with other works. Also, there was not any physical implementation, thus presenting only simulated results.

The work presented in [14] introduced a technique that used Adaptive Notch

Filters (ANF) to execute reactive power measurement. Since the filters were adaptive, they could respond to a frequency variation easily. Also, the method presented a very high precision measurement and it also delivers the instantaneous reactive power. However, for every harmonic component added on the measurement, another filter must be added to the system, making the technique very hardware demanding for wideband measurements. For instance, to measure the reactive power in 19 harmonics components, it would be necessary 19 ANFs in the system, making it quite extensive.

3.1.4 Summary

A summary of the related works is presented on Table 3.1. As we showed, reactive power measurement is still a subject of study with many different approaches but they all have something in common: digital domain approach. Wideband procedures in analog domain were not explored by previous researches and it represents a possibility of a low-cost high-precision measurement system, which justify the research done in this dissertation.

Table 3.1: Characteristics of related works.

	Measurement Method	Filter Order	Physical Implementation	Measurement	Maximum Error
[7]	Hilbert IIR	6 coefficients	DSP	40 Hz - 960 Hz	0.2%
[8]	Hilbert FIR	31 taps	FPGA	40 Hz - 960 Hz	-
[9]	Hilbert FIR	31 taps	CMOS .35μm	0.5 Hz - 2048 Hz	-
[10]	FFT	-	Microcontroller	50 Hz	0.812%
[11]	FFT	-	FPGA	0 - 50MHz	0.0309%
[12]	Wavelet	10 coefficients	-	46.93 Hz - 3626.7 Hz	0.0099%
[13]	Walsh Functions	-	-	50 Hz - 550 Hz	3.068%
[14]	ANF	-	-	50 Hz - 250 Hz	0.000444%

3.2 Reactive Power Measurement

To begin presenting the measurement procedures used in this section, we need to specify a definition of the power quantities to be used. In this work, the definitions presented by Budeanu [36] for active and reactive power under non-sinusoidal conditions were chosen due to simplicity and wide use in others reactive power measurement works. These definitions were used for a long time, and it was defined in the Dictionary of Standards IEEE 1459-2000 [37], but it was strongly objected by Czarnecki [38], since the relationship between Budeanu's reactive power definition and line loss were not straightforward. It resulted in taking down Budeanu's definition from the IEEE 1459-2010 version [39], but new studies done by Willems [40] and Jeltsema [41] revisited the definitions and showed the usefulness of Budeanu's definition. Moreover, the use of Budeanu's definition for billing was not questioned

by any of the works, and it is the main focus of this dissertation. Thus, his definitions will be used throughout this work.

According to Budeanu [36], the definition of active power and reactive power under non-sinusoidal conditions are, respectively,

$$P = \sum_{k=1}^{\infty} P_k = \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k) \tag{3.1}$$

and

$$Q = \sum_{k=1}^{\infty} Q_k = \sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k) \tag{3.2}$$

where P_k and Q_k are, respectively, the RMS values of the kth active and reactive power harmonic component, V_k and I_k are the RMS values of the kth voltage and current harmonic component, and φ_k is the phase difference between each of them. Based on these definitions and the measurement method developed by Hao [7], we will present the reactive power measurement theory using an ideal Hilbert transformer and a real IIR Hilbert transformer with a phase error around the 90 degrees phase shift, to show the effects of this error in the measurement precision.

3.2.1 Using an ideal Hilbert transformer

The measurement system using a Hilbert transformer is shown in Fig. 3.1.

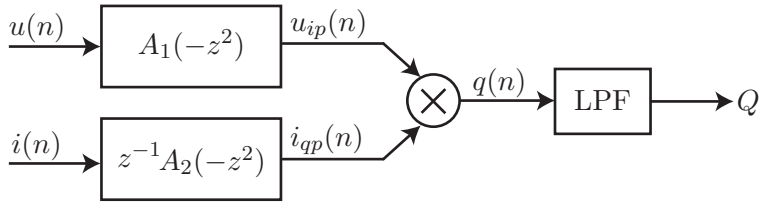


Figure 3.1: Reactive power measurement system using one Hilbert transformer.

Consider the sampled voltage signal expressed by its Fourier series:

$$u(n) = \sum_{k=1}^{N} \sqrt{2} V_k \sin\left(\omega_k n + \phi_k\right) \tag{3.3}$$

$$\omega_k = 2\pi k f_1 T_s \tag{3.4}$$

where V_k is the RMS voltage value of the kth harmonic, f_1 is the fundamental frequency, T_s is the sampling period and ϕ_k is the phase of the kth harmonic. The sampled current of the system should present same characteristics and is represented by

$$i(n) = \sum_{k=1}^{N} \sqrt{2} I_k \sin\left(\omega_k n + \phi_k - \varphi_k\right) \tag{3.5}$$

where I_k is the RMS current value of the kth harmonic and φ_k is the phase difference between the kth voltage and current harmonic.

As it can be seen in Fig. 3.1, the voltage signal goes through the all-pass filter $A_1(-z^2)$ and the current signal goes through the path with the all-pass transfer function $z^{-1}A_2(-z^2)$ which guarantees a 90 degrees phase shift between current and voltage signal. If the phase shift introduced by $A_1(-z^2)$ is $\theta_1(k)$ for the kth harmonic component, then the signals $u_{ip}(n)$ and $i_{qp}(n)$ can be represented by

$$u_{ip}(n) = \sum_{k=1}^{N} \sqrt{2} V_k \sin\left(\omega_k n + \phi_k + \theta_1(k)\right) \tag{3.6}$$

and

$$\begin{aligned} i_{qp}(n) &= \sum_{k=1}^{N} \sqrt{2} I_k \sin\left(\omega_k n + \phi_k + \theta_1(k) + \frac{\pi}{2} - \varphi_k\right) \\ &= \sum_{k=1}^{N} \sqrt{2} I_k \cos\left(\omega_k n + \phi_k + \theta_1(k) - \varphi_k\right) \end{aligned} \tag{3.7}$$

Both signals are then multiplied, and after applying the distributing property of the summations, we obtain

$$\begin{aligned} q(n) = \sum_{k=1}^{N} \sum_{l=1}^{N} 2 V_k I_l \sin\left(\omega_k n + \phi_k + \theta_1(k)\right) \times \\ \cos\left(\omega_l n + \phi_l + \theta_1(l) - \varphi_l\right) \end{aligned} \tag{3.8}$$

which can be simplified to

$$\begin{aligned} q(n) = \sum_{k=1}^{N} \sum_{l=1}^{N} V_k I_l \left[\sin\left(\omega_{k+l} n + \phi_k + \phi_l + \theta_1(k) + \theta_1(l) - \varphi_l\right)\right. \\ \left. + \sin\left(\omega_{k-l} n + \phi_k - \phi_l + \theta_1(k) - \theta_1(l) + \varphi_l\right)\right] \end{aligned} \tag{3.9}$$

There will be $2N + 1$ harmonic components in $q(n)$, so it can be represented by a signal with a form

$$q(n) = q_0 + \sum_{m=1}^{2N} A_m \sin\left(\omega_m n + \phi_m\right) \tag{3.10}$$

To calculate each component of $q(n)$ is not a simple task and also not relevant for the measurement. The value of the DC component of $q(n)$, q_o, is obtained when $k = l$ in (3.9) and is given by

$$q_0 = \sum_{k=1}^{N} V_k I_k \sin\left(\varphi_k\right) \tag{3.11}$$

which can be extracted from $q(n)$ by using a low-pass filter with cutoff frequency below the fundamental frequency. The final result of the system, Q, is the given by

$$Q = q_0 = \sum_{k=1}^{N} V_k I_k \sin(\varphi_k) \tag{3.12}$$

which is close to the definition in (3.2), except for the limited number of harmonics. Since the bandwidth of the Hilbert transformer can be designed to be as wide as necessary to include the main harmonics recommended by the standards of each country, this method proves to be an efficient way to measure the reactive power.

3.2.2 Using a real Hilbert transformer

Since building a perfect 90 degree phase shifter is not achievable by real circuits, we consider now that the Hilbert transformer has a small phase error ε_k around the $\frac{\pi}{2}$ phase shift. The current signal after passing through the phase-shifting network is now expressed by

$$\begin{aligned} i_{qp}(n) &= \sum_{k=1}^{N} \sqrt{2} I_k \sin\left(\omega_k n + \phi_k + \theta_1(k) - \varphi_k + \frac{\pi}{2} + \varepsilon_k\right) \\ &= \sum_{k=1}^{N} \sqrt{2} I_k \cos\left(\omega_k n + \phi_k + \theta_1(k) - \varphi_k + \varepsilon_k\right) \end{aligned} \tag{3.13}$$

The same process used through equations (3.6)-(3.11) can be used, and it is easy to see that the final measurement result with an phase error on the Hilbert transformer will be

$$Q = \sum_{k=1}^{N} V_k I_k \sin\left(\varphi_k - \varepsilon_k\right) \tag{3.14}$$

which can be splitted into two parts

$$Q = \sum_{k=1}^{N} V_k I_k \sin(\varphi_k)\cos(\varepsilon_k) - \sum_{k=1}^{N} V_k I_k \cos(\varphi_k)\sin(\varepsilon_k) \tag{3.15}$$

and using the definitions from (3.1) and (3.2) we simplify it to

$$Q = \sum_{k=1}^{N} Q_k \cos(\varepsilon_k) - \sum_{k=1}^{N} P_k \sin(\varepsilon_k) \tag{3.16}$$

Since the phase error is small, both sine and cosine can be expanded into Taylor series, obtaining

$$Q \approx \sum_{k=1}^{N} Q_k \left(1 - \frac{1}{2}\varepsilon_k^2\right) - \sum_{k=1}^{N} P_k \varepsilon_k. \tag{3.17}$$

The result from (3.17) has a linear and a quadratic term of the phase error and since the error is small, the linear term dominates the measurement error. Thus, to obtain a high precision in the measurement using this method, the Hilbert transform phase error has to be very small, which is achieved by using high order filters. In digital applications, building high order filters is straight-forward, but in analog circuits, because of the process parameters variations, which causes mismatch between transistors and process gradient, higher-order filters tend to have higher statistical variation in its response.

To show the effect of parameters variation in the phase error, we compared two Hilbert transformers with different transfer function order length. The first Hilbert transformer, referred as HT1, was implemented in [27] and it used a 7^{th} order transfer function, which means 3 structurally all-pass sections (SAPS). The all-pass transfer functions are

$$A_1(-z^2) = \frac{-z^{-2} + 0.1907}{1 - 0.1907z^{-2}} \times \frac{-z^{-2} + 0.8607}{1 - 0.8607z^{-2}} \tag{3.18}$$

and

$$A_2(-z^2) = \frac{-z^{-2} + 0.5531}{1 - 0.5531z^{-2}}. \tag{3.19}$$

The second Hilbert transformer, referred as HT2, was implemented in [7] and it used a 13^{th} order transfer function, which means 6 SAPS. The all-pass transfer functions are

$$A_1(-z^2) = \frac{-z^{-2} + 0.80000}{1 - 0.80000z^{-2}} \times \frac{-z^{-2} + 0.44868}{1 - 0.44868z^{-2}} \times \frac{-z^{-2} + 0.06820}{1 - 0.06820z^{-2}} \tag{3.20}$$

and

$$A_2(-z^2) = \frac{-z^{-2} + 0.24027}{1 - 0.24027z^{-2}} \times \frac{-z^{-2} + 0.64112}{1 - 0.64112z^{-2}} \times \frac{-z^{-2} + 0.93448}{1 - 0.93448z^{-2}}. \tag{3.21}$$

With these two Hilbert transformers, we performed a Monte Carlo analysis using MATLAB, adopting a 1% variation of each coefficient values of the SAPS. The simulation result is presented in Fig 3.2 and it shows the phase error around the 90 degree phase shift.

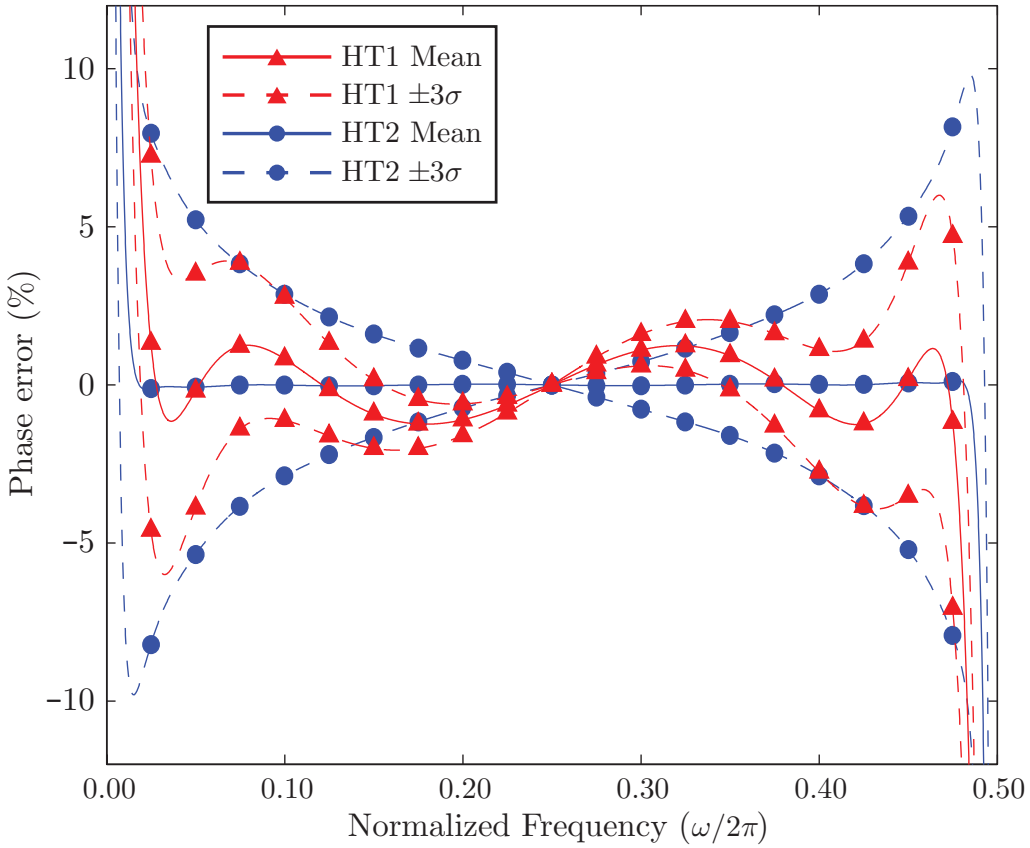


Figure 3.2: Phase error around the 90° phase shift for different Hilbert transformers. Monte Carlo analysis adopting a 1% variation on each structurally all-pass section coefficient.

From the simulation result, one can see that the mean phase error of HT2 is much smaller than the HT1, but its standard deviation is greater then HT1. This means that, even though a high-order transfer function is used to build the Hilbert transformer, the phase error might not be smaller than a low-order transfer function, since analog applications are subject to mismatch between transistors and process parameters variations. Thus, high-order Hilbert transformers are not a reliable technique to reduce measurement error on analog systems.

3.2.3 Measurement Method Using Two Hilbert Transformers

To overcome the linear dependency of the phase error in the measurement response, a new measurement technique was presented in [42]. This technique consist in using two copies of the same filter to cancel the linear term of (3.17). Even though it basically doubles the overall order of the system, since it cancel the linear term, the effect of the phase error in the measurement is highly reduced, lowering the constraints for the design of the Hilbert transformer, therefore lowering the order of each filter. The technique is shown in Fig. 3.3.

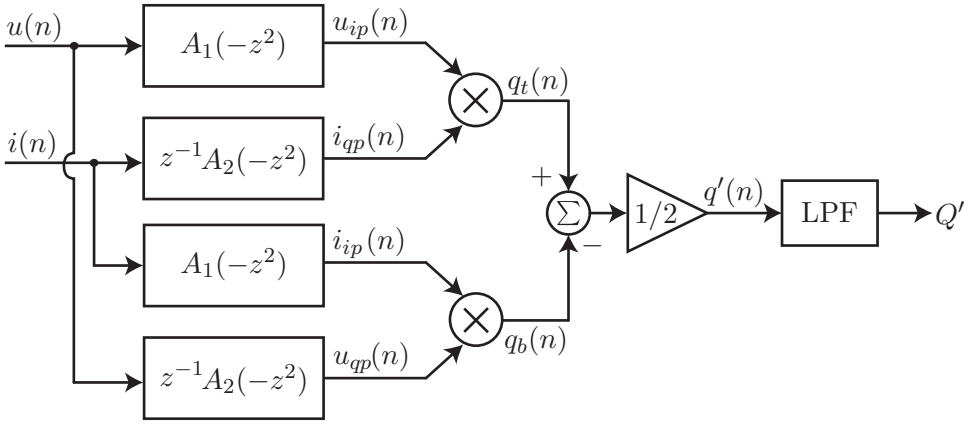


Figure 3.3: Reactive Power measurement using two Hilbert transformers.

It works as follows: the top transformer has the voltage signal in-phase and the current signal in quadrature phase, with their values defined by (3.6) and (3.13) respectively. The bottom transformer has exactly the opposite, the current signal in-phase, described as

$$i_{ip}(n) = \sum_{k=1}^{N} \sqrt{2} I_k \sin\left(\omega_k n + \phi_k - \varphi_k + \theta_1(k)\right) \tag{3.22}$$

and the voltage signal in quadrature-phase, which can be described as

$$\begin{aligned} u_{qp}(n) &= \sum_{k=1}^{N} \sqrt{2} V_k \sin\left(\omega_k n + \phi_k + \theta_1(k) + \frac{\pi}{2} + \varepsilon_k\right) \\ &= \sum_{k=1}^{N} \sqrt{2} V_k \cos\left(\omega_k n + \phi_k + \theta_1(k) + \varepsilon_k\right) \end{aligned} \tag{3.23}$$

The procedure described through equations (3.6)-(3.11) can be used again to obtain the DC components of $q_t(n)$ and $q_b(n)$, which are given by

$$q_{t0} = \sum_{k=1}^{N} V_k I_k \sin\left(\varphi_k - \varepsilon_k\right) \tag{3.24}$$

$$q_{b0} = \sum_{k=1}^{N} V_k I_k \sin\left(-\varphi_k - \varepsilon_k\right) \tag{3.25}$$

Similarly from equation (3.10), the value of $q'(n)$ from Fig. 3.3 have also $2N+1$ harmonic components and can be described as

$$q'(n) = q'_0 + \sum_{m=1}^{2N} A'_m \sin\left(\omega_k n + \phi'_m\right) \tag{3.26}$$

where the DC component, q'_0 is given by

$$\begin{aligned} q'_0 &= \frac{1}{2}[q_{t0} - q_{b0}] \\ &= \frac{1}{2}\sum_{k=1}^{N} V_k I_k \left[\sin\left(\varphi_k - \varepsilon_k\right) - \sin\left(-\varphi_k - \varepsilon_k\right)\right] \\ &= \sum_{k=1}^{N} V_k I_k \sin\left(\varphi_k\right)\cos\left(\varepsilon_k\right) \end{aligned} \tag{3.27}$$

After the Low-Pass filter with cutoff below fundamental frequency, the measurement result is given by

$$Q' = q'_0 = \sum_{k=1}^{N} Q_k \cos\left(\varepsilon_k\right) \tag{3.28}$$

and after Taylor expansion, it is approximated by

$$Q' \approx \sum_{k=1}^{N} Q_k \left(1 - \frac{1}{2}\varepsilon_k^2\right) \tag{3.29}$$

Comparing the result from (3.29) with the one from (3.17), it is clear that the measurement error is much smaller in (3.29) since the linear term is cancelled. The drawback is the need to implement two versions of the same Hilbert transformer.

As mentioned before, this result has a big advantage for analog design, which are lower constraints to build each transformer, making both top and bottom transformers smaller filters with a lower phase error statistical variation. On the other hand, this method requires a perfect matching between top and bottom transformers, which is not possible to guarantee because of mismatch and parameters variation. So, in order to obtain a perfect cancellation of the linear term in the measurement error, some structural changes into the switched-current structural all-pass section (SI-SAPS) are necessary, and they will be proposed in the next section.

3.3 Proposed Method

To achieve perfect matching between top and bottom HT, some changes on the SI-SAPS circuit of Fig. 2.5 are proposed. For clarity, the previous figure is repeated here.

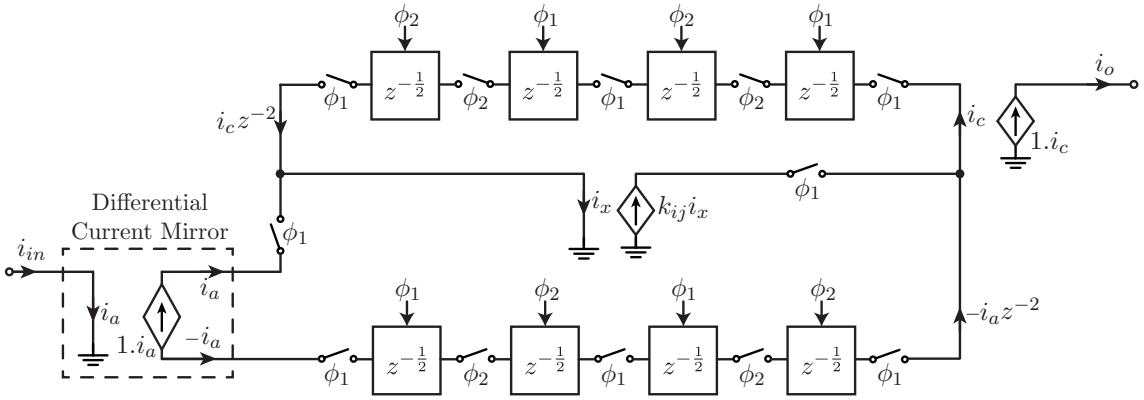


Figure 3.4: Block diagram of a one-coefficient switched-current structurally all-pass section.

One can see that the section is realized by the current mirror in the middle, where both input currents i_a and $i_c z^{-2}$ and output current $k_{ij} i_x$ are only required during phase one. This means that during phase two, the current mirror is idle: there is no current going in or coming out of it. Thus, the same current mirror can be shared between both top and bottom all-pass transfer functions, therefore guaranteeing a perfect matching between both HT. The same idea can be used for the differential current mirror block. A block diagram that implements the all-pass section with these shared blocks is presented in Fig. 3.5.

Now, there are two inputs and two outputs for each all-pass section, one to process the current signal and the other to process the voltage signal. During the phase one, the top part of the circuit is using the current mirror, so that all switches connecting the current mirror to the memory cells are controlled by phase one. During the phase two, all the switches that connect the current mirror to the top part are open, disconnecting it from the top memory cells. The switches connecting the current mirror to the bottom memory cells are now closed and then it can be used by the bottom part.

A chain of cascaded sections of circuits from Fig. 3.5 is used to implement the complete all-pass transfer function as shown in Fig. 3.6. Notice that the input and output port t is the one connected to the top all-pass section, and the input and output port b is the one connected to the bottom section.

One problem of sharing the coefficient is that the bottom all-pass is delayed from the top all-pass by a half-delay ($z^{-1/2}$). To correct it, a half-unit delay have to be introduced in the top path. Also, since both signals are half-unit delayed, the output

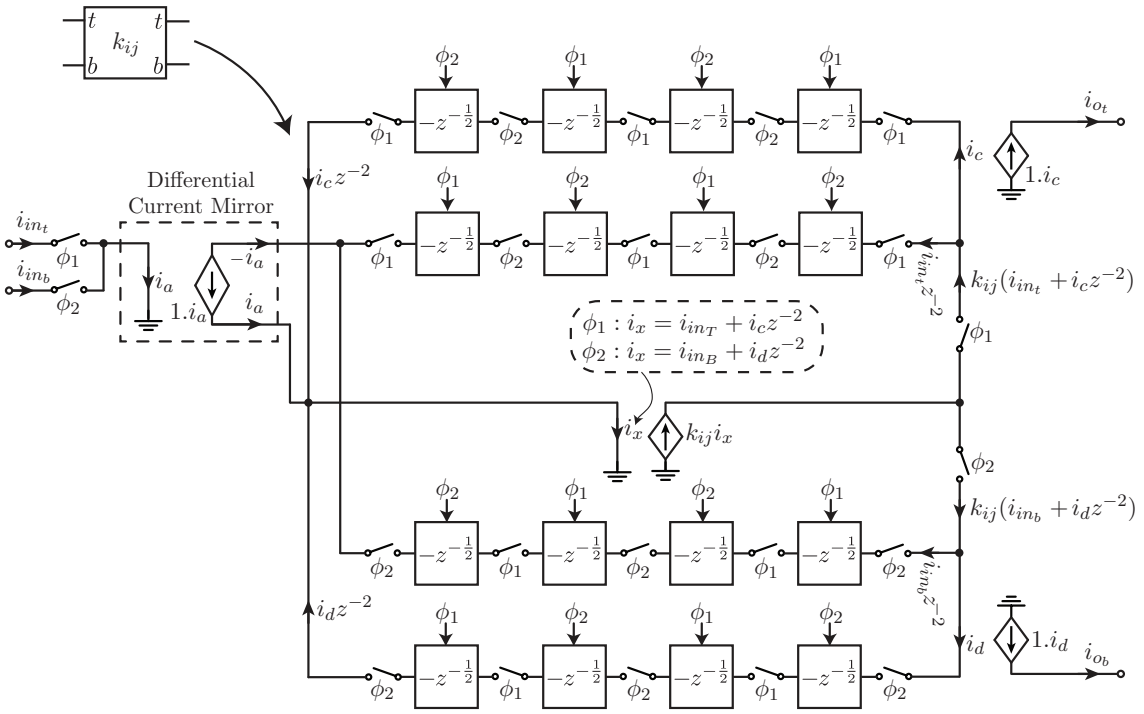


Figure 3.5: Block diagram of two switched-current structurally all-pass sections with shared coefficients.

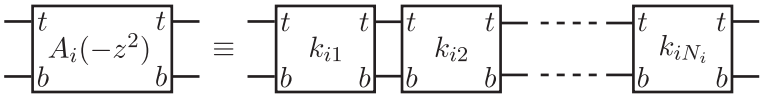


Figure 3.6: Representation of the all-pass transfer function with a cascade of shared coefficient SAPS.

signal would be delivered on phase two. To avoid this issue and balance both top and bottom paths, another half-unit delay is introduced in every path, leading to the final measurement system presented in Fig. 3.7. Since every path is delayed equally, there is no change in the final measurement result from (3.28). Also, since now the coefficient sharing circuits are being used, the perfect matching between top and bottom HT is now guaranteed and the linear term is canceled.

3.4 Simulation Results

To verify the performance of the proposed method we executed a behavioral simulation using MATLAB comparing four different measurement systems. The first system, referred here as System 1, uses the 'one Hilbert transformer' method described in Fig. 3.1, where the all-pass transfer functions have lower order, therefore it has less structurally all-pass sections (SAPS). For System 1 it was chosen the transfer function presented by Petraglia [27]. The transfer function was used in the last section to simulate the phase error, and they are defined by (3.18) and (3.19)

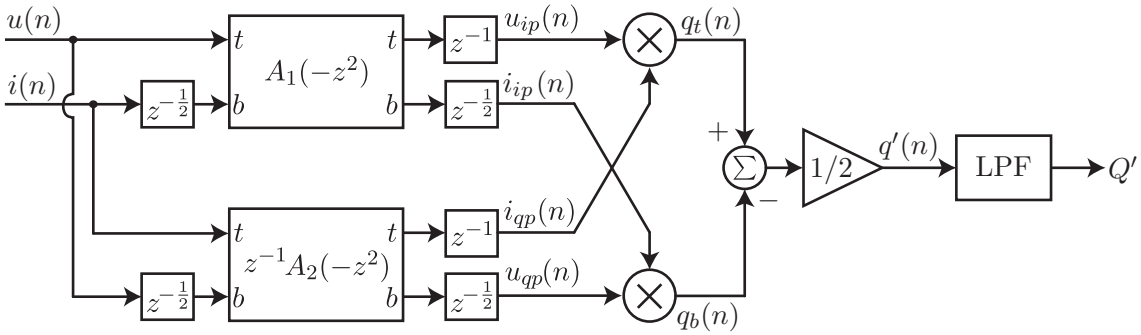


Figure 3.7: Final measurement system proposed in this work.

The second system, referred as System 2, also uses the same method from System 1, which is the 'one Hilbert transformer' method from Fig. 3.1, However, for System 2, the all-pass transfer functions have a higher order, therefore it has more SAPS. The Hilbert transformer implemented in this system used the transfer function presented by Hao [7] and also used in the last section, defined by (3.20) and (3.21).

The third system, referred as System 3, uses the 'two Hilbert transformers' method from Fig. 3.3, and the transfer function of its Hilbert transformers is the same as System 1. However, since two transformers are required, the overall system uses 6 SAPS. Also System 3 does not use the coefficient sharing structure we present in this Chapter, therefore both top and bottom Hilbert transformers are implemented separately and each coefficient are subject to different mismatch.

The fourth system, referred as System 4, also uses the 'two Hilbert transformers' method, but in this case the SAPS with coefficient sharing are used, therefore guaranteeing same coefficient variation for both top and bottom Hilbert transformers. Thus, System 4 implements the method from Fig. 3.7. The transfer functions used in System 4 are the ones from System 1, and since two version of the transformer are used, the overall system has 6 SAPS. Table 3.2 summarizes the specifications of each system.

Table 3.2: Summary of systems specifications.

	Measurement Method	Filter Order	SAPS with Shared Coefficients
System 1	One Hilbert transformer (Fig. 3.1)	3^{rd} order	-
System 2	One Hilbert transformer (Fig. 3.1)	6^{th} order	-
System 3	Two Hilbert transformers (Fig. 3.3)	2×3^{rd} order	No
System 4	Two Hilbert transformers (Fig. 3.7)	2×3^{rd} order	Yes

In order to test their performances against the non-ideal effects of analog systems, we need to specify a test input and observe the reactive power measured by each system. These input signals were chosen based on a table of maximum distortion allowed from the Brazilian National Electrical Energy Agency (ANEEL) [3].

For simplicity, the current values were set with same values as the voltage components. The phase angle was determined in a random manner, since it is just for exemplification. These values are presented in Table 3.3. The ideal reactive power for each component were calculated and it is also presented on Table 3.3.

Table 3.3: Input Signal Characteristics.

Harmonic Component	RMS Voltage V_k (V)	RMS Current I_k (A)	Phase Angle φ_k (deg)	Ideal Reactive Power Q_k (var)
Fundamental	1	1	15	0.2588190
2^{nd}	$2.5 \cdot 10^{-2}$	$2.5 \cdot 10^{-2}$	20	0.0002137
3^{rd}	$6.5 \cdot 10^{-2}$	$6.5 \cdot 10^{-2}$	10	0.0007336
4^{th}	$1.5 \cdot 10^{-2}$	$1.5 \cdot 10^{-2}$	12	0.0000467
5^{th}	$7.5 \cdot 10^{-2}$	$7.5 \cdot 10^{-2}$	14.5	0.0014083
6^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	17	0.0000292
7^{th}	$6.5 \cdot 10^{-2}$	$6.5 \cdot 10^{-2}$	39	0.0026588
8^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	53	0.0000798
9^{th}	$2 \cdot 10^{-2}$	$2 \cdot 10^{-2}$	10	0.0000694
10^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	5	0.0000087
11^{th}	$4.5 \cdot 10^{-2}$	$4.5 \cdot 10^{-2}$	55	0.0016587
12^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	70	0.0000939
13^{th}	$4 \cdot 10^{-2}$	$4 \cdot 10^{-2}$	15	0.0004141
14^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	22	0.0000374
15^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	43.5	0.0000688
16^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	10	0.0000173
17^{th}	$2.5 \cdot 10^{-2}$	$2.5 \cdot 10^{-2}$	17	0.0001827
18^{th}	$1 \cdot 10^{-2}$	$1 \cdot 10^{-2}$	9	0.0000156
19^{th}	$2 \cdot 10^{-2}$	$2 \cdot 10^{-2}$	10	0.0000694

The final measurement result is the sum of all component's reactive power, resulting in

$$Q_{\text{Ideal}} = 0.2666261 \tag{3.30}$$

To verify the behavior of the proposed method against mismatch and parameters variation, we performed a Monte Carlo simulation where a random Gaussian error with standard deviation of 0.333% ($3\sigma = 1\%$) was introduced in each all-pass section coefficient of the four systems. 1000 runs were performed. In each run, a reactive power reading sample was made for each system, and all this data was organized on the Histograms presented in Fig. 3.8. A better way to compare the measurement accuracy is to obtain the relative error of each sample, defined by (3.31). Histograms with the relative error are presented in Fig. 3.9.

$$\text{Relative Error} = \frac{Q_{\text{Measured}} - Q_{\text{Ideal}}}{Q_{\text{Ideal}}} \tag{3.31}$$

Some key aspects from the results have to be emphasized: comparing System 1 and System 2 histograms, one can see that even though its mean value is closer to

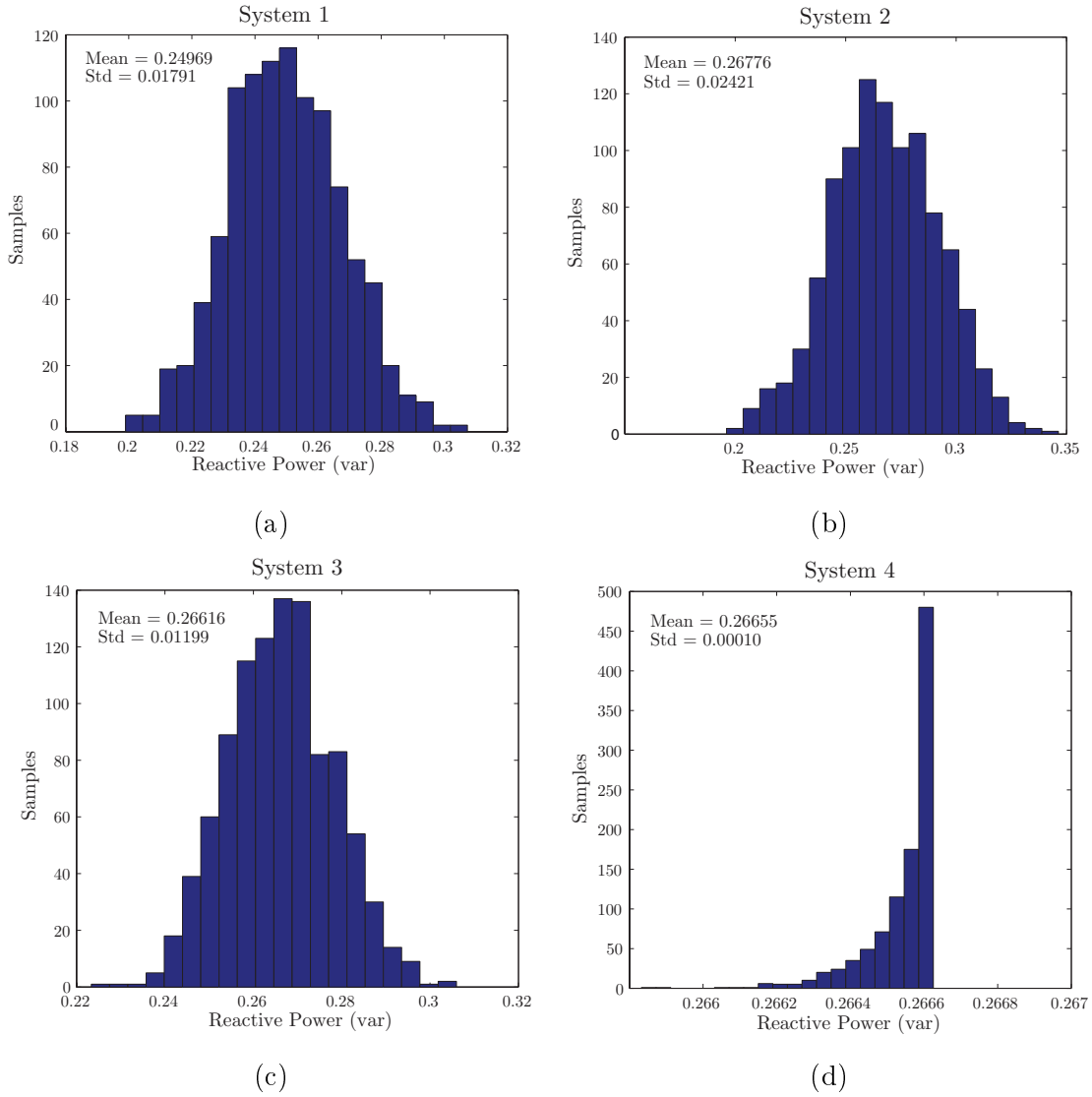


Figure 3.8: Histogram of reactive power measurement for each system.

the ideal value, the standard deviation of the results from System 2 is much bigger than System 1, which shows that increasing the order of the Hilbert transformer is not an effective method to reduce measurement error using analog circuits.

When System 3 is compared with the previous ones, its results are slightly improved, but not enough to justify doubling the order of the filter. Since matching between top and bottom transformers is not guaranteed, the error cancellation does not occur on its full extent. On the other hand, when the matching between top and bottom transformers is guaranteed, as done by the proposed method, the cancellation occurs independent of the coefficient variation.

One way to observe the linear term cancellation on the measurement error of System 4 is to notice that, from (3.29), we obtained a measurement result where $Q \propto \left(1 - \frac{1}{2}\varepsilon_k^2\right)$, which is always less than the effective reactive power value independent of a positive or negative phase error. In System 4 histogram, most of the samples

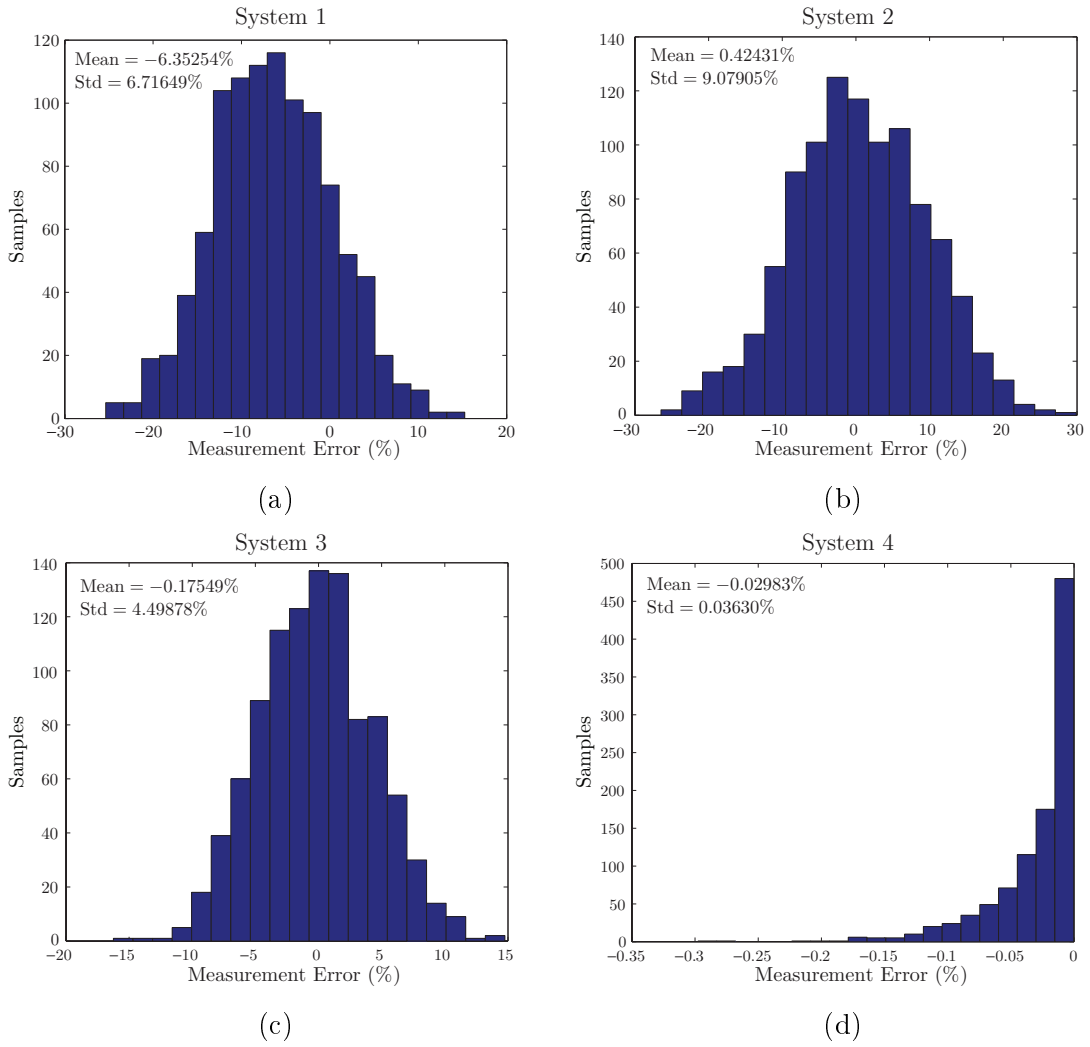


Figure 3.9: Histogram of measurement relative error for each system.

are under the ideal measurement value, which shows the quadratic dependence from (3.29).

These simulations could show the robustness of the proposed method against non-ideal effects during fabrication process. By sharing the current mirror that implements the structural all-pass section coefficient between top and bottom Hilbert transformers, a perfect matching is guaranteed and therefore the phase error linear term dependency is eliminated, even though the coefficient value varies due to non-ideal effects during manufacturing. Not only the mean value is closer to the ideal value when compared with the other systems, but also its standard deviation is extremely smaller. Therefore, the proposed method is more precise and more accurate.

Chapter 4

System Level Design

The Reactive Power Measurement System (RPMS) presented on last chapter can be used on a wide variety of applications, from utility meters to smart home appliances. However, to become a final product for its consumers, it depends on many other components. The goal of this chapter is to derive specifications for RPMS' building blocks, such as current memory cells and coefficient current mirrors, and also allow communication with the other blocks within the product. As an example, an implementation of the RPMS as a part of a utility meter will be presented. However, the design procedure presented here is suitable to any other application.

4.1 Utility Meter

The block diagram for the Utility Meter used as example is shown in Fig. 4.1.

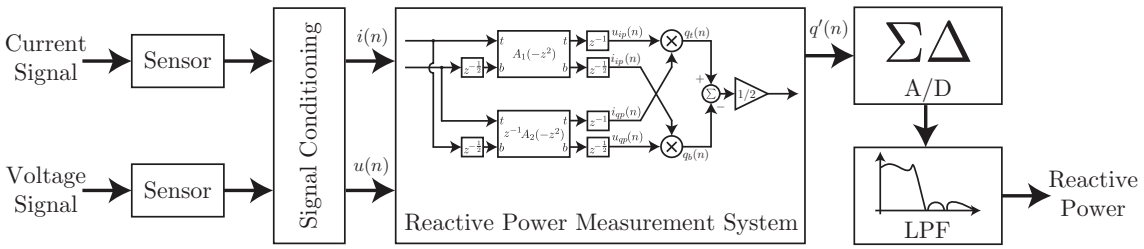


Figure 4.1: Block diagram of the Utility Meter.

The first step of the Utility Meter is to sense both current and voltage from the power grid. The main techniques utilized to sense the voltage is the use of a voltage divider with precision resistors. To sense the current, both Shunt resistor and current transformer can be used. For this example, a Shunt resistor will be consider to sense the current. More details on the sensing techniques can be found in [43].

These two sensing techniques are widely used in utility meters. However, the signal obtained from these sensors are voltage signals. Therefore, a signal condition-

ing step is important to ensure proper compliance with the current requirements of the RPMS. For this specific example, a signal conditioning phase would require at least a Voltage-to-Current converter, and might include a current mirror to adjust current levels to the limits of the RPMS.

Both current signals would be processed by the RPMS and would generate a current signal proportional to the reactive power ($q'(n)$) at the output. To allow reading of the signal, an analog-to-digital converter must transform the current signal into a digital one. For this kind of application, sigma-delta converters are widely used since it delivers the high-precision required by the technical standards at a low-cost and reduced circuit complexity. Naturally, the sigma-delta used in this example must work on current mode.

Finally, the digital signal is filtered by a low-pass filter, obtaining the DC component of $q'(n)$. Even though this filter is a part of the RPMS, it was decided to put it on digital domain, since a sigma-delta modulator also needs a low-pass filter to eliminate the noise shaped into high-frequency. Therefore, instead of implementing two filters, only one filter is implemented that addresses both specifications.

The design of the RPMS will be based on this Utility Meter implementation. However, in this thesis, the focus in only in designing the measurement system part. Therefore, for the next chapters, both current and voltage signals will be assumed to be already conditioned for the RPMS. Also, since the digital part is fundamental to evaluate the final value of the reactive power, it will be simulated on MATLAB.

4.2 Technical Standards and Design Specifications

In order to be approved by regulatory agencies, the utility meter must meet technical standards specifications. The most reliable standards widely used worldwide are provided by the International Electrotechnical Comission (IEC), which has a specific standard for utility meters, the IEC 62053-21:2003.

Since this work is design based on the Brazilian power grid, the rules of Brazilian National Electrical Energy Agency (ANEEL) must be taken into account. These rules are specified under the document Procedures of Electrical Energy Distributions in the National Electric System (PRODIST) [3].

Furthermore, to use design paramenters consistent with reality, the system design procedure used here is based on technical specifications of a real utility meter used by one energy distribution company from Brazil, the *Companhia Paranaense de Energia*, also known as COPEL. From COPEL's utility meter manual [44], we obtain a nominal frequency of 60 Hz, nominal voltage of 120V, and nominal current and maximum current of 2.5 A and 10 A respectively.

Since the RPMS designed is this work is able to measure Budeanu's reactive

power under presence of distortion, one important specification is the number of harmonics to be measured. The PRODIST - Module 8, Section 8.1, Paragraph 4.5 - specifies measurement under distortion to include harmonics at least under the 25^{th} order. Thus, the number of harmonics to measured are 25.

The final specification is obtained through IEC 62053-21:2003, from where Table 4.1 was extracted, which shows the percentage error limits for single phase meters. A shunt resistor sensing utility meter is considered a direct connected meter. Also, for simplicity, we chose to implement a Class 2 meter.

Table 4.1: Percentage error limits (for single-phase meters and polyphase meters with balanced loads)

Value of current		Power Factor	Percentage error limits for meters of class	
for direct connected meters	for transformer operated meters		1	2
$0,05I_n \leq I < 0,1I_n$	$0,02I_n \leq I < 0,05I_n$	1	$\pm 1,5$	$\pm 2,5$
$0,1I_n \leq I \leq I_{max}$	$0,05I_n \leq I \leq I_{max}$	1	$\pm 1,0$	$\pm 2,0$
$0,1I_n \leq I < 0,2I_n$	$0,05I_n \leq I < 0,1I_n$	0,5 inductive 0,8 capacitive	$\pm 1,5$ $\pm 1,5$	$\pm 2,5$ -
$0,2I_n \leq I \leq I_{max}$	$0,1I_n \leq I \leq I_{max}$	0,5 inductive 0,8 capacitive	$\pm 1,0$ $\pm 1,0$	$\pm 2,0$ -
When specially requested by the user: From				
$0,2I_n \leq I \leq I_n$	$0,1I_n \leq I \leq I_n$	0,25 inductive 0,5 capacitive	$\pm 3,5$ $\pm 2,5$	- -

Using the error limits on the table, the maximum dynamic range (DR) for the utility meter can be obtained using the largest and smallest values of the direct connected meters current range column. Considering $I_n = 2.5\ A$ and $I_{max} = 10\ A$, the highest dynamic range is obtained on the second line of the table, given by

$$\text{DR} = \frac{10\ A}{0.1 \cdot 2.5\ A} = 40 : 1 \tag{4.1}$$

Also, in order to be below the $\pm 2\%$ requirement, a percentage error limit of $\pm 1\%$ was specified. A summary of system specifications is given on Table 4.2.

4.3 System Design

Before beginning the system design, is is important to remember that the focus of this work is the RPMS design. Therefore, it is assumed that those specifications of current and voltage will be conditioned to the correct current levels expected by the measurement system. It is a natural process, since the technology used in this thesis for integrated circuit design implementation works with current on the μA level.

Table 4.2: Specification summary for the utility meter.

Parameter	Value
Meter Class	2
Meter Type	Direct Connected
Nominal Frequency (Hz)	60
Nominal Voltage (V)	120
Nominal Current (A)	2.5
Maximum Current (A)	10
Number of Harmonics	25
Dynamic Range	40:1
Percentage Error Limit	$\pm 1\%$

Clarifying this issue, we begin designing the system by obtaining the transfer functions for the Hilbert transformer. Then, transfer functions coefficients will be rounded in order to improve transistor matching. Following the Hilbert transformer design, constraints for its basic building blocks, such as current memory cell and differential current mirror, will be obtained. Finally, some strategies for hardware saving are introduced.

One important tool to help realize this system is the error analysis performed on Appendix C. On this analysis we obtained the effects of offset and gain error of building blocks into the final measurement. This result will help to evaluate some design choices in this section.

4.3.1 Hilbert Transformer Design

The transformer bandwidth is easily obtained using the number of harmonics and the nominal frequency. The highest and lowest frequencies on the bandwidth can be expressed by

$$f_l = 60 \text{ Hz} \tag{4.2}$$

$$f_h = 25 \cdot 60 = 1500 \text{ Hz} \tag{4.3}$$

Since the half-band filter has an equiripple design [15], there is a symmetry around the center of the bandwidth. Thus, the switching frequency is given by

$$f_s = 3120 \text{ Hz} \tag{4.4}$$

The number of structurally all-pass section was a design choice, specified by

$$N_{\text{SAPS}} = 3 \tag{4.5}$$

which gives a overall filter order of 7. The bandwidth, combined with the filter order, is enough to design the half-band filter, and thereby the Hilbert transformer, by using the procedure described in Chapter 2. Using the algorithm proposed in [28], implemented in the Signal Processing Toolbox from MATLAB, we obtain the above values for the transfer functions

$$A_1(-z^2) = \frac{-z^{-2} + 0.215810}{1 - 0.215810z^{-2}} \times \frac{-z^{-2} + 0.881558}{1 - 0.881558z^{-2}}, \tag{4.6}$$

$$A_2(-z^2) = \frac{-z^{-2} + 0.595894}{1 - 0.595894z^{-2}}. \tag{4.7}$$

To simplify, we will express the transfer function by a vector with its coefficients. Thus, we have

$$k_{i1} = \begin{bmatrix} 0.215810 & 0.881558 \end{bmatrix} \tag{4.8}$$

and

$$k_{i2} = \begin{bmatrix} 0.595894 \end{bmatrix} \tag{4.9}$$

4.3.2 Coefficient Rounding

The transfer function coefficients will be implemented in our circuit by current mirrors. However, these coefficients are irrational numbers and therefore, to improve circuit matching, they must be rounded by a rational number [45]. This way, the coefficient is implemented by different ratios of unitary transistors and less mismatch errors can affect the circuit [46].

The chosen criterion when rounding the transfer function coefficients was based on finding the ratio of integers which reduces the average phase error into the fundamental frequency. Since most of the power is located at the fundamental frequency (around 90%), as reported by the ANEEL [3], by reducing the average error at this frequency, we drastically reduce the average phase-error effect into the final measurement result. Using MATLAB, we can develop a Remez-like algorithm to optimize this error. The optimized rounded coefficients are given by

$$\widetilde{k_{i1}} = \begin{bmatrix} 1/5 & 8/9 \end{bmatrix} \tag{4.10}$$

and

$$\widetilde{k_{i2}} = \begin{bmatrix} 3/5 \end{bmatrix} \tag{4.11}$$

Fig. 4.2 compares the filter response with the ideal coefficients and the rounded

coefficients. One can see that the error around 90 degrees at the middle of the bandwidth is higher for the rounded coefficients, but for the fundamental frequency, the error is smaller.

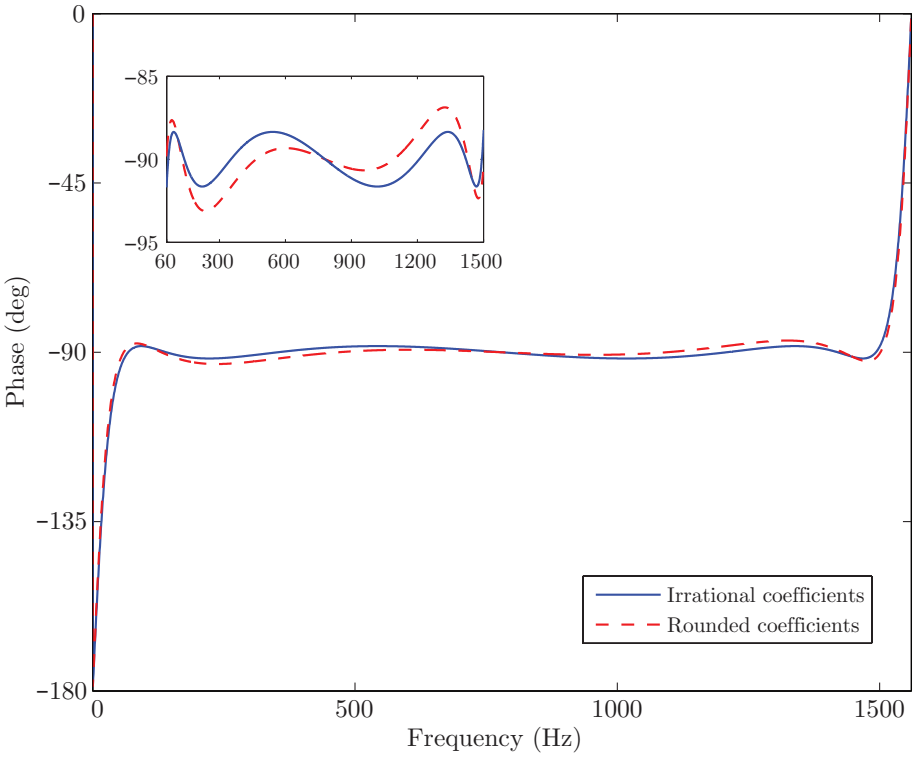


Figure 4.2: Phase comparison between ideal and rounded coefficients.

4.3.3 Building Blocks Constraints

With the design parameters obtained so far, two constraints can be obtained for the current memory cell (CMC). The settling time is directly related to the sampling phase. It is easy to see that the final sampled value must settle within the pulse width of the sampling phase, which corresponds to half of the sampling period $T_s = 1/f_s$. However, as it will be showed in Chapter 6.4, the current multiplier block operates with a different switching scheme, where the sampling phase pulse width corresponds to 1/8 of the sampling period. Therefore, the minimum pulse width is given by

$$\mathrm{PW}_{\mathrm{MIN}} = \frac{1}{8} \cdot T_s \tag{4.12}$$

A good practice is to design the memory cell to settle at 1/4 of the minimum pulse width, thus the settling time can be expressed by

$$\mathrm{ST} = \frac{1}{4} \cdot \frac{1}{8} \cdot T_s = \frac{1}{32 f_s} \approx 10\mu s \tag{4.13}$$

Using the dynamic range, together with the percentage error limit from Table 4.2, a lower-bound for the effective number of bits (ENOB) is given by [43]

$$ENOB \geq \log_2\left(\frac{DR}{0.01}\right) = 11.965 \tag{4.14}$$

For the other blocks, since they are all current mirrors, mismatch and process parameters variation can affect the mirror ratio and introduce a gain error. However, transistor mismatch can be controlled using Pelgrom's rules for its design [47] and process parameters variation can be minimized with a careful layout [48].

The mismatch errors of the coefficient gain block are already minimized due to the system architecture of two Hilbert transformers presented on the last chapter. As a good design practice, the coefficient standard deviation was defined in 1% for 3σ. Thus, we have

$$\sigma(\alpha_{\text{COEF}}) = \frac{0.01}{3} = 3.33 \cdot 10^{-3} \tag{4.15}$$

The phase-error effect on the measurement was derived in (3.29), which states

$$Q' \approx \sum_{k=1}^{N} Q_k \left(1 - \frac{1}{2}\varepsilon_k^2\right) \tag{4.16}$$

and it shows that its effect depends on the input signal. However, the relative error of the measurement is given by

$$E_{rel} = \left|\frac{Q' - Q_{ideal}}{Q_{ideal}}\right| \tag{4.17}$$

where

$$Q_{ideal} = \sum_{k=1}^{N} Q_k \tag{4.18}$$

The relative error can be upper-bound by

$$E_{rel} = \frac{\sum\limits_{k=1}^{N} Q_k \frac{1}{2}\varepsilon_k^2}{\sum\limits_{k=1}^{N} Q_k} \leq \frac{\frac{1}{2}\max(\varepsilon_k)^2 \sum\limits_{k=1}^{N} Q_k}{\sum\limits_{k=1}^{N} Q_k} = \frac{1}{2}\max(\varepsilon_k)^2 \tag{4.19}$$

Thus, the maximum relative error is given by

$$E_{rel_{\text{MAX}}} = \frac{1}{2}\max(\varepsilon_k)^2 \tag{4.20}$$

To observe how coefficient's gain error affects $E_{rel_{\text{MAX}}}$, a Monte Carlo analysis with 10000 samples was performed using MATLAB. For each sample, the maxi-

mum relative error was obtained using (4.20) and displayed into the histogram from Fig. 4.3. The average obtained was $\overline{E_{rel_{\mathrm{MAX}}}} = 0.1530\%$ with a standard deviation of $\sigma(E_{rel_{\mathrm{MAX}}}) = 0.0415\%$. From the histogram is important to see that the relative error is lower than the percentage error limits of $\pm 1\%$, making (4.15) a reasonable constraint.

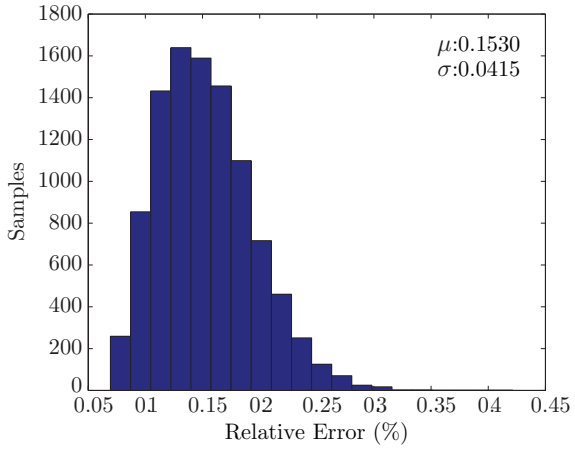


Figure 4.3: Histogram with the maximum relative error of the system obtained with 10000 Monte Carlo simulations.

In Appendix C, it was derived that the gain error of the measurement result is the sum of each differential current mirror and output copy gain errors. This gain error is constant once the integrated circuit is fabricated, so it does not change when the circuit is turned off or with the input signal. Therefore, the gain error of these blocks can be compensated with a simple multiplication by a constant, a straightforward procedure to perform in digital domain.

To obtain the constant value, a simple calibration routine can be used [49], and since these utility meters are mostly installed by professionals, a calibration routine is expected from the energy distribution company. Therefore, a design constraint for both differential current mirror and output copy is obtained using the same principle, setting the standard deviation in 1% for 3σ. Thus, we have

$$\sigma(\alpha_{\mathrm{OC}}) = \sigma(\alpha_{\mathrm{DCM}}) = \frac{0.01}{3} = 3.33 \cdot 10^{-3} \tag{4.21}$$

4.4 Hardware Saving

Saving any hardware is extremely important to reduce area consumption, and by extension, manufacturing costs. The main hardware saving is done with the multiplier. In the RPMS presented before, both multiplications occur at the same phase (ϕ_1). It means that, during the other phase, both multipliers are idle. Using the same principle for the coefficient sharing, the same multiplier can be use to perform

both products, but each one on a different phase. The resulting scheme is presented in Fig. 4.4. Comparing with the previous one, from Fig. 3.5, not only it saves one multiplier, but also three current memory cells.

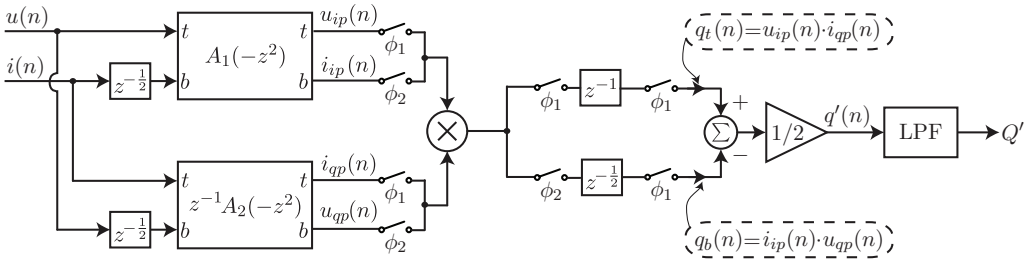
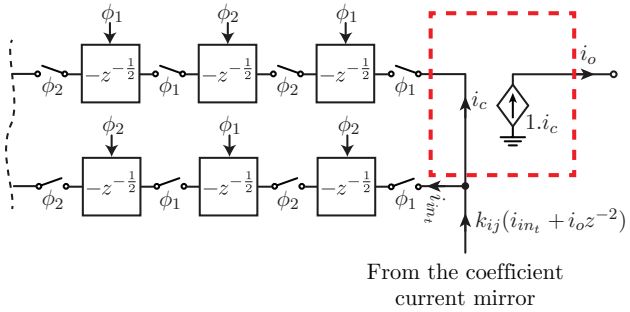
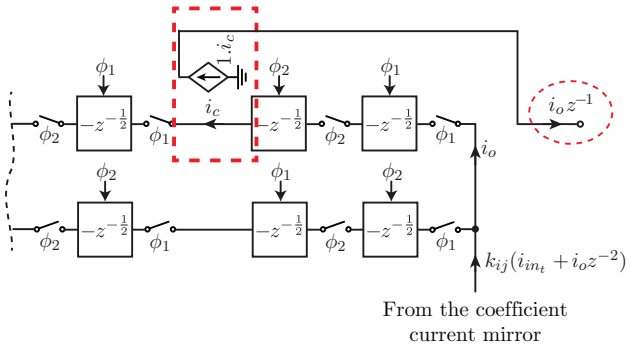


Figure 4.4: Reactive power measurement system with a shared multiplier.

The other hardware saving possibility is to take advantage of the delay chains within the structurally all-pass section to implement the unit delay z^{-1} of the quadrature transfer function ($z^{-1}A_2(-z^2)$). Fig. 4.5a shows a cut from the structurally all-pass section with shared coefficients. Normally, the output copy is taken from the highlighted place, copying the actual output current, i_o. However, if the output is copied two CMCs after, as pictured in Fig. 4.5b, the output obtained is the output current with a unit delay, $i_o z^{-1}$. With this simple change, the area of four CMCs are saved, two for the top path, and two for the bottom path.



(a)



(b)

Figure 4.5: A cut from the structurally all-pass filter copying the output signal (a) and copying a delayed version of the output signal (b).

Chapter 5

Current Memory Cell Design

The current memory cell (CMC) is the main building block of any switched-current (SI) circuit, thus it deserve a special attention on its design. For the last 25 years, many improvements were developed for the first generation and second generation basic memory cells, providing several options of memory cell designs with different pros and cons for each one. One of these techniques is the Zero-Voltage Switching (ZVS), which allows high-performance at high sampling rates. In this chapter, the ZVS principle of operation is discussed and also improvements are proposed. The full design procedure for the memory cell is presented and validated through circuit simulation.

5.1 Principle of Operation

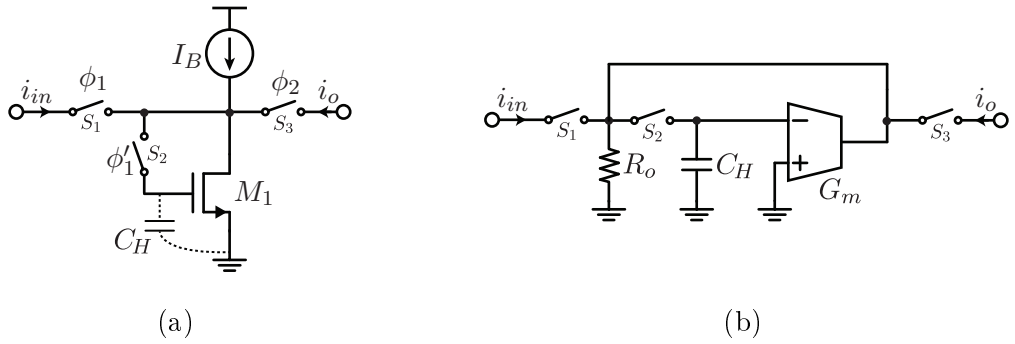
To better understand the operation of the zero-voltage switching (ZVS) current memory cell, a feedback analysis of the basic Second-Generation current memory cell was performed by Sawigun [50], and we repeat this analysis here to explain the need to enhance the loop gain.

5.1.1 Second-Generation current memory cell analysis

The circuit of the second-generation current memory cell (SG-CMC) is presented in Fig. 5.1a. A small-signal model for the SG-CMC, considering channel length modulation effect, is presented on Fig. 5.1b, where R_o is M_1's output resistance, G_m is M_1's transconductance and C_H is its gate-source capacitance.

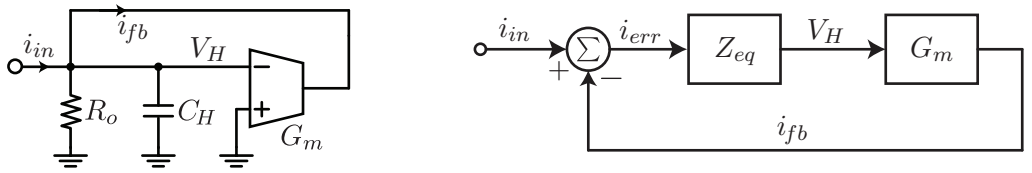
The circuit operation is divided in two phases: the sampling phase (ϕ_1) and the holding phase (ϕ_2). During the sampling phase, switches S_1 and S_2 are closed and switch S_3 is open, leading to the configuration on Fig. 5.2a.

As shown in [50], this system can be represented by the block diagram of Fig. 5.2b. Z_{eq} is the equivalent impedance from the parallel association of the hold



(a) (b)

Figure 5.1: Second-generation current memory cell circuit (a) and small-signal model (b).



(a) (b)

Figure 5.2: Second-generation current memory cell during sampling phase (ϕ_1). Small-signal model (a) and block diagram representation (b).

capacitor C_H and the drain-source resistance R_o, given by

$$Z_{eq} = \frac{R_o}{sC_H R_o + 1} \tag{5.1}$$

The voltage V_H stored into the hold capacitor is defined by the error current i_{err}.

$$V_H = Z_{eq} i_{err} = Z_{eq}(i_{in} - i_{fb}) = Z_{eq}(i_{in} - G_m V_H) \tag{5.2}$$

$$V_H = \frac{Z_{eq} i_{in}}{1 + G_m Z_{eq}} \tag{5.3}$$

However, it is easy to see that the loop gain of the feedback system is given by

$$LG = G_m Z_{eq} = \frac{G_m R_o}{sC_H R_o + 1} \tag{5.4}$$

thus (5.4) can be rewritten as

$$V_H = \frac{Z_{eq} i_{in}}{1 + LG} \tag{5.5}$$

During the holding phase, switch S_3 is now closed and switches S_1 and S_2 are open, breaking the feedback loop and leading to the configuration in Fig. 5.3. The transconductor input is a high-impedance node, thus V_H remains unchanged during

the holding phase (ignoring charge injection effects). The output current i_o is then given by

$$i_o = G_m V_H + \frac{V_o}{R_o} \tag{5.6}$$

$$i_o = i_{in} \frac{LG}{1+LG} + \frac{V_o}{R_o} \tag{5.7}$$

Notice from (5.7) that the output current tends to the input current when the loop gain (LG) tends to infinity and the output voltage (V_o) tends to zero. However, from (5.4), one can see that the loop gain is equal to transistor's intrinsic gain, which is decreasing with new technologies and smaller transistor sizes, leading to an current error transfer. Therefore, enhancing the loop gain would ensure higher transfer accuracy, which is highly desirable on a measurement application.

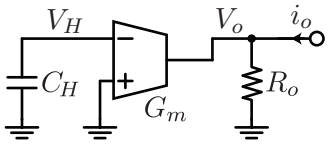


Figure 5.3: Small-signal model of a second-generation current memory cell during holding phase (ϕ_2).

5.1.2 Loop Gain Enhancement

From (5.4), one can see that $LG \propto G_m R_o$. Therefore to enhance the loop gain, the transconductance and/or the output resistance should be increased, and two different approaches can be used for this purpose.

The first approach consists in increasing the output resistance R_o by using cascoded transistors. This method was widely used in the literature [51] due to its simplicity and a further reduction of transfer error since it attenuates the effects of the output voltage in (5.7). However, cascoding transistors is not always possible in low-voltage applications. Moreover, increasing the output resistance does not affect the charge injection directly, thus many implementations dealed with the charge injection issues separately, from which we can highlight the dummy replica [18], S^2I [19] and common-mode feedforward structures [20]. A great summary with many charge injection reduction techniques was presented by Jonsson in his Ph.D. thesis [52].

The second approach to enhance loop gain is to increase the transconductance G_m by cascading transconductance stages. The basic implementation is shown in Fig.5.4. In this case, a voltage amplifier with gain A is introduced before the transconductor,

leading to an effective transconductance of AG_m. However, the amplifier implementation increases the order of the system, which might require compensation to avoid instability. Also, it does not suppress the effects of the output voltage into the current transfer. On the other hand, it is suitable for low-voltage applications and it also supress charge injection effects, as we will show on next section.

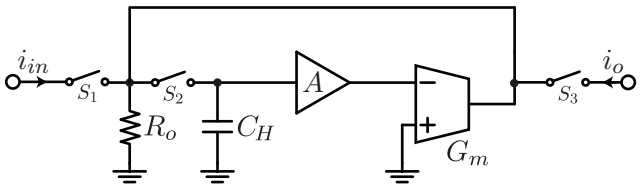


Figure 5.4: Lopp-gain enhancement by introducing a voltage amplifier.

5.1.3 Zero-Voltage Switching

To solve stability issues and improve circuit operation, a new enhancement technique was introduced by Nairn [21]. Instead of using the hold capacitor grounded before the first stage, his technique placed the capacitor across the first amplifier. Also, to keep it stable, the phase inversion performed by the second stage was transferred to the first stage, leading to the configuration in Fig. 5.5. With this technique, a pole splitting is performed, increasing phase margin and stability. However, the great advantage of Nairn's technique is related to charge injection.

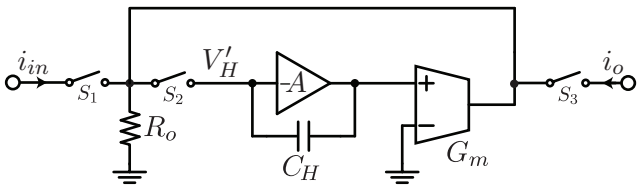


Figure 5.5: Circuit representation of a Zero-Voltage switching current memory cell.

The switch S_2, which injects charge into the hold capacitor, is operated at the voltage V_H, derived in (5.3), which can be simplified to

$$V_H = \frac{i_{in}}{G_m}\left(\frac{1}{1+\frac{1}{LG}}\right) \tag{5.8}$$

After applying Nairn's technique to the memory cell, the new value of the hold voltage, V'_H, is given

$$V'_H = \frac{i_{in}}{AG_m}\left(\frac{1}{1+\frac{1}{LG}}\right) \tag{5.9}$$

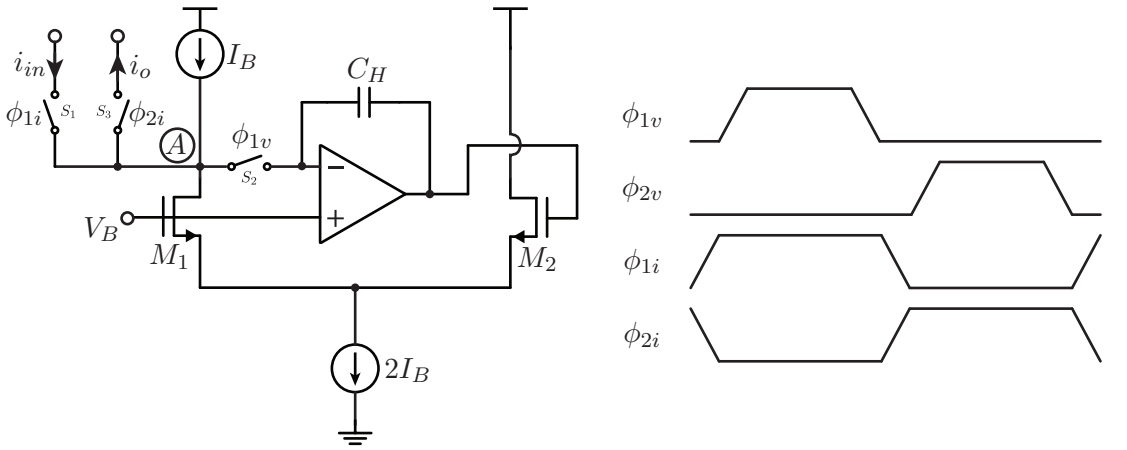
It can be seen that the voltage swing of V'_H is reduced by a factor A, where A is a large number. Therefore, V'_H can be considered a virtual ground. Since the

switch S_2 is operated at this virtual ground, the charge injection becomes signal independent, and therefore, constant. This constant charge injection becomes a voltage offset into the hold capacitor, which can be eliminated from the circuit with a differential structure [53]. However, since some applications are not sensitive to offset, the differential structure is not always needed.

This advantage gives the Zero-Voltage switching (ZVS) memory cell a high-linearity operation at high-sampling rates. Due to this property, his CMC was used throughout this work, along with some operation improvements.

5.1.4 Nairn's Current Memory Cell

The circuit implementation of Nairn's current memory cell, also referred as zero-voltage switching current memory cell (ZVS-CMC), is presented in Fig. 5.6a [21]. The amplifier is implemented with the classic folded cascode OTA, which we will discuss in Section 5.2.5. The transconductance stage, used in the SG-CMC as a single transistor, was replaced by a simple differential pair. This way, the virtual ground can be set at a specific voltage V_B, chosen by the designer.



(a) (b)

Figure 5.6: Circuit implementation of Nairn's current memory cell (a) and its switching sequence (b).

One important issue to address are the control phases. Second generation switched-current circuits have two kinds of switches. Current switches, which are responsible to allow and to stop current flux, requires overlapping control phases to ensure that the switching node is not floating at any given time. Voltage switches, which determine the connection to a capacitive node, require non-overlapping control phases so that the stored voltages are not loss [54]. Throughout this work, current switches are controlled by phases with subscript i and voltage switches are controlled by phases with subscript v. The switching scheme for the ZVS-CMC is shown in Fig. 5.6b. A detailed study of the switching phases is presented in [55].

5.2 Design Improvements

Although the ZVS-CMC represents a great improvement over the basic SG-CMC, it also has some performance issues, such as non-linearity errors and high-power consumption. Over the next section, performance improvements for Nairn's original memory cell are presented.

5.2.1 Dealing with Output Voltage

As seen before, the small signal error associated with the output resistance is given by

$$\varepsilon_{ss} = \frac{V_o}{R_o} \tag{5.10}$$

On a first look, this error seems independent of the input signal. However, it depends on the voltage of the node driven by the memory cell. This voltage can be dependent on the current signal, introducing non-linearity errors.

Notice that, if V_o is somehow kept constant, ε_o only introduces an offset into the output. This offset would sum with charge injection offset, and could even attenuate it depending on charge injection characteristics.

Analyzing the system to be implemented in this work, discussed in Chapter 4, one can see that, in most of the cases, the CMCs load their output on another CMC input. When the prior CMC is on holding phase, loading on the next CMC, the latter one is working on sampling phase, with a virtual ground on its input. It means that, when a CMC drives another CMC, the output voltage V_o is a virtual ground, eliminating the associated error.

The only other block which is driven by CMCs in our system are the coefficient current mirrors. To guarantee this effect in this situation as well, a virtual ground (at V_B) was introduced at the coefficient current mirror's input, as it will be showed in Section 6.2. This way, ε_o is controlled and it does not interfere into memory cell's precision.

However, the virtual ground at the output only cancels the small-signal error into the current. As we know, a virtual ground for small-signal means a constant voltage at the referred node, and for Nairn's cell, this voltage has value V_B.

Using Fig. 5.6a as reference, let node A have the voltage V_A. During sampling phase (ϕ_1), the output resistance of the differential pair drains a current of value $V_A(\phi_1)/R_o$, and the effective input current that goes into the loop is set to

$$i_{eff} = i_{in} - \frac{V_A(\phi_1)}{R_o} \tag{5.11}$$

and this effective current is stored into the hold capacitor. During ϕ_2, the output current for a large loop gain is given by

$$i_o = i_{eff} + \frac{V_A(\phi_2)}{R_o} = i_{in} + \frac{V_A(\phi_2) - V_A(\phi_1)}{R_o} \tag{5.12}$$

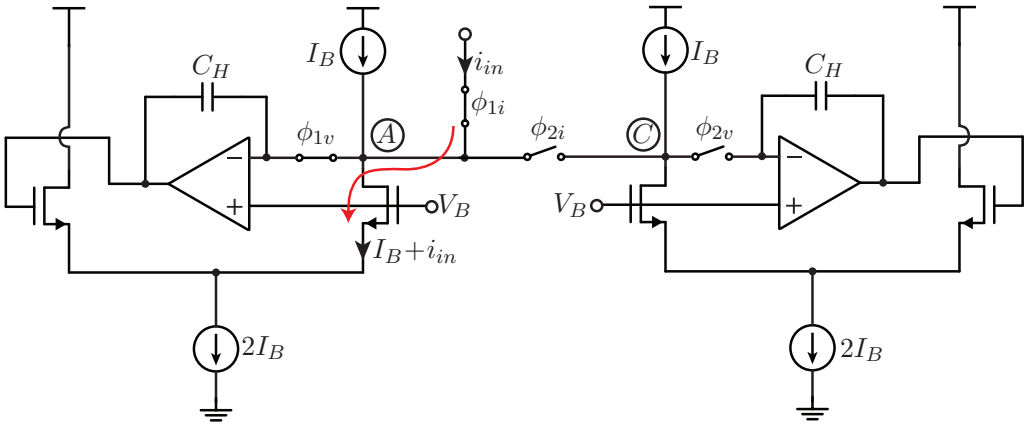
which has a large signal error associated given by

$$\varepsilon_{ls} = \frac{V_A(\phi_2) - V_A(\phi_1)}{R_o} \tag{5.13}$$

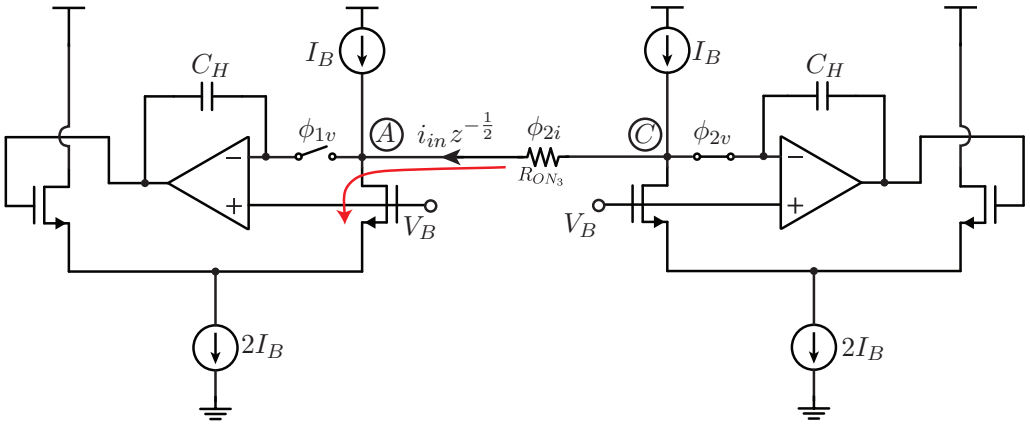
Therefore, not only the output node should have a virtual ground, but also the virtual ground voltage should be the same for both phases.

5.2.2 Output Switch Voltage Drop Compensation

To keep the voltage at differential pair constant for both phases, the output switch voltage drop should be taken into account. Consider two cascade CMCs during two moments. In Fig. 5.7a the CMC on the left is at the sampling phase and at the holding phase at Fig. 5.7b.



(a)



(b)

Figure 5.7: Cascade of two current memory cells, with the left one operating on sampling phase (a) and holding phase (b).

During the sampling phase, the voltage at the input node A is kept at the virtual ground, thus

$$V_A(\phi_1) = V_B. \tag{5.14}$$

However, during holding phase (ϕ_2), the voltage at node C is kept at the same virtual ground, and since there is current flowing through switch S_3, its on-resistance introduces a voltage drop, changing node A potential to

$$V_A(\phi_2) = V_B - i_{in}R_{ON_3}. \tag{5.15}$$

Applying (5.15) to (5.13), it leads to

$$\varepsilon_{ls} = -\frac{i_{in}R_{ON_3}}{R_o} \tag{5.16}$$

which is signal-dependent and can generate errors. To avoid it, a dummy switch was used in both [54] and [56]. The dummy switch is positioned as shown in Fig. 5.8a and changes the voltage at node A during its sampling phase as well, as pictured in Fig. 5.8b. The dummy switch introduces a resistor between amplifier's negative input and CMC's output node, and forces all the current to flow through it by changing the location of switch S_1. Therefore, during ϕ_1 we obtain

$$V_A(\phi_1) = V_B - i_{in}R_{ON_{3d}} \tag{5.17}$$

and by making switch S_{3d} equal to S_3, the large signal error $\varepsilon_{ls} = 0$.

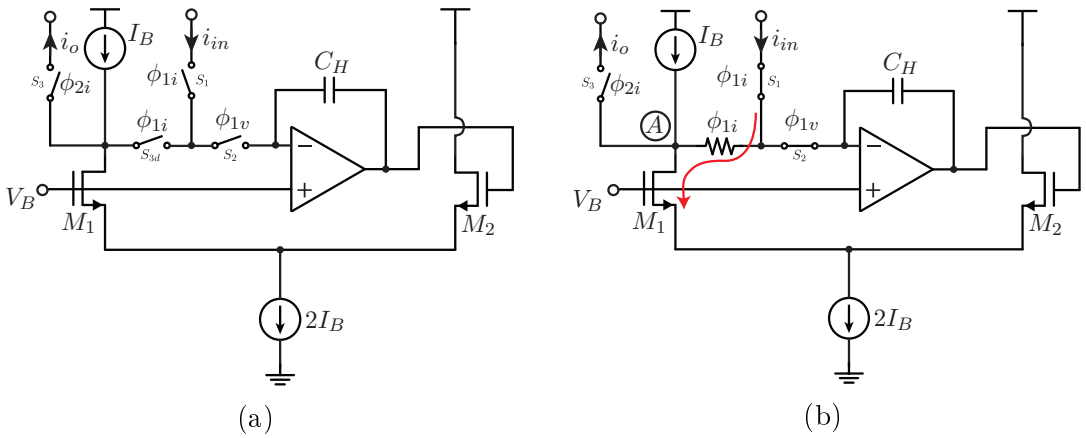


Figure 5.8: Current memory cell with dummy switch S_{3d} (a) and current path during sampling phase (b).

5.2.3 Non-linearity Errors

From section 5.1.3, we deducted that, due to a virtual ground operation of switch S_2, the charge injection into the hold capacitor C_H is constant. This constant charge injection becomes a constant voltage increment into the capacitor stored voltage. Recalling (5.6), the output current after charge injection is given by

$$i_o = G_m \left(V_H + \frac{Q_{ci}}{C_H} \right) \approx i_{in} + i_{err} \tag{5.18}$$

where

$$i_{err} = G_m \frac{Q_{ci}}{C_H} \tag{5.19}$$

and Q_{ci} is the charge injected into C_H. Thus, if G_m is linear, the current error introduced by the charge injection would be an offset. However, on Nairn's CMC, the transconductance G_m is implemented by a simple differential pair (SDP), which is highly non-linear and signal-dependent. Consequently, non-linearity errors are observed into the output current.

As widely known, a simple differential pair has a non-linear relationship between input voltage and output current and its transconductance curve varies as a function of its input voltage value [48, p. 108]. However, due to the feedback loop explained in the last section, this input voltage is set according to the CMC input current. Therefore, the transconductance is signal-dependent, making the current error signal-dependent as well.

For the SDP, the transconductance curve with respect to the CMC input current i_{in} was derived in Appendix B.2 and its given by

$$Gm_{\text{SDP}}(i_{in}) = \sqrt{\beta_1 I_B} \frac{2\sqrt{1 - \left(\frac{i_{in}}{I_B}\right)^2}}{\sqrt{1 + \frac{i_{in}}{I_B}} + \sqrt{1 - \frac{i_{in}}{I_B}}} \tag{5.20}$$

where I_B is the bias current. It is convenient to define the modulation index, m_i, as the ratio between the input current i_{in} and the bias current I_B, i.e. $m_i = i_{in}/I_B$. Applying it to (5.20) we obtain

$$Gm_{\text{SDP}}(m_i) = \sqrt{\beta_1 I_B} \frac{2\sqrt{1 - m_i^2}}{\sqrt{1 + m_i} + \sqrt{1 - m_i}} \tag{5.21}$$

which is plotted in Fig. 5.10. One can notice that, around the middle of the curve, where $m_i = 0$, the transconductance is approximately linear. However, as the modulation index goes far from 0, it starts to become highly non-linear.

Within a certain range of the modulation index, Gm can be broken into an constant average value Gm_{DP} and a ripple $\Delta Gm(m_i)$, which can be applied to (5.19)

leading to

$$i_{err} = \frac{Gm_{\mathrm{DP}} \cdot Q_{ci}}{C_H} + \frac{\Delta Gm(m_i) \cdot Q_{ci}}{C_H} \tag{5.22}$$

which can be upper-bounded by

$$i_{err} \leq i_{off} \pm i_{nl\mathrm{MAX}} \tag{5.23}$$

where

$$i_{off} = \frac{Gm_{\mathrm{DP}} \cdot Q_{ci}}{C_H} \tag{5.24}$$

$$i_{nl\mathrm{MAX}} = \frac{\Delta Gm_{\mathrm{MAX}} \cdot Q_{ci}}{C_H} \tag{5.25}$$

$$\Delta Gm_{\mathrm{MAX}} = \max\{|\Delta Gm(m_i)|\} \tag{5.26}$$

In (5.23), the average transconductance term represents an offset error and the ripple term corresponds to non-linearity errors. Since the maximum ripple is smaller than the average transconductance, it can be written in terms of the average transconductance. By making

$$\delta_n = \frac{\Delta Gm_{\mathrm{MAX}}}{Gm_{DP}} \tag{5.27}$$

equation (5.25) can be rewritten as

$$i_{nl\mathrm{MAX}} = \frac{\delta_n Gm_{\mathrm{DP}} \cdot Q_{ci}}{C_H} \tag{5.28}$$

Therefore, to increase the CMC precision, the transconductance ripple percentage δ_n must be reduced. A simple solution to reduce it is to increase the bias current I_B, limiting the modulation index to a shorter range and thus using a more linear region of the transconductance curve of the simple differential pair. However, this implies an increase in power consumption of the memory cell, reducing its power efficiency. A better solution is to use the high-linearity differential pair (HLDP) of Fig. 5.9, introduced by Krummenacher [57], which presents much less transconductance variation for the same input current range.

Since the derivation of HLDP's transconductance with respect to the modulation index is far more complex, we simulated both SDP and HLDP using SPICE and obtained their transconductance curves to be normalized and compared. Fig. 5.10 compares both structures using their normalized transconductance with respect to the modulation index.

In previous works, m_i was often limited between 0.7 and 0.8 [21, 53, 54]. For m_i

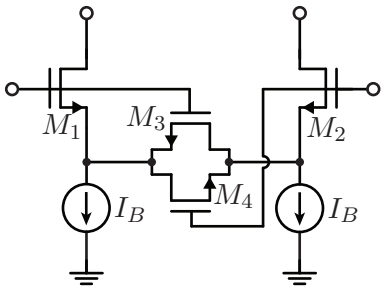


Figure 5.9: High-linearity differential pair.

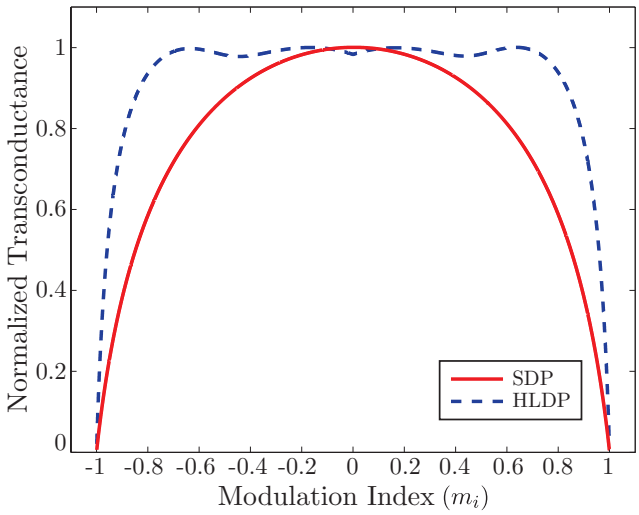


Figure 5.10: Normalized transconductance vs modulation index.

equal to 0.8, the SDP ripple (δ_n) is around 17% whereas the HLDP δ_n is less than 4%, which represents approximately four times less non-linearity error.

5.2.4 Stability

Since the ZVS-CMC has more than two poles, it is important to analyze its stability. The current memory cell circuit with the parasitic components is shown in Fig. 5.11.

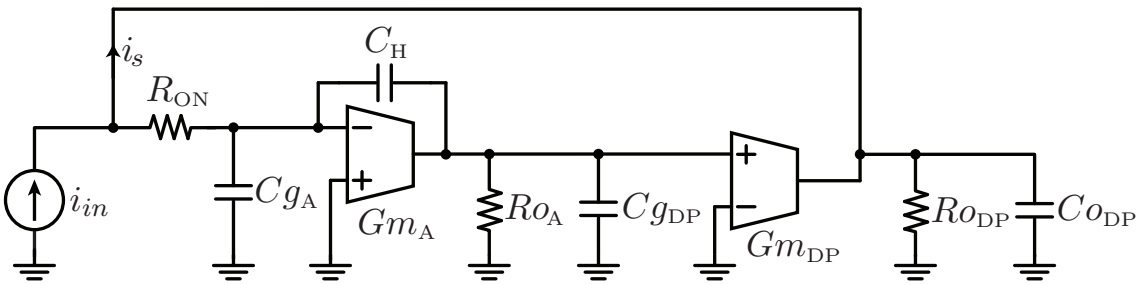


Figure 5.11: Small-signal model of a zero-voltage switching current memory cell with parasitic components.

The transfer function of the system is given by

$$\frac{I_s}{I_{in}}(s) \approx \frac{Gm_{\mathrm{DP}}Gm_{\mathrm{A}}\left(1-\frac{sC_H}{Gm_{\mathrm{A}}}\right)}{s^3R_{\mathrm{ON}}C_HCo_{\mathrm{DP}}(Cg_{\mathrm{DP}}+Cg_{\mathrm{A}})+s^2C_H(Co_{\mathrm{DP}}+Cg_{\mathrm{DP}}+Cg_{\mathrm{A}})+sC_H(Gm_{\mathrm{A}}-Gm_{\mathrm{DP}})+Gm_{\mathrm{DP}}Gm_{\mathrm{A}}} \quad (5.29)$$

where Gm_{A} is the amplifier transconductance, Gm_{DP} is the differential pair transconductance, Ro_{A} is amplifier's output resistance, Ro_{DP} is the differential pair output resistance, R_{ON} is switch S_2 on-resistance, C_H is the hold capacitor and Cg_{A}, Cg_{DP} and Co_{DP} are parasitic capacitances. Since R_{ON} is small, (5.29) can be simplified to

$$\frac{I_s}{I_{in}}(s) \approx \frac{Gm_{\mathrm{DP}}Gm_{\mathrm{A}}\left(1-\frac{sC_H}{Gm_{\mathrm{A}}}\right)}{s^2C_H(Co_{\mathrm{DP}}+Cg_{\mathrm{DP}}+Cg_{\mathrm{A}})+sC_H(Gm_{\mathrm{A}}-Gm_{\mathrm{DP}})+Gm_{\mathrm{DP}}Gm_{\mathrm{A}}} \quad (5.30)$$

Poles and zeros of (5.30) can be approximated to be

$$\omega_{p1} \cong -\frac{Gm_{\mathrm{DP}}Gm_{\mathrm{A}}}{C_H(Gm_{\mathrm{A}}-Gm_{\mathrm{DP}})}, \quad (5.31)$$

$$\omega_{p2} \cong -\frac{Gm_{\mathrm{A}}-Gm_{\mathrm{DP}}}{Co_{\mathrm{DP}}+Cg_{\mathrm{DP}}+Cg_{\mathrm{A}}}, \quad (5.32)$$

$$\omega_z = \frac{Gm_{\mathrm{A}}}{C_H} \quad (5.33)$$

One can see that, in order to be stable, the amplifier transconductance Gm_A must be greater than the differential pair transconductance Gm_{DP}, otherwise ω_{p1} is brought to the right half plane. Also, there is a right hand zero, which can bring the system to instability, depending on the other poles. However, the hold capacitor is responsible for a pole splitting compensation, and it might be enough to keep the system stable [50].

5.2.5 Amplifier and Speed

As said before, the condition for stability is an amplifier transconductance Gm_A greater than the differential pair transconductance Gm_{DP}. Since for MOS transistors $gm \propto \sqrt{I_b}$, the amplifier will be responsible for a high amount of power consumption. To improve the design, instead of using the classical Folded Cascode topology as an high-gain one stage amplifier, as used by Nairn [21] and showed in Fig. 5.12a, we decided to utilize the Recycling Folded Cascode (RFC) topology, which achieves higher transconductance with half of the classical Folded Cascode power consumption [58]. The RFC circuit is presented in Fig. 5.12b.

According to Assaad [58], the main inefficiency of the classical folded cascode,

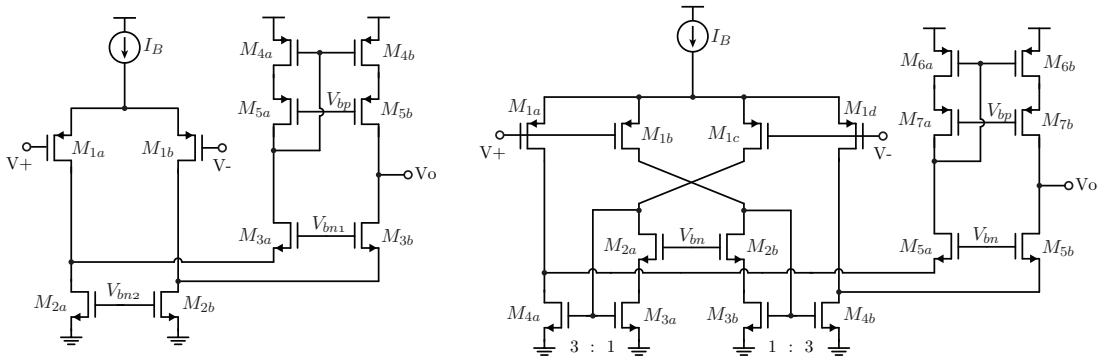


Figure 5.12: Voltage amplifiers topology, Folded Cascode (a) and Recycling Folded Cascode (b).

pictured in Fig. 5.12a, is that the transistors that conduct the most current (M_{2a}] and M_{2b}), are limited to only provide the folding node for the small signal current. To address this inefficiency, the RFC pictured in Fig. 5.12b uses this node also for driving the load, by having a mirror ratio of 1:3.

Considering the stability criteria, not only the RFC has a higher Gm_A when compared to the folded cascode with similar power specs, but also the HLDP has a smaller Gm_{DP} when compared with a SDP with similar specifications, due to its source degeneration. In one hand, stability is easily achieved with the HLDP, allowing a further reduction of the amplifier power's consumption. On the other hand, the differential pair transconductance reduction also implies a speed decrease, since the unit gain frequency tends to

$$\omega_u \cong \frac{Gm_{DP}}{C_H} \tag{5.34}$$

Due to speed reduction, the proposed memory cell is more suitable for lower speed, high precision applications, such as audio sigma-delta modulators and measurement systems.

5.2.6 Proposed Memory Cell

The proposed current memory cell in this work is presented in Fig. 5.13, where the amplifier is implemented by the recycling folded cascode (RFC) circuit on Fig. 5.12b. Since the RFC input transistors are PMOS, to allow a source-bulk connection and reduce amplifier offset [48, p. 23], we also implemented the high-linearity differential pair (HLDP) using PMOS transistors, giving similar common-mode input voltage range for both structures, allowing a better operation.

The current sources in the circuit were implemented using a wide-swing cascode current mirror architecture. Although these current sources come from a separated

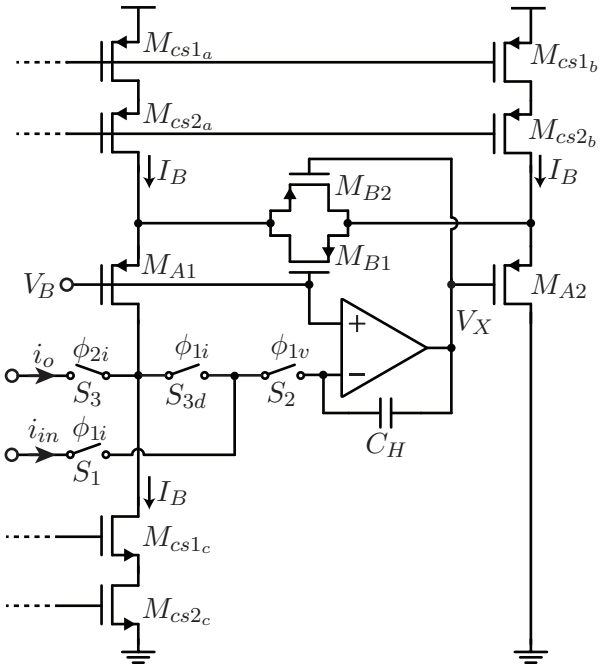


Figure 5.13: Proposed current memory cell, with a high-linearity differential pair implemented with PMOS transistors.

biasing block, we place them in Fig. 5.13 in order to observe the voltage limits for circuit operation. More details on the current sources are given in Section 6.1.

5.3 Circuit Design

The current memory cell implemented in this work will be designed for a CMOS 0.35 μm process, whose process parameters were extracted and displayed in Appendix AP. In this process an asymmetric biasing will be used, with the lowest voltage at ground and $V_{DD} = 3.3$ V. In this section it is presented the design details for the CMC pictured in Fig. 5.13.

5.3.1 Selecting Virtual Ground Voltage

Some key aspects must be taken into account when selecting the virtual ground voltage V_B:

- V_B is the voltage level on which the switch operates. It is interesting to set this voltage closer to ground, to use only a NMOS switch, or closer to V_{DD}, to use only PMOS switch, avoiding the usage of complementary switches.
- The virtual ground voltage works as the common-mode voltage of the amplifier. Therefore, it should be a value within amplifier's input common-mode voltage range.

- The high-linearity differential pair also operates using V_B in one of its terminals. Therefore, for the whole input current range of the CMC, V_B must guarantee correct operation of HLDP.

To find the boundaries for the biasing voltage, we need to observe the operation limits of node V_X on Fig. 5.13. This voltage will be set during the sampling phase (ϕ_1), when the feedback loop is closed. To ensure M_{A2} working in saturation region for every input current, we have

$$V_X \leq V_{DD} - 2|\Delta V_{GS_{cs}}| - |\Delta V_{GS_{A2}}| - |V_{tp_{A2}}| \tag{5.35}$$

where $\Delta V_{GS} = V_{GS} - V_t$. For transistor M_{A2}, there is no lower boundary for V_X. However, since the node V_X is connected to the amplifier's output, its voltage should not lead to amplifier's saturation. Therefore, the amplifier output current mirrors should be kept in saturation region, and V_X lower boundary can be expressed by

$$V_X \geq \Delta V_{GS_4} + \Delta V_{GS_5} \tag{5.36}$$

Considering a maximum ΔV_{GS} of $\pm 250mV$, and applying the threshold voltage on Appendix A with body effect, with a V_{DD} of 3.3 V, we obtain

$$0.5 \leq V_X \leq 1.75 \tag{5.37}$$

As said before, the voltage in node V_X is set according to the input and the differential pair transconductance. We have that

$$V_X - V_B \approx -\frac{i_{in}}{Gm_{\text{DP}}} \tag{5.38}$$

where Gm_{DP} is the average differential pair transconductance, as mentioned in Section 5.2.3. The negative sign is due to amplifier's phase inversion. As it can be seen, $V_X \approx V_B$ when $i_{in} = 0$. Since the input current has symmetric limits, i.e $i_{in\text{MAX}} = -i_{in\text{MIN}}$, V_B should be selected right in the middle of V_X boundaries, to ensure a wider operation of the input current. Hence it was selected

$$V_B = 1.1\text{V} \tag{5.39}$$

5.3.2 Choice of Input Current

The input current is direct responsible for CMC's precision. From Section 5.2.3 we derived the maximum non-linearity current error $i_{nl\text{MAX}}$ in (5.28). The ratio between $i_{nl\text{MAX}}$ and maximum input current $i_{in\text{MAX}}$ defines the effective number of bits (ENOB) of the current memory cell, which is given by

$$\frac{1}{2^{\mathrm{ENOB}}} = \frac{i_{nl\mathrm{MAX}}}{i_{in\mathrm{MAX}}} \tag{5.40}$$

$$\mathrm{ENOB} = \log_2\left(\frac{i_{in\mathrm{MAX}} C_H}{\delta_n G m_{\mathrm{DP}} \cdot Q_{ci}}\right) \tag{5.41}$$

A high precision memory cell also requires a long settling time. If not enough time is given for the memory cell to track the input and settle to the last value, settling errors shall be observed into the output [52]. The settling error must be smaller than the desired number of bit levels of the CMC. In other words, settling time (ST) and ENOB are related by the following

$$e^{-\frac{\mathrm{ST}}{\tau}} = \frac{1}{2^{\mathrm{ENOB}}} \tag{5.42}$$

where τ is the time constant. It can be roughly estimated by the unit-gain frequency, where $\tau \approx 1/\omega_u$, thus (5.42) can be expressed by

$$\omega_u \cdot \mathrm{ST} = \mathrm{ENOB}\ln(2) \tag{5.43}$$

$$\frac{G m_{\mathrm{DP}}}{C_H} = \frac{\mathrm{ENOB}\ln(2)}{\mathrm{ST}} \tag{5.44}$$

Applying (5.44) to (5.41) leads to

$$\mathrm{ENOB} = \log_2\left(\frac{i_{in\mathrm{MAX}} \cdot \mathrm{ST}}{\delta_n \cdot \mathrm{ENOB}\ln(2) \cdot Q_{ci}}\right) \tag{5.45}$$

which after isolating ENOB becomes

$$\mathrm{ENOB} + \log_2(\mathrm{ENOB}) = \log_2\left(\frac{i_{in\mathrm{MAX}} \cdot \mathrm{ST}}{\delta_n \cdot \ln(2) \cdot Q_{ci}}\right) \tag{5.46}$$

On the right hand side of (5.46), the settling time ST is a design constrain from the system design, and was specified in (4.13); the transconductance ripple percentage δ_n is around 4% when a high-linearity differential pair is used; the charge injection Q_{ci} is determined by the process since minimum size switches are used, thus ENOB is a function of the maximum input current since the other terms are fixed.

The charge injected Q_{ci} due to channel charge and clock feedthrough, for its worst case, is approximately [48, p. 418-420]

$$Q_{ci} \approx WLC_{ox}(V_{DD} - V_B - V_{tn}) + V_{DD}WC_{ov} \tag{5.47}$$

where W and L are the switch dimmensions, C_{ox} is the oxide capacitance per unit area, V_B is the virtual ground voltage and C_{ov} is overlap capacitance. Applying

process parameters on Appendix A, we have obtained for a NMOS switch with minimum size the charge

$$Q_{ci} \approx 1.23 \cdot 10^{-15} C \ . \tag{5.48}$$

With charge injection values, ENOB can be plotted with respect to the maximum input current, as showed in Fig. 5.14. One can see that, to achieve 16 bits of resolution, the maximum input current must be greater than 3.569 μA. In order to have relaxed specifications for other blocks, it was selected

$$i_{in\mathrm{MAX}} = 10 \mu A. \tag{5.49}$$

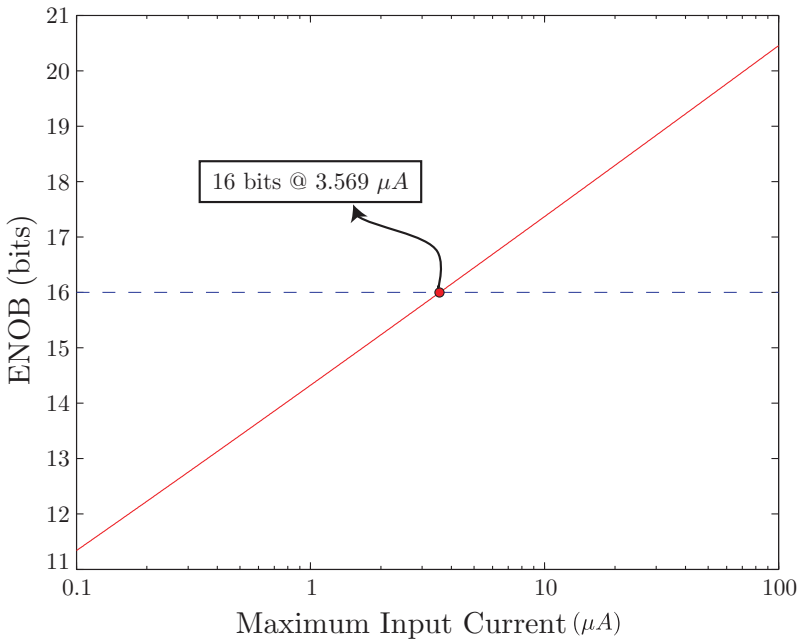


Figure 5.14: Effective number of bits (ENOB) vs maximum input current.

5.3.3 High-Linearity Differential Pair Design

The high-linearity differential pair (HLDP) is composed by transistors M_{A1}, M_{A2}, M_{B1} and M_{B2} in Fig. 5.13. The transistor sizing of the HLDP will be done using circuit simulation with high accuracy transistor models instead of analytic equations. However, some basic constraints must be met for a proper operation of the circuit.

On its original work, Krummenacher [57] performs a deep study of the HLDP, where he concluded that, for high linearity, the best value for ratio β_A/β_B is around 7. The transconductance with $i_{in} = 0$ is given by

$$Gm|_{i_{in}=0} = \frac{gm_A}{1 + \frac{\beta_A}{4\beta_B}} \tag{5.50}$$

which is close to the average transconductance Gm_{DP}.

Applying V_B and $i_{in\text{MAX}}$ definitions on (5.37) and (5.38), the lower bound for the average transconductance Gm_{DP} can be expressed as

$$Gm_{\text{DP}} \geq 16.7\mu A/V \tag{5.51}$$

and to guarantee that condition is satisfied under manufacturing imperfections, the average transconductance was specified around $20\mu A/V$.

The modulation index m_i, defined in section 5.2.3, will be limited in 80%. Therefore, the bias current is defined by

$$I_B = \frac{i_{in\text{MAX}}}{m_{i\text{MAX}}} = 12.5\mu A \tag{5.52}$$

Using Cadence Analog Design Environment, a DC sweep simulation was performed varying the ratio $R = \beta_A/\beta_B$ from 5.5 to 8, with different transistor sizes. The average transconductance must meet the specified value closely and the best fit would presented the smallest ripple. After many configurations, the best values for transistors M_{A1}, M_{A2}, M_{B1} and M_{B2} were obtained and they are presented on Table 5.1. The optimum ratio $R = 6$, which was implemented using parallel transistor to improve matching.

Table 5.1: High-linearity differential pair transistor's dimensions.

Transistor	**Width** (μm)	**Length** (μm)
M_{A1}, M_{A2}	28.8 ($6 \cdot 4.8$)	2.4
M_{B1}, M_{B2}	4.8	2.4

5.3.4 Amplifier Design

The amplifier used in our current memory cell is the Recycled Folded Cascode, mentioned in Section 5.2.5. For clarity, its circuit is repeated in Fig. 5.15. All the equations used to design the amplifier were derived by Assaad in [58]. Transistors with same subscript number have the same ratio.

The first amplifier constrain was set when selecting the virtual ground voltage V_B, which is the output voltage swing. The lower limit for the output swing was specified in (5.36). To have a symmetric output swing, the upper limit is set as

$$V_o \leq V_{DD} - 0.5 = 2.8 \tag{5.53}$$

The amplifier small signal transconductance is given by

$$Gm_{\text{A}} = 4gm_1 \tag{5.54}$$

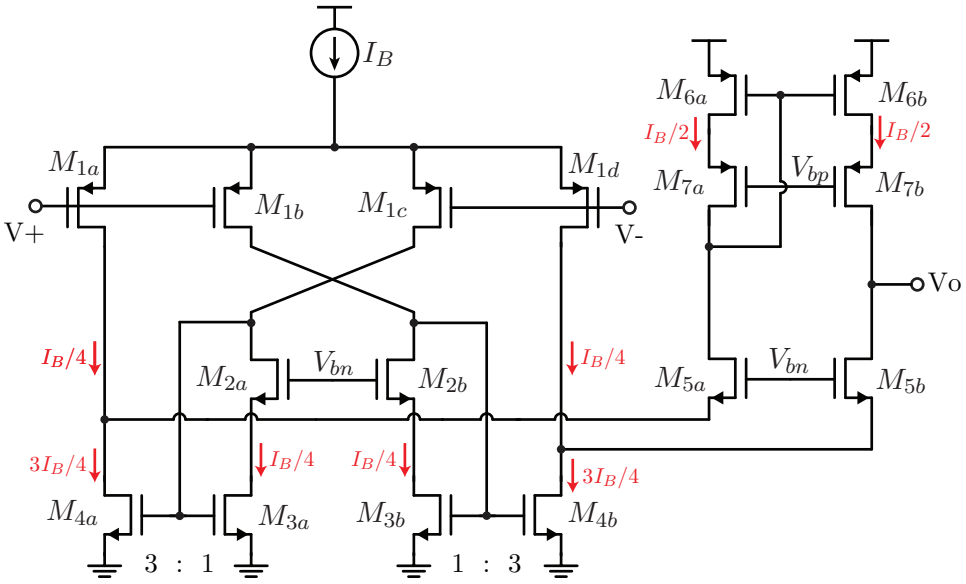


Figure 5.15: Recycling Folded Cascode amplifier with current paths on small-signal operation.

which has to be greater then the differential pair transconductance Gm_{DP} to guarantee stability. To ensure this condition, we specify Gm_{A} to be at least five times greater then Gm_{DP}. With this specification, a lower-bound can be found for M_1 aspect ratio.

$$4gm_1 \geq 5Gm_{\text{DP}} \tag{5.55}$$

$$\left(\frac{W}{L}\right)_{M_1} \geq \frac{25Gm_{\text{DP}}^2\alpha_p}{8K_{pp}I_B} \tag{5.56}$$

Applying the parameters into (5.56), it leads to

$$\left(\frac{W}{L}\right)_{M_1} \geq 2.0468 \tag{5.57}$$

To improve matching between input transistors M_{1a}, M_{1b}, M_{1c} and M_{1d} and also facilitate the layout design, we selected $(W/L)_{M_1} = 3$.

Transistors M_6 - M_7 compose a wide-swing cascode current mirror. To satisfy saturation region conditions of operation, there is a minimum ratio W/L which depends on current swing and transistor parameters. Since this current mirror will appear more times throughout this work, the minimum ratio was derived in Appendix B.1 for further reference.

On small-signal operation, where $V_+ \approx V_-$, the current flowing through M_6 and M_7 is $I_B/2$, as pictured in 5.15. The maximum output swing of the amplifier sets the condition to operate in the saturation region. Applying these constraints in (B.23),

together with PMOS parameters from Appendix A, we obtain the minimum ratio equal to

$$\left(\frac{W}{L}\right)_{M_6} \geq 2.385 \tag{5.58}$$

To allow a wider range of voltage values for V_{bp}, we chose $(W/L)_{M_6} = 5$. Since the output impedance is directly related to voltage gain, transistor length should be larger than minimum size. Therefore, we have

$$M_{6a} = M_{6b} = \frac{5\mu m}{1\mu m} \tag{5.59}$$

To achieve reasonable matching between M_6 and M_7, they have the same width, but since M_7 presents more parasitics, its lenght should be minimum, as recommended by the authors of the RFC [58]. Thus, we have

$$M_{7a} = M_{7b} = \frac{5\mu m}{0.35\mu m} \tag{5.60}$$

Using (B.17), the biasing voltage range can be expressed by

$$1.62 < V_{bp} < 1.75 \tag{5.61}$$

and from that we chose $V_{bp} = 1.68$.

A similar procedure done for M_6 and M_7 can be used to find M_2-M_5. Transistors M_3 and M_4 are responsible for the current copy with a 1:3 ratio, therefore $(W/L)_{M_4} = 3(W/L)_{M_3}$. Transistors M_2 and M_5 are responsible for fixing the drain potential and reduce channel length modulation effect. In equilibrium, the current flowing through M_5 is twice as large as M_2, thus $(W/L)_{M_5} = 2(W/L)_{M_2}$.

On small-signal operation, the current flowing through M_2 and M_3 is $I_B/4$. Applying the current and minimum output swing to (B.23), together with NMOS parameters from Appendix A, the minimum ratio obtained for M_3 is

$$\left(\frac{W}{L}\right)_{M_3} \geq 0.4698 \tag{5.62}$$

and to allow a wider range of voltage values for V_{bn}, we chose $(W/L)_{M_3} = 2$. By extension, $(W/L)_{M_4} = 6$. Transistor M_4 will be implemented using 3 equal parallel devices to obtain a better matching with M_3. It means that $L_4 = L_3$ and $W_4 = 3W_3$. To have a higher output impedance for the amplifier, we chose

$$M_{3a} = M_{3b} = \frac{2\mu m}{1\mu m} \tag{5.63}$$

Similarly to M_7, M_2 and M_5 have minimum length to introduce less parasitics.

We then selected

$$M_{2a} = M_{2b} = \frac{2\mu m}{0.35\mu m} \tag{5.64}$$

Using (B.17), the biasing voltage range can be expressed by

$$1.03 < V_{bn} < 1.18 \tag{5.65}$$

and from that we chose $V_{bn} = 1.13$.

A summary of devices sizes is shown in Table 5.2.

Table 5.2: Recycling folded cascode transistor's dimensions.

Transistor	**Width** (μm)	**Length** (μm)
$M_{1a}, M_{1b}, M_{1c}, M_{1d}$	3	1
M_{2a}, M_{2b}	2	0.35
M_{3a}, M_{3b}	2	1
M_{4a}, M_{4b}	4	0.35
M_{5a}, M_{5b}	6	1
M_{6a}, M_{6b}	5	1
M_{7a}, M_{7b}	5	0.35

5.3.5 Choice of Hold Capacitor

The hold capacitor plays a crucial role in many performance related parameters. As showed in section 5.3.2, it defines the settling time and also non-linearity errors. A large capacitor gives a high precision but increases settling time, as opposed to a small capacitor which increases memory cell speed but reduces its precision.

However, another important issue when choosing the capacitor is its area. As well known, capacitance is proportional to area, which for a integrated circuit manufacturer leads to a higher manufacturing costs. Therefore, it is mandatory to use a capacitor as small as possible.

The main idea of selecting a higher maximum input current than the required is to allow the usage of a smaller capacitor and still achieve high precision. Remembering equation (4.14), where CMC's ENOB lower bound was found to be 11.965 bits. Applying to (5.41), the minimum hold capacitor is given by

$$C_H \geq \frac{2^{11.965} \cdot Q_{ci} \cdot Gm_{\mathrm{DP}} \cdot \delta_n}{i_{in\mathrm{MAX}}} = 0.490pF \tag{5.66}$$

which is a fairly small capacitor. However, to achieve 16 bits, the hold capacitor should have a capacitance of approximately $8pF$. Although it seems small, on a circuit like the one implemented in this work, with more than 50 memory cells, it

would result on a $400pF$ capacitance area, making it very expensive. Therefore, an ENOB 13 bits was adopted, selecting

$$C_H = 1.2pF \tag{5.67}$$

With this choice of capacitor, the unit-frequency, which defines CMC's speed, is given by

$$\omega_u \approx \frac{Gm_{\text{DP}}}{C_H} = 16.667 \text{ Mrad/s} = 2.652 \text{ MHz} \tag{5.68}$$

5.3.6 Switches

As said before, this circuit will work with two kinds of switches, current switches (S_1, S_3 and S_{3d}) and voltage switches (S_2). Since the voltage switch is responsible for charge injection into the hold capacitor, it will be used a minimum size NMOS transistor to implement it, since V_B is closer to GND than V_{DD}. Therefore, we have

$$S_2 = \frac{0.4\mu m}{0.35\mu m} \tag{5.69}$$

The current switches are responsible to open or close the current path. Its dimension influences on switch's on-resistance, which could change the potential at the current memory cell output node. However, since we introduced a dummy switch this effect is not observed in the proposed memory cell. Therefore, current switch sizes does not have to be too large in our design.

We performed a DC sweep to find a switch with an on-resistance of $1k\Omega$, to minimize its effects. This resistance would lead to a maximum drain-source potential of $10mV$ when maximum input current is applied. The value obtained for the current switches is given by

$$S_1 = S_3 = S_{3d} = \frac{2\mu m}{0.35\mu m} \tag{5.70}$$

5.4 Circuit Simulation Results

In this section, the results obtained for the proposed cell through computer-aided circuit simulation are presented. These simulations were performed using the software Cadence Spectre, which uses BSIM3v3 MOSFET model for simulate the transistors. All Monte Carlo analysis were performed considering the statistical variation provided by the CMOS $0.35\mu m$ process manufacturer.

5.4.1 Recycling Folded Cascode

To evaluate the recycling folded cascode (RFC) amplifier, we first performed an AC sweep using the hold capacitor ($C_H = 1.2pF$) on the setup from Fig. 5.16. The results of magnitude and phase obtained are shown in Fig. 5.17. The gain-bandwidth product (GBW) is 14.73 MHz, and the phase margin obtain was 83.93°. The DC gain obtained of 75.08 dB represents a 5675.4 V/V gain, which is the amount of loop-gain enhancement provided by the RFC.

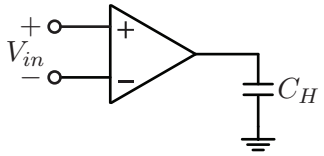


Figure 5.16: AC Sweep simulation setup.

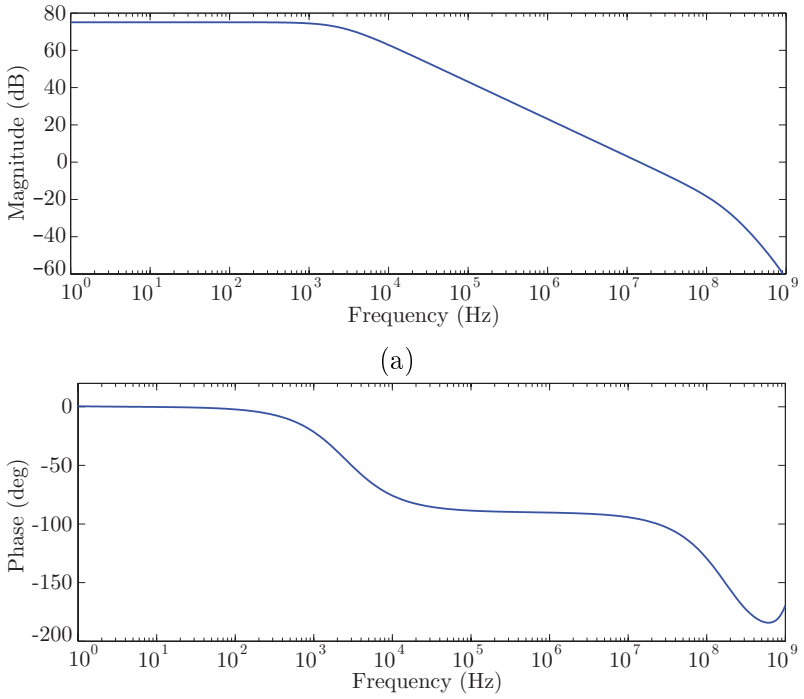


Figure 5.17: Magnitude (a) and Phase (b) plots for the recycling folded cascode.

In order to evaluate the effects of process variation and mismatch in the amplifier parameters, a Monte Carlo simulation was performed with 500 samples. In Fig. 5.18 the results for the magnitude and phase are shown for both mismatch and process parameters variation together. Fig. 5.19 displays the histogram for DC gain, phase margin and gain-bandwidth. The results are very satisfactory, since a DC gain of at least 1000 (60dB) can be guaranteed for 99.7% of the samples (3σ). Also both phase margin and gain-bandwidth shows small variation.

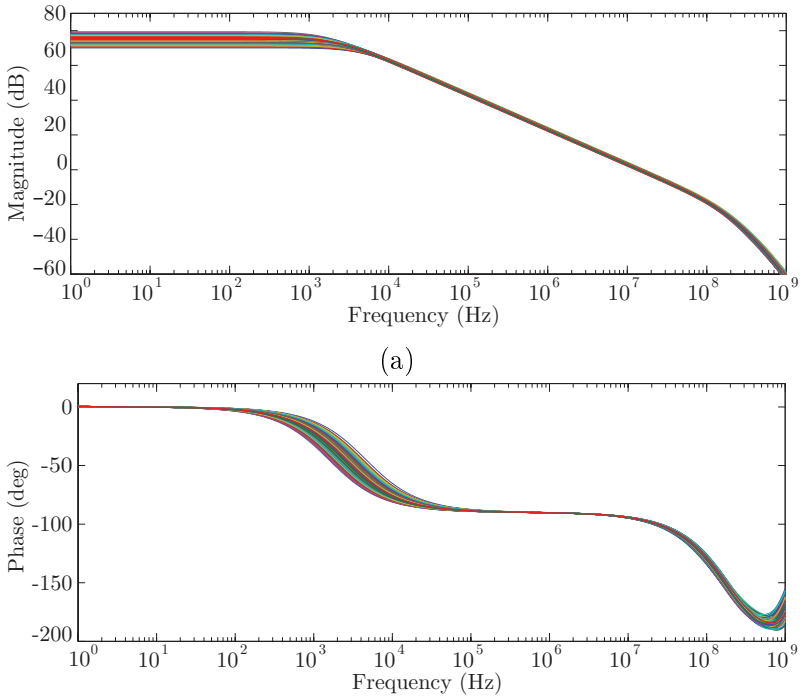


Figure 5.18: Magnitude (a) and Phase (b) plots for all Monte Carlo simulations of the recycling folded cascode.

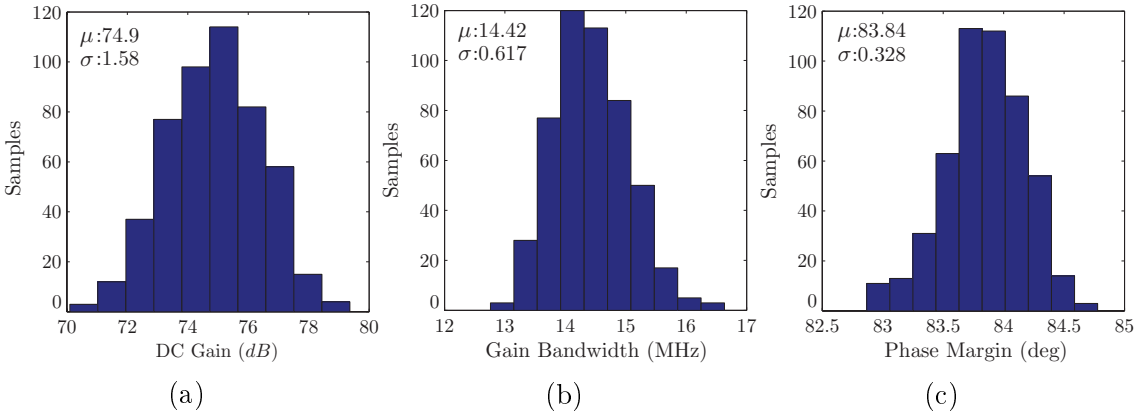


Figure 5.19: Histogram of Monte Carlo simulation resultant data for DC Gain (a), Gain Bandwidth (b) and Phase Margin (c).

Since the amplifier's transconductance is essential to stability, a DC sweep analysis was performed to evaluate its curve. Using the setup on Fig. 5.20 and $V_{cm} = V_B = 1.1V$, the output current i_o obtained with differential voltage v_d variation is presented on Fig. 5.21a. The first derivative of this curve - i.e the amplifier's transconductance - is shown in Fig. 5.21b. Since the RFC will be used to set a virtual ground at switching node, the differential voltage will have a small variation throughout memory cell's operation. The transconductance obtained for $v_d \approx 0$ was $109.06\mu A/V$.

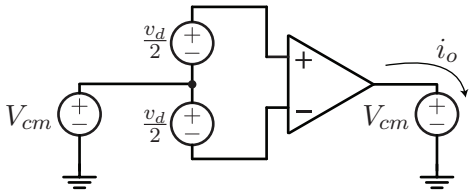
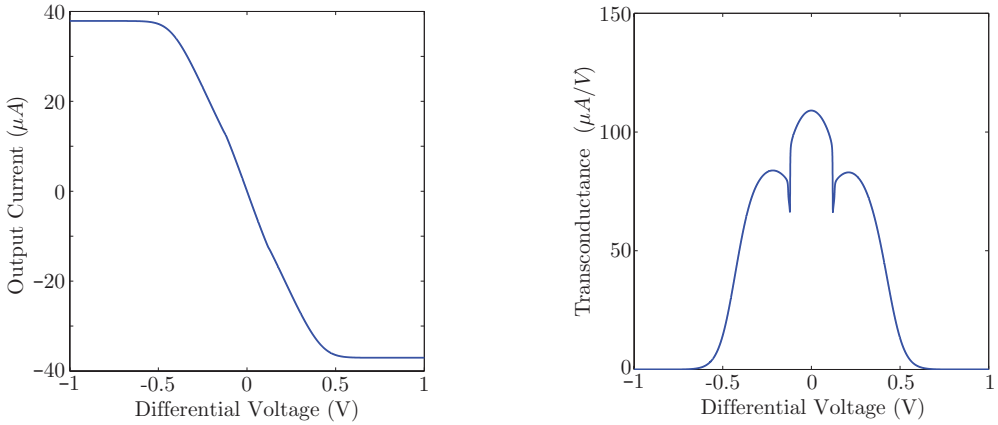


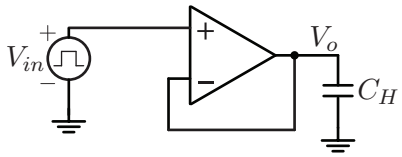
Figure 5.20: DC Sweep simulation setup.



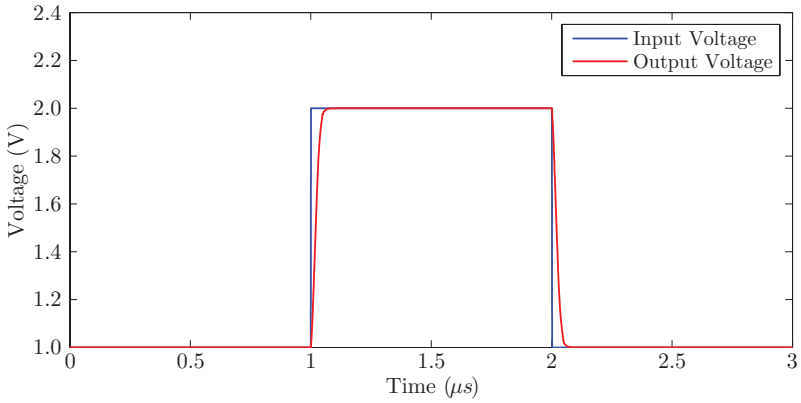
(a) (b)

Figure 5.21: Plot of amplifier's output current (a) and transconductance (b) vs input differential voltage.

To measure slew-rate, a $1V_{pp}$ step input was used, according to the setup shown in Fig 5.22a. The results are given in Fig. 5.22b. The slew-rate obtained was $23.71V/\mu s$, with a 1% settling time of 58.35 ns.



(a)



(b)

Figure 5.22: Slew rate test setup (a) and plot of amplifier's step response (b).

Finally, to observe the input offset, a Monte Carlo simulation with 500 samples

was performed using the setup on Fig 5.23a. The input offset voltage observed at the output is dependent on the amplifier's voltage gain. If A_v is the amplifier DC gain, the output voltage is given by

$$V_o = (V_{cm} + V_{off})\frac{A_v}{1 + A_v} \tag{5.71}$$

The offset voltage can be expressed by

$$V_{off} = V_o\left(\frac{1 + A_v}{A_v}\right) - V_{cm} \tag{5.72}$$

and since $A_v > 1000$, after subtracting the common-mode, the offset error is less than 0.1%. The input offset voltage is distributed according to the histogram on Fig. 5.23b.

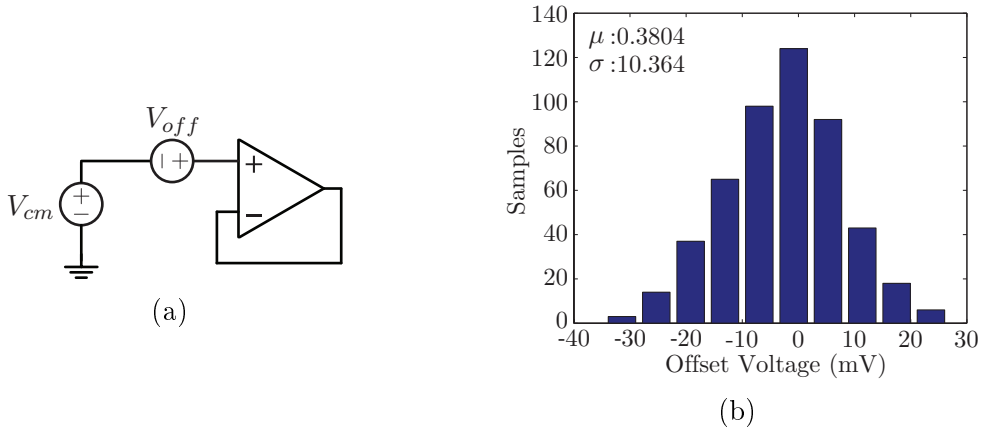


Figure 5.23: Offset Monte Carlo simulation setup (b) and histogram of the resultant data (b).

A summary of the performance characterization results is shown in Table 5.3.

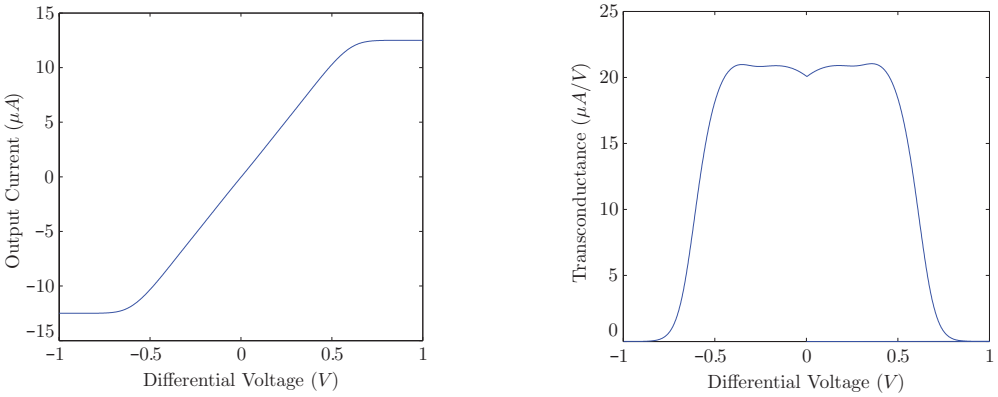
Table 5.3: Recycling folded cascode performance summary.

Parameter	**Nominal**
DC Gain (dB)	74.8988
GBW (MHz)	14.4206
Phase Margin (deg)	83.8452
Transconductance ($\mu A/V$)	109.062
Slew Rate ($V/\mu s$)	23.71
1% Settling Time (ns)	58.35
Input Offset (3σ) (mV)	31.0926

5.4.2 High-Linearity Differential Pair

To evaluate the high-linearity differential pair transconductance, a DC sweep was performed using a similar setup to the one used for the RFC, pictured in Fig. 5.20,

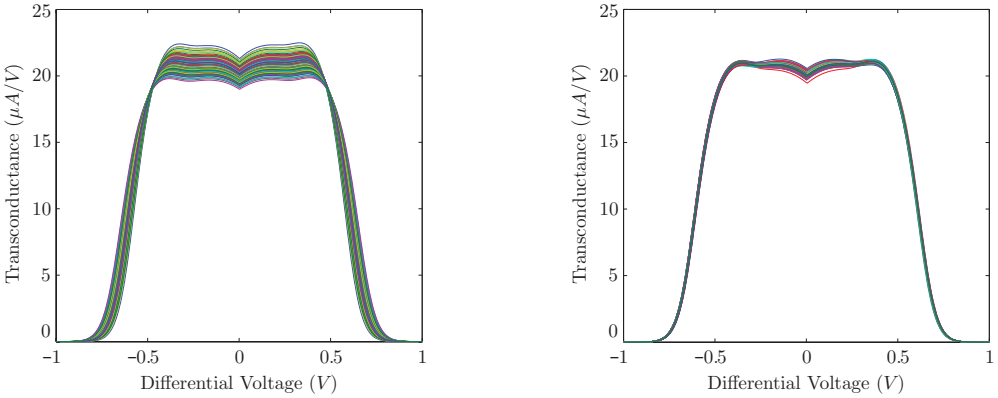
where instead of the RFC, the HLDP was used. The differential voltage v_d is swept from -1V to 1V to measure the output current i_o. The output current plot is presented in Fig. 5.24a and its derivative in Fig. 5.24b. A ripple of $\pm 5.3\%$ was achieved with an average transconductance $Gm_{\mathrm{DP}} = 19.98\mu A/V$. Both ripple and average transconductance were obtained by clipping the transconductance curve between maximum input current limits of $\pm 10\mu A$.



(a) (b)

Figure 5.24: Plot of high-linearity differential pair output current (a) and transconductance (b) vs input differential voltage.

To observe the effects of both mismatch and process parameters variation on the high-linearity differential pair, two Monte Carlo analysis were executed, with 100 samples each, considering each variation separately. The results for process parameters variation and transistor mismatch are presented in Fig. 5.25a and Fig. 5.25b, respectively. As it can be seen, process variations has more influence on the transconductance mean value and mismatch on its shape.

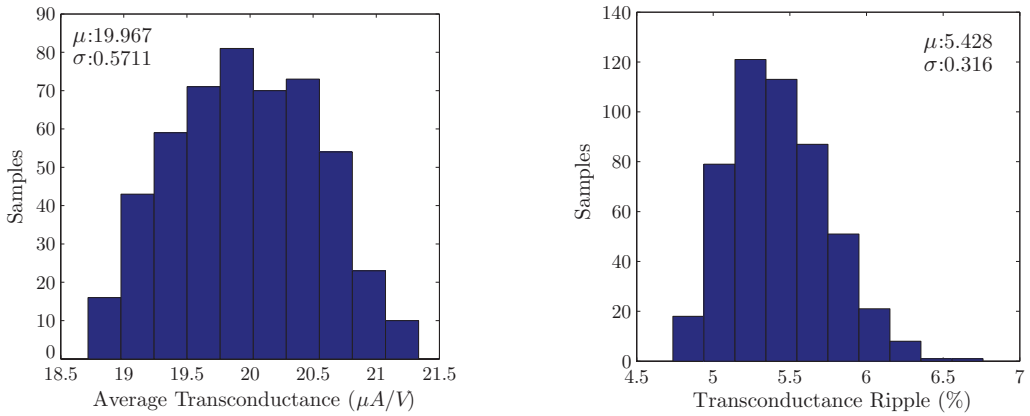


(a) (b)

Figure 5.25: Monte Carlo results of the high-linearity differential pair transconductance curve under process parameters variation (a) and mismatch (b).

To evaluate the effect of manufacturing imperfection into the HLDP, a Monte Carlo analysis considering both effects was performed with 500 samples. With this

analysis, the statistical distribution of average transconductance Gm_{DP} and its ripple δ_n were obtained. Both histograms are presented in Fig. 5.26. The condition for minimum transconductance $Gm_{\mathrm{DP}} > 16.7\mu A/V$ is achieved for 3σ. Also, ripple variation is very small, and therefore the improvements introduced by using this high-linearity differential pair are effective even when manufacturing imperfection are considered.



(a) (b)

Figure 5.26: Histogram of Monte Carlo simulation resultant data for average transconductance(a) and transconductance ripple (b).

5.4.3 Proposed Memory Cell

To start evaluating the memory cell precision, its stability should be checked to ensure proper operation. A stability analysis was performed using Spectre to obtain the open-loop characteristics presented in Fig. 5.27. An open-loop DC gain of 128.5881 dB was obtained with 77.197° phase margin at 2.711 MHz. A gain margin of 13.5 dB was obtained at 42.32 MHz. Notice the unit frequency of 2.711 MHz is close to the 2.652 MHz calculated before, proofing the mathematical approach used.

To further evaluate stability properties, the closed-loop transfer function was also measured. To perform this analysis the loop was closed and an AC stimulus was introduced at the input, and the HLDP output current was observed. The results are shown in Fig. 5.28. Due to high-frequency complex poles, a small peak is formed around 100 MHz, but its level is under 0 dB, representing no issues for CMC's operation. Its -3dB frequency is 3.752 MHz.

The main important measurement for the proposed memory cell is its precision. Two different tests can be performed for this matter, a static test, which evaluates precision using current transfer error; and a dynamic test, which evaluates precision using spectral properties.

Starting with the static test, the goal is to obtain the current transfer error,

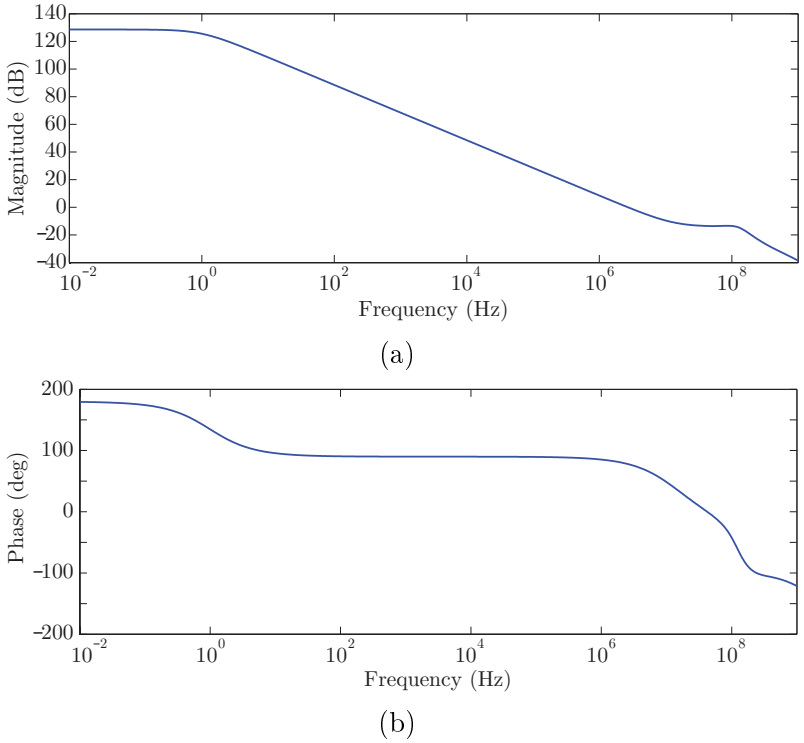


Figure 5.27: Open-loop magnitude (a) and phase (b) characteristics.

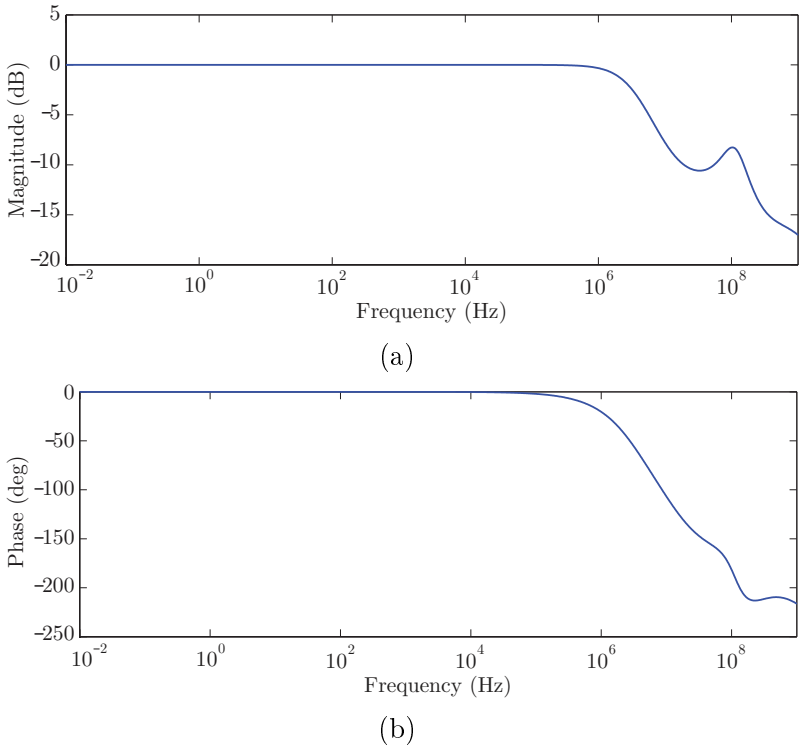


Figure 5.28: Closed-loop magnitude (a) and phase (b) characteristics.

defined by $i_o - i_{in}$. Since the CMC works in two different phases, sampling and holding, a DC sweep is not an option. Thus, to evaluate the transfer error, a series of current steps were applied to the input, forming almost a staircase signal. Each

degree of the staircase had a distance of $1\mu A$, from $-10\mu A$ to $10\mu A$, allowing 21 points to trace the curve. The test setup is pictured in Fig. 5.29. The output of the CMC under test goes to a second CMC, in order to keep a virtual ground at the previous CMC output node. Also, to never stop current flow, a dummy switch to a low impedance node is put at input current source node.

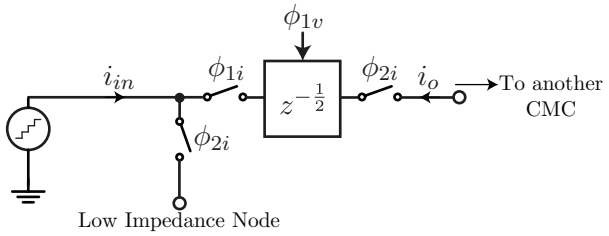


Figure 5.29: Current memory cell static test setup.

The transient response for the referred test is showed in Fig. 5.30. Current peaks can be observed in the output current, during the phase transitions. These are numerical errors created by the simulator due to the switching of current paths, which might create discontinuities in the simulation. After the peak, the output current value remains constant during the holding phase, and three samples were taken for each step value of input current, right at the center of holding phase pulse. The average of these three samples was taken in order to mitigate imperfections created by the simulator, such as a small current drain by G_{min}. The resulting curve is presented in Fig. 5.31.

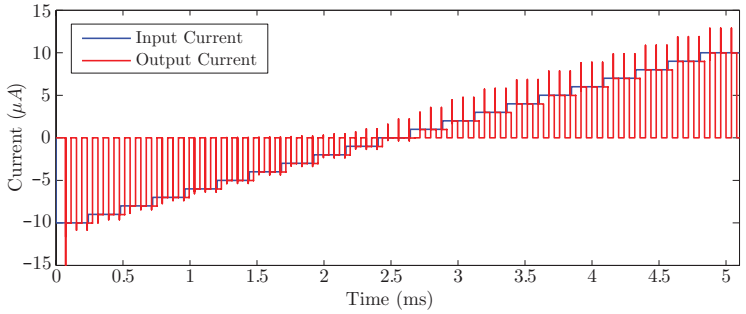


Figure 5.30: Transient response of the static test.

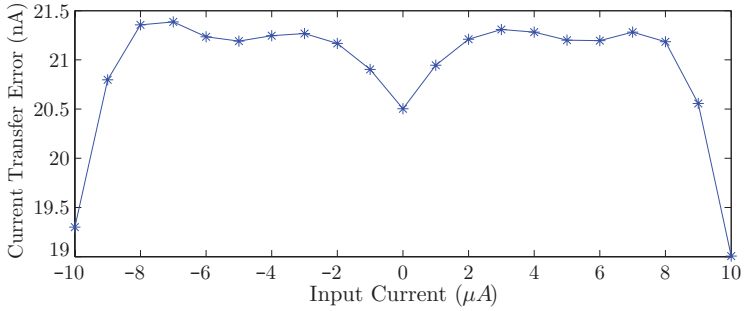
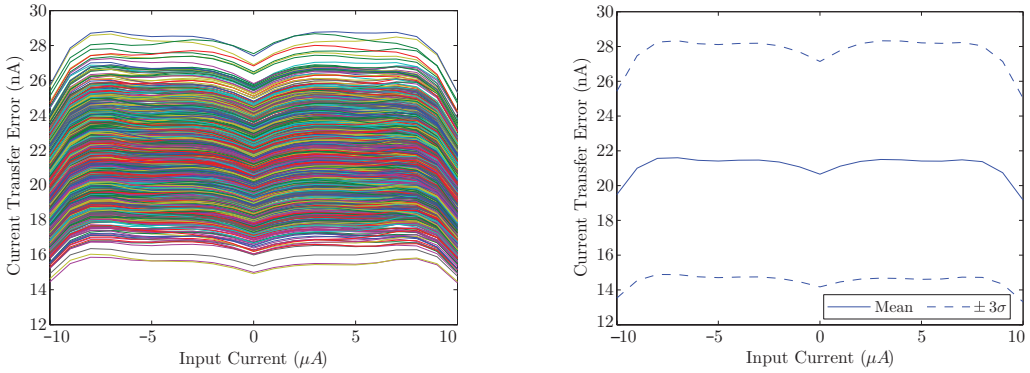


Figure 5.31: Current transfer error ($i_o - i_{in}$) vs input current (i_{in}).

As it can be seen, the current transfer error curve has similar appearance to the high-linearity differential pair transconductance curve. From the transfer error curve, it can be seen an offset of $20.195nA$, with non-linearity errors corresponding to $\pm 1.18982nA$. The effective number of bits (ENOB) is obtain using (5.40), leading to 13.03697 bits, which is slightly higher than the designed value of 13 bits, showing that our mathematical model is accurate.

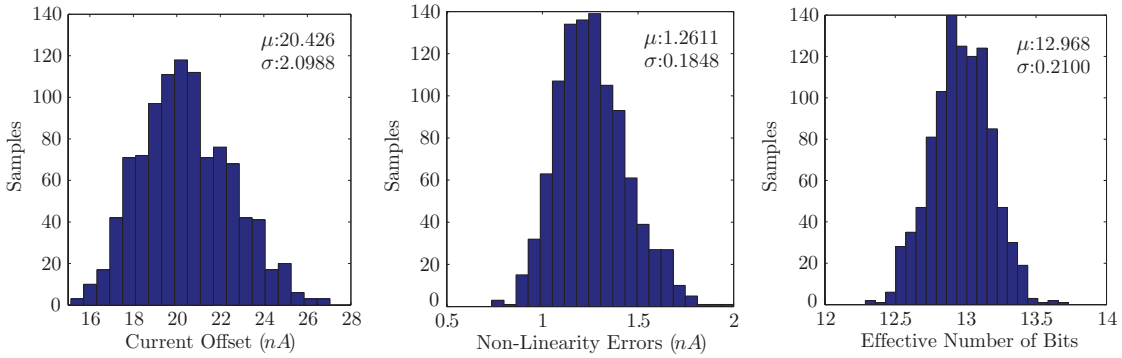
To evaluate the effects of process parameter variation and mismatch to the memory cell precision, a Monte Carlo simulation was performed with 1000 samples. For each Monte Carlo sample, one transfer error curve is obtained, leading to the result of Fig. 5.32a. The statistics are shown in Fig. 5.32b.



(a) (b)

Figure 5.32: Monte Carlo results of the current transfer error curve (a) and its statistical variations (b).

The values of offset, non-linearity errors and ENOB for each Monte Carlo transfer error curve were extracted, and displayed on the histograms of Fig. 5.33. In Chapter 4.3.3, a minimum ENOB of 11.965 bits was derived. For the ENOB distribution obtained, the minimum value is guaranteed with a 4.8σ yield, which represents 99.96% of the samples. This gives a high reliability to the designed CMC.



(a) (b) (c)

Figure 5.33: Histogram of Monte Carlo simulation resultant data for current offset (a), non-linearity errors (b) and effective number of bits (c).

Following the static test, the dynamic test was performed to evaluate spectral behavior of the proposed CMC. To perform this test, a sinusoidal input was applied to the input of the CMC under test and the memory cell performed as a sample and hold circuit. The discrete sinusoidal observed at the output was then analyzed in the frequency domain using a fast-fourier transform. Fig. 5.34 exhibits the dynamic test setup.

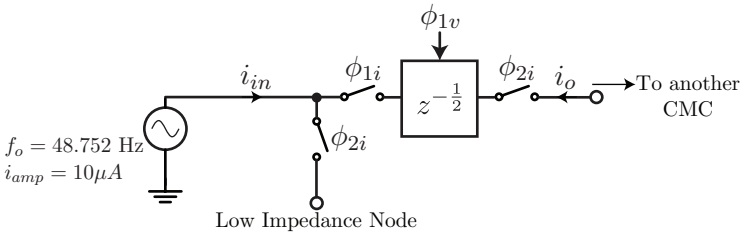


Figure 5.34: Current memory cell dynamic test setup.

The maximum current of $10\mu A$ was adopted for the sinusoidal input current. The signal frequency should be equal to switching frequency divided by a power of 2, to facilitate FFT evaluation and have the fundamental frequency equal to a FFT bin center. Since the system's input signal is 60 Hz, we chose

$$f_o = \frac{f_s}{2^8} = \frac{12.4805 \cdot 10^3}{256} = 48.752Hz \tag{5.73}$$

With this setup, a transient simulation was performed to obtain the sampled signal at the output. The transient results are shown in Fig. 5.35. From the discrete output signal, a sample was taken right in the center of the holding phase, composing the sampled output signal from Fig. 5.36.

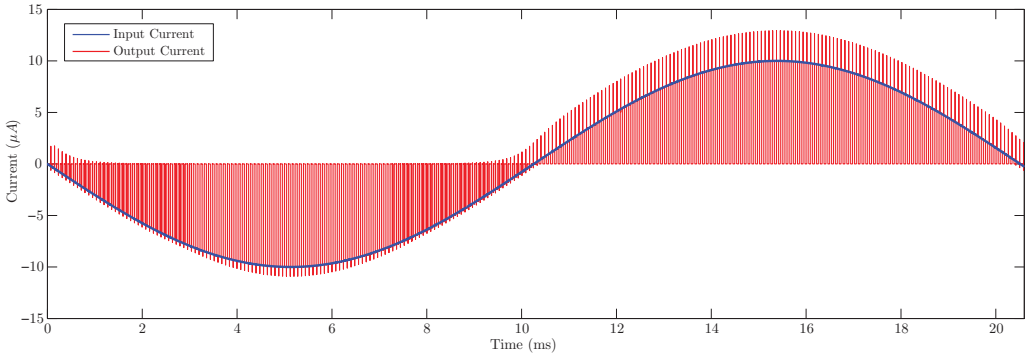


Figure 5.35: Transient response of the dynamic test.

With the sampled output, a fast Fourier transform was performed using 256 points. The results are shown in Fig. 5.37. From the FFT, two measurements were obtained: Signal-to-Noise-and-Distortion ratio (SINAD) , which is ratio between signal power over noise and distortion power; and Spurious-Free Dynamic Range

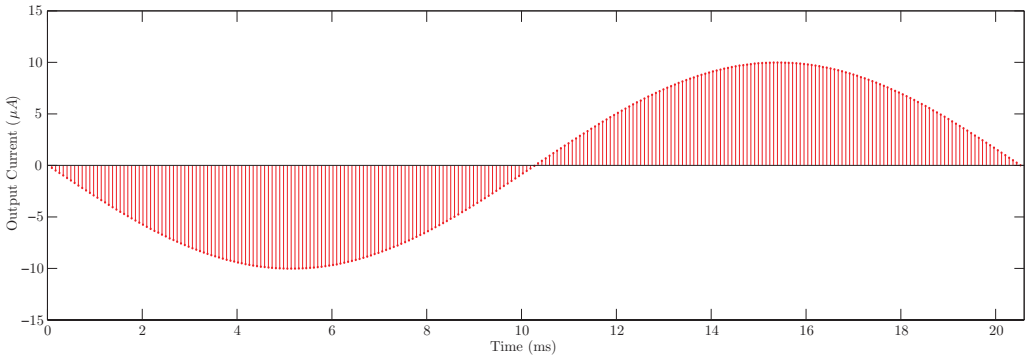


Figure 5.36: Sampled output of the dynamic test.

(SFDR), which is defined by the strength ratio of fundamental and strongest spurious on the signal [59, p. 445-461]. The effective number of bits is given by

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{5.74}$$

where SINAD is given in dB. For the nominal simulation, a SINAD of 79.79 dB and a SFDR of 83.01 dB were obtain. Using (5.74) leads to a ENOB of 12.96 bits. Comparing with the static test, the results were very similar, reinforcing the effectiveness of the mathematical model used in this work.

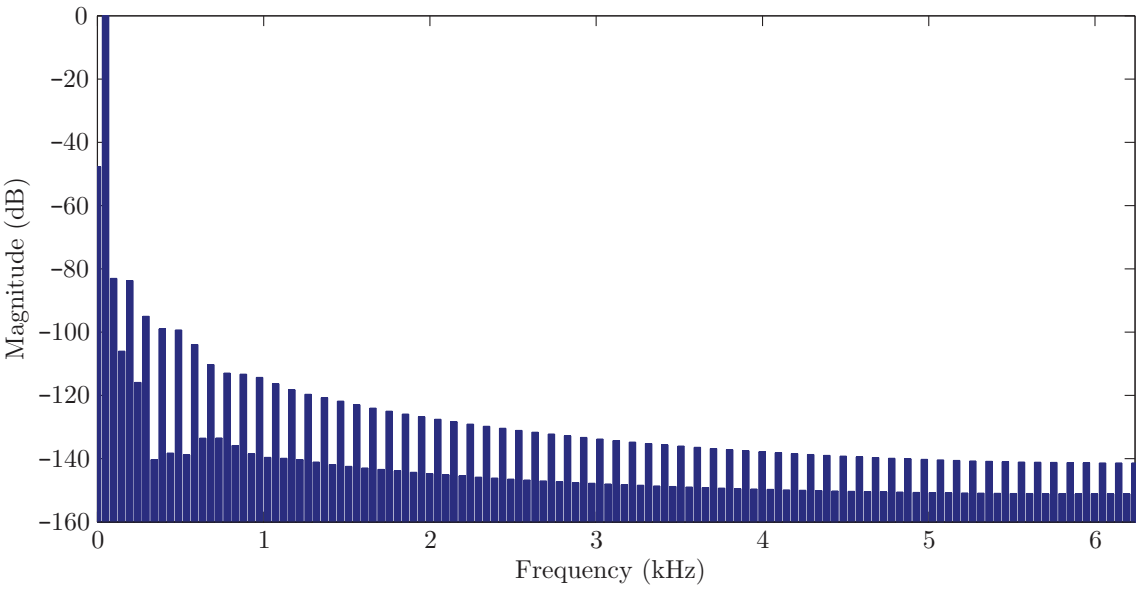
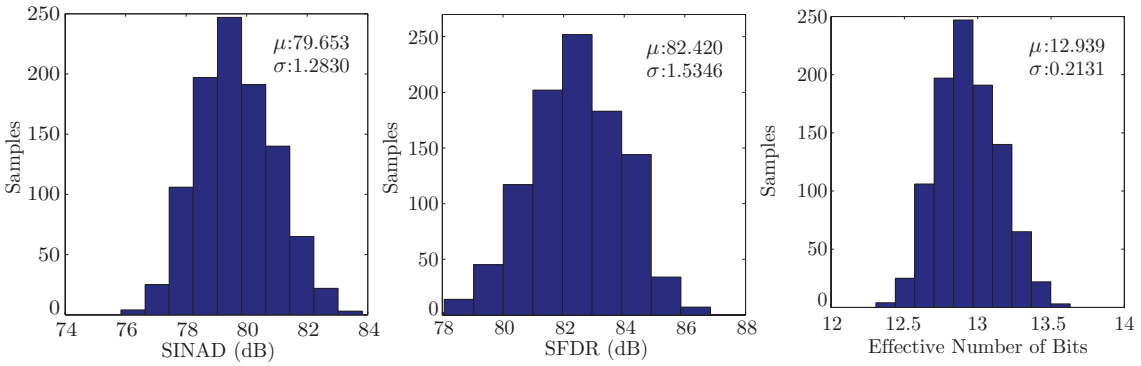


Figure 5.37: Magnitude response of the sampled output fast Fourier transform.

Once again, to evaluate the effects of process parameter variation and mismatch in the memory cell precision, a Monte Carlo simulation was performed with 1000 samples and histograms for SINAD, SFDR and ENOB were obtained, and are presented in Fig. 5.38. When compared to the static tests, both ENOB distribution are very similar.



(a) (b) (c)

Figure 5.38: Histograms of Monte Carlo simulation resultant data for signal-to-noise-and-distortion ratio (a), spurious-free dynamic range (b) and effective number of bits (c).

A summary with simulated parameters for the proposed current memory cell is presented in Table 5.4.

Table 5.4: Proposed current memory cell performance summary.

Parameter	**Nominal**	**Mean**	**Std. Dev.**
Static Power (μW)	165	-	-
Current Range (μA)	$\pm$10	-	-
Open-loop Gain (dB)	128.5881	-	-
Phase Margin (deg)	77.197	-	-
Unit-Frequency (MHz)	2.71	-	-
Offset Error (nA)	20.195	20.426	2.0988
Non-linearity Error (nA)	1.18982	1.2611	0.1848
ENOB (static)	13.03	12.968	0.2100
SINAD (dB)	79.79	79.565	1.2830
SFDR (dB)	83.01	82.420	1.5346
ENOB (dynamic)	12.96	12.939	0.2131

Chapter 6

Circuit Level Design

In this Chapter, the other building blocks necessary for the system design - biasing currents, coefficient gain block, differential current mirror, output current copy and current multiplier - are analyzed. For each block, its implementation choices are discussed and the circuit design process is detailed. Each block is validated through circuit simulation.

6.1 Biasing Current

Throughout this work, current sources are used to bias the transistors and allow operation on the proper region. These current sources are implemented by "mirroring" a single current reference from outside the integrated circuit. To achieve high-precision on the mirror copy, a cascode topology must be used to increase the current source output resistance. Also, to allow a wide voltage swing at the current source output, wide-swing cascode current mirror was chosen [48, p. 144].

The current sources must be implemented to provide current, using PMOS transistors, and to drain current, using NMOS transistors. The circuit implementation is presented on Fig. 6.1. The current source I_{REF} provides the reference for the current copies.

In this system, the current reference have the biasing value defined while designing the current memory cell, given by

$$I_{REF} = I_B = 12.5\mu A \tag{6.1}$$

The reference is mirrored with a 1:1 ratio, thus each PMOS transistor have same dimmensions, as well as each NMOS transistor.

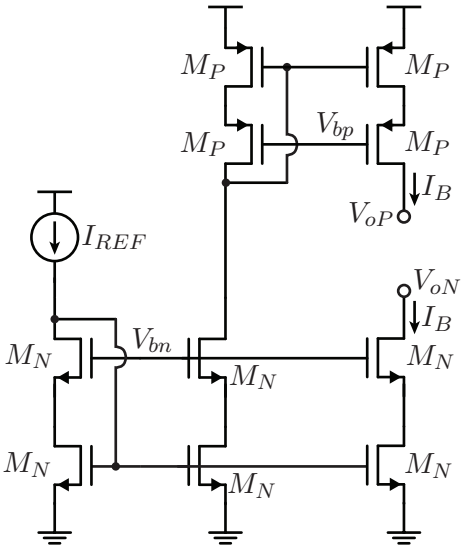


Figure 6.1: Circuit implementation of the biasing currents.

6.1.1 Circuit Design

The design process for the current sources is simple. Since the current is constant, the mirror operation is constraint by the output voltage. The wide-swing cascode current mirror allows V_{oN} to swing as low as $2V_{ov}$ for a NMOS, and V_{oP} to swing as high as $V_{DD} - 2|V_{ov}|$, where V_{ov} is the overdrive voltage. Specifying a $250mV$ overdrive for both NMOS and PMOS, we obtain

$$V_{oN\text{MIN}} = 0.5V \tag{6.2}$$

$$V_{oP\text{MAX}} = 2.8V \tag{6.3}$$

The minimum ratio to realize a wide-swing cascode current mirror was obtained in Appendix B.1. For the NMOS current mirror, $V_{oN\text{MIN}}$ and I_B can be applied to (B.23), and the minimum ratio is expressed by

$$\left(\frac{W}{L}\right)_N \geq \frac{8I_B}{\alpha_n k_{pn} V_{oN\text{MIN}}^2} = 1.8793 \tag{6.4}$$

To allow a wider range of biasing voltages, it was chosen $(W/L)_N = 3$. With the chosen ratio and the design variables, the biasing voltage V_{bn} can be in the range

$$1.1176 \geq V_{bn} \geq 1.0133 \tag{6.5}$$

from which it was chosen $V_{bn} = 1.06$.

The current source will have a small deviation from the reference value due to mismatch between transistors. To control the deviation, the Pelgrom rules applied to the current mirror in Appendix D.3 are used here to dimension the current sources

transistors. For the current sources, it is specified a 1% deviation for 3σ. The standard deviation in percentage of the reference is given by

$$\sigma_{CS} = 0.333\% \tag{6.6}$$

Employing σ_{CS} and the ratio $(W/L)_N$ in (D.25), the minimum length is given by

$$L_N \geq 12.838\mu m \tag{6.7}$$

and to guarantee that the variance is met, the final choice for M_N is expressed by

$$\left(\frac{W}{L}\right)_N = \frac{45\mu m}{15\mu m} \tag{6.8}$$

A similar procedure is done for the PMOS current mirror. The minimum ratio is given by

$$\left(\frac{W}{L}\right)_P \geq \frac{8I_B}{\alpha_p k_{pp}(V_{DD} - V_{oP\text{MAX}})^2} = 4.7710 \tag{6.9}$$

and to allow a wider range of biasing voltages, it was chosen $(W/L)_P = 7$. With the chosen ratio and the design variables, the biasing voltage V_{bp} can range between

$$2.0630 \geq V_{bp} \geq 1.9758 \tag{6.10}$$

and finally was chosen $V_{bp} = 2.02$. Employing σ_{CS} and the ratio $(W/L)_P$ in (D.25), the minimum length is given by

$$L_P \geq 12.372\mu m \tag{6.11}$$

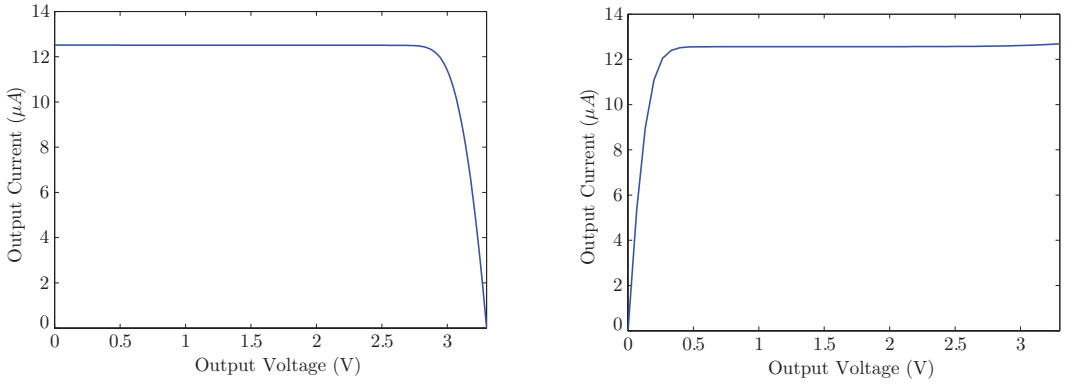
and to guarantee that the variance is met, the final choice for M_P is expressed by

$$\left(\frac{W}{L}\right)_P = \frac{98\mu m}{14\mu m} \tag{6.12}$$

6.1.2 Circuit Simulation

To evaluate the biasing current sources, a DC sweep simulation was perform to evaluate the output voltage range. Both V_{oP} and V_{oN} were swept from ground to V_{dd} and the output current was obtained. The results are shown in Fig. 6.2. The PMOS current source, showed in Fig. 6.2a, has an almost constant value for a range between 0 and 2.76V and the NMOS current source, presented in Fig. 6.2b, has an output voltage range from V_{dd} to 0.462 V.

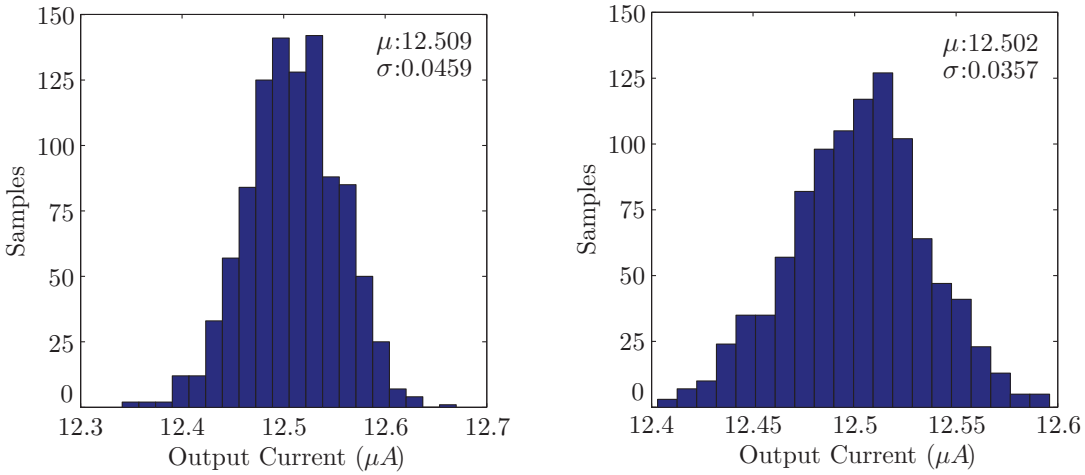
A Monte Carlo simulation with 1000 samples was performed to observe the current variation with mismatch and process parameters. Results are presented



(a) (b)

Figure 6.2: DC Sweep of the output voltage for (a) PMOS biasing current and (b) NMOS biasing current.

in Fig. 6.3. The standard deviation obtained for PMOS biasing current of $45.9nA$ represents 0.362% of the bias current. The NMOS biasing current standard deviation of $35.7nA$ represents 0.285% of the bias current. The values are close to the desired σ of 0.33%.



(a) (b)

Figure 6.3: Histogram of the Monte Carlo simulation resultant data for the output current of (a) PMOS biasing current with Vop = 2.1 and (b) NMOS biasing current with Von = 1.1.

6.2 Coefficient Gain Block

The coefficient gain block (CGB) is responsible to implement the transfer function coefficient in the structurally all-pass section. Its ideal representation in shown in Fig. 6.4.

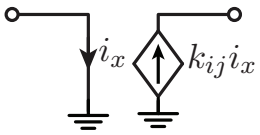


Figure 6.4: Coefficient gain block ideal implementation.

From the ideal model, one can see that the output current leaves the CGB with same phase as the input. Since basic current mirrors invert the current signal phase, two cascade current mirrors are necessary to implement the CGB. For simplicity, the first current mirror will implement the coefficient gain, and the second one will just invert the phase (ratio 1:1).

The transfer function coefficients were approximated by a ratio of integers in Chapter 4.3.2 to improve matching properties of the current mirror. The ratios to be implemented are given by

$$k_{11} = \frac{8}{9}; \quad k_{12} = \frac{1}{5}; \quad k_{21} = \frac{3}{5} \tag{6.13}$$

One important issue to address is related to the current memory cells (CMC). Since they load the stored current into CGB input, a virtual ground should be provided by the CGB. For this task, a simple current conveyor, pictured in Fig. 6.5, will met specifications. The amplifier works on a voltage buffer configuration, setting CGB's input node voltage at V_B. Transistor M_g works on a source-follower configuration. Since the amplifier is stable, with 83.93° of phase margin, transistor M_g will not bring the system to instability, since it works as a buffer. However, the referred phase margin was obtained for a 1.2pF load capacitor, which is implemented by the gate-source capacitance of M_g. This must be taken into account while sizing M_g.

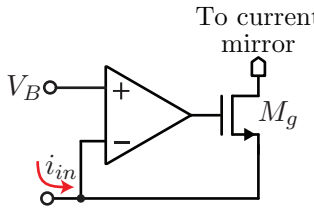


Figure 6.5: Current conveyor to implement input virtual ground.

To reduce design complexity, the amplifier will be implemented using the Recycling folded cascode (RFC) implemented for the CMC, in Chapter 5. By reusing the RFC, the layout work is also reduced. The complete circuit, with both current mirrors and the input current conveyor is presented in Fig. 6.6a. The first current mirror is implemented using PMOS and is responsible for implemented the coefficient and the second mirror is implemented with NMOS with a 1:1 ratio. Since it

operates in class A, a biasing current is added at the input, which is also scaled by a k_{ij} factor. Hence the biasing current with value $2k_{ij}I_B$. Considering that the biasing block does not provide such current, the PMOS current mirror is repeated to implement it, as pictured in Fig. 6.6b. The layout design can be also be reused.

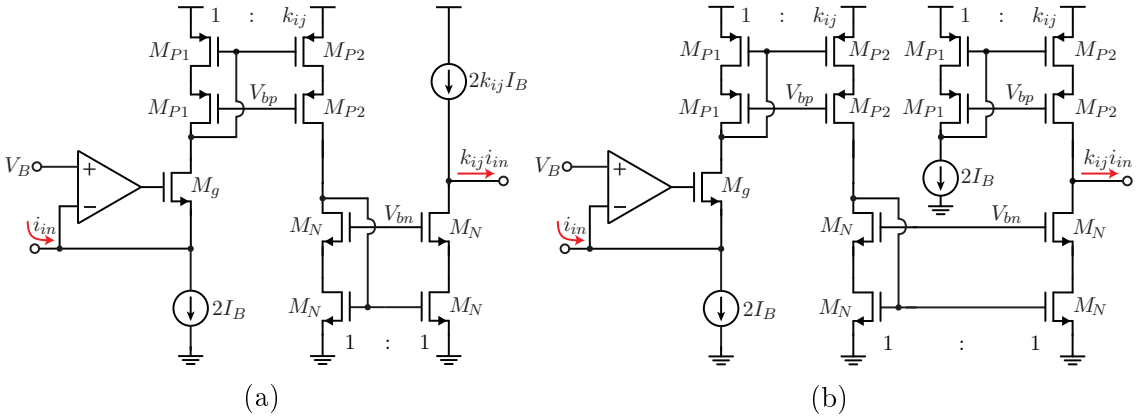


Figure 6.6: Coefficient gain block complete circuit with (a) $2k_{ij}I_B$ biasing current at the output and (b) with current mirror to implement the current.

The reason for using a biasing current of value $2I_B$ instead of I_B is that the CGB input current is the sum of the output from the differential current mirror and a current memory cell. If both have maximum current, it would extrapolate the limit of I_B, since $i_{in\text{MAX}} = 0.8I_B$. To ensure proper operation at those limits, the biasing current was set in $2I_B$.

6.2.1 Circuit Design

Each coefficient requires a different design, since their current mirroring ratios are different. Therefore, the design procedure was made for a generic k_{ij} coefficient, and the equation for each transistor sizes were obtained in a general form, so that each coefficient value is plugged in and their values were obtained. The design is based in the circuit from Fig. 6.6b.

First, consider that the coefficient k_{ij} is implemented by a ratio of two integers, N_1 and N_2, i.e. $k_{ij} = N_2/N_1$. Transistors M_{P1} and M_{P2} are implemented by parallel unitary transistors of same size, however M_{P1} is implemented with N_1 in parallel and M_{P2} with N_2 transistors in parallel. Hence

$$M_{P1} = N_1 \left(\frac{W}{L}\right)_P \quad ; \quad M_{P2} = N_2 \left(\frac{W}{L}\right)_P \tag{6.14}$$

The current requirements for each unitary transistor of the PMOS current mirror is given by

$$I_{P\text{MAX}} = \frac{2I_B + 2i_{in\text{MAX}}}{N_1} = \frac{3.6I_B}{N_1} \tag{6.15}$$

$$I_{P\text{MIN}} = \frac{2I_B + 2i_{in\text{MIN}}}{N_1} = \frac{0.4I_B}{N_1} \tag{6.16}$$

which is applied to (B.29) to obtain the minimum ratio, given by

$$\left(\frac{W}{L}\right)_P \geq \frac{2\alpha_p I_B}{k_{pp} V_{T0p}^2 N_1} \left[\left(1 + \frac{1}{\alpha_p}\right)\sqrt{3.6} - \left(2 - \frac{1}{\alpha_p}\right)\sqrt{0.4}\right]^2 \tag{6.17}$$

and the chosen value should be slightly bigger. With W/L chosen, the biasing voltage limits can be retrieved using (B.24)

$$V_{bp\text{MIN}} \approx V_{DD} - \left(2 - \frac{1}{\alpha_p}\right)\sqrt{\frac{0.8\alpha_p I_B}{k_{pp} N_1 (W/L)_P}} - 2|V_{T0p}| - 0.150 \tag{6.18}$$

$$V_{bp\text{MAX}} \approx V_{DD} - \left(1 + \frac{1}{\alpha_p}\right)\sqrt{\frac{7.2\alpha_p I_B}{k_{pp} N_1 (W/L)_P}} - |V_{T0p}| - 0.150 \tag{6.19}$$

and V_{bp} must be chosen between those limits. Finally, the transistor size is selected using the Pelgrom model derived in Appendix D.3 for current mirrors. For a 1% gain error in a 3σ yield. This gain error is splitted by each current mirror, thus

$$\sigma_P = \sigma_N = \frac{1\%}{3\sqrt{2}} \approx 0.236\% \tag{6.20}$$

The minimum length to obtain the desired yield was derived in (D.25) and is given by

$$L_{P\text{MIN}} = \frac{1}{\sigma_P}\sqrt{\left(\frac{N_1 + N_2}{N_2}\right)\left[\frac{1}{(W/L)_P N_1}\hat{A}_{k_p}^2 + \frac{k_{pp} V_{T0p}^2}{I_B \alpha_p}\hat{A}_{V_{T0}}^2\right]} \tag{6.21}$$

A similar procedure is done to find M_N dimensions. The current limits of operation are given by

$$I_{P\text{MAX}} = \frac{N_2}{N_1}(2I_B + 2i_{in\text{MAX}}) = \frac{N_2}{N_1} 3.6 I_B \tag{6.22}$$

$$I_{P\text{MIN}} = \frac{N_2}{N_1}(2I_B + 2i_{in\text{MIN}}) = \frac{N_2}{N_1} 0.4 I_B \tag{6.23}$$

and the minimum ratio is expressed by

$$\left(\frac{W}{L}\right)_N \geq \frac{2\alpha_n I_B N_2}{k_{pn} V_{T0n}^2 N_1} \left[\left(1 + \frac{1}{\alpha_n}\right)\sqrt{3.6} - \left(2 - \frac{1}{\alpha_n}\right)\sqrt{0.4}\right]^2 \tag{6.24}$$

and the chosen value should be slightly bigger. With W/L chosen, the biasing voltage limits can be retrieved using (B.24)

$$V_{bn\text{MAX}} \approx \left(2 - \frac{1}{\alpha_p}\right)\sqrt{\frac{0.8\alpha_p N_2 I_B}{k_{pp} N_1 (W/L)_N}} + 2V_{T0n} + 0.1 \tag{6.25}$$

$$V_{bn\text{MIN}} \approx \left(1 + \frac{1}{\alpha_n}\right)\sqrt{\frac{7.2\alpha_p N_2 I_B}{k_{pn} N_1 (W/L)_N}} + V_{T0n} + 0.1 \tag{6.26}$$

The minimum length to obtain the desired yield is given by

$$L_{N\text{MIN}} = \frac{1}{\sigma_N}\sqrt{2\left[\frac{1}{(W/L)_N}\hat{A}_{k_p}^2 + \frac{k_{pn}V_{T0n}^2}{\frac{N_2}{N_1} I_B \alpha_n}\hat{A}_{V_{T0}}^2\right]} \tag{6.27}$$

Based on these equations, the design of each transistor was executed. The results for each parameter is presented in Table 6.1.

Table 6.1: Design summary for each coefficient gain block.

Parameters	$k_{11} = 8/9$	$k_{12} = 1/5$	$k_{21} = 3/5$
N_1	9	5	5
N_2	8	1	3
$(W/L)_P$ min	0.7849	1.4128	1.4128
$V_{bp\text{MAX}}$ (V)	1.7436	1.7069	1.7069
$V_{bp\text{MIN}}$ (V)	1.5424	1.5968	1.5968
V_{bp} (V)	1.65	1.65	1.65
$L_{p\text{MIN}}$	12.626 μm	21.250 μm	14.166 μm
$(W/L)_P$ final	$19.5\mu m/13\mu m$	$44\mu m/22\mu m$	$30\mu m/15\mu m$
$(W/L)_N$ min	4.8674	1.0952	3.2855
$V_{bn\text{MAX}}$ (V)	1.2220	1.2083	1.2186
$V_{bn\text{MIN}}$ (V)	1.1406	1.0809	1.1258
V_{bn} (V)	1.18	1.14	1.16
$L_{n\text{MIN}}$	$13.466\mu m$	$27.433\mu m$	$15.857\mu m$
$(W/L)_N$ final	$94.5\mu m/13.5\mu m$	$56\mu m/28\mu m$	$80\mu m/16\mu m$

The final step into the coefficient gain block is to size transistor M_g, which is the same for every coefficient. To keep it in strong inversion throughout whole operation range, it is specified

$$\left(\frac{gm}{2I_B + 2i_{in\text{MIN}}}\right) = 10 \rightarrow \left(\frac{W}{L}\right)_{M_g} \approx 2 \tag{6.28}$$

and to keep phase margin of the RFC, the gate source capacitance on saturation region must be equal to 1.2 pF, the load capacitance for which the RFC was design. Therefore, we have

$$\frac{2}{3}C_{ox}WL = \frac{2}{3}C_{ox}\left(\frac{W}{L}\right)_{M_g} L^2 = 1.2pF \tag{6.29}$$

$$L = \sqrt{\frac{1.2pF}{\frac{4}{3}C_{ox}}} \approx 14\mu m \rightarrow \left(\frac{W}{L}\right)_{M_g} = \frac{28\mu m}{14\mu m} \tag{6.30}$$

6.2.2 Simulation Results

To evaluate the coefficient gain blocks, we performed several analysis. To observe the current gain, a DC Sweep simulation was performed by varying the input current and observing the output. To evaluate the current gain (curve slope), a linear regression was performed on MATLAB. The results are presented in Fig. 6.7.

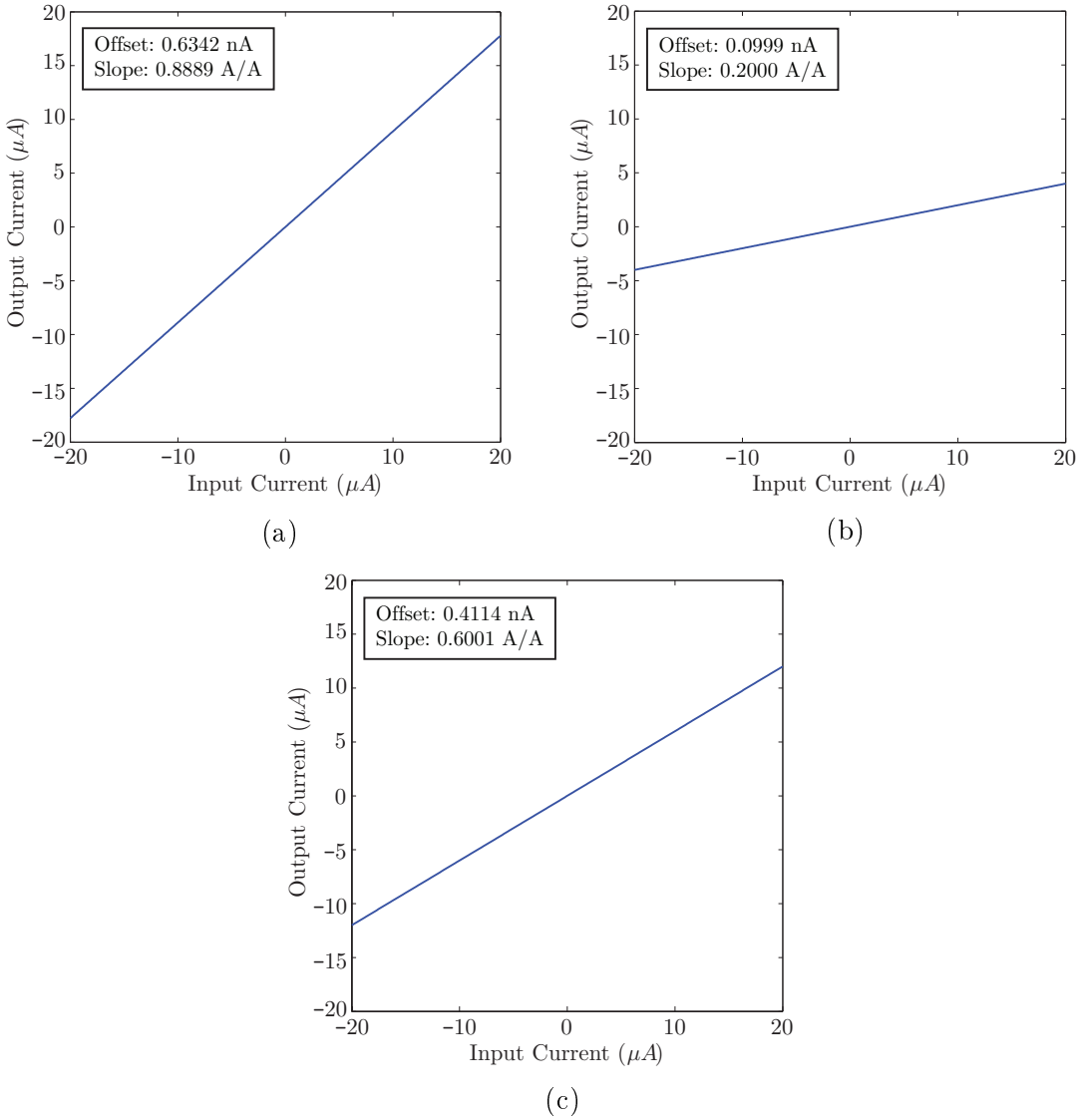


Figure 6.7: Simulation results for the output current with a DC sweep of input current for coefficient (a) $k_{11} = 8/9$, (b) $k_{12} = 1/5$ and (c) $k_{21} = 3/5$.

An AC Sweep simulation was also performed to obtain the frequency response of the coefficients. The cutoff frequency of each coefficient must be higher than the filter bandwidth to guarantee perfect functionality. The results are presented in Fig. 6.8. Since the switching frequency is very low ($\approx 3kHz$), the coefficient gain blocks have no problem to operate in such frequency. The cutoff frequency of each coefficient is highlighted in the figure. Since each block introduces a gain smaller than 1, the cutoff frequency is determined considering the DC gain minus 3 dB.

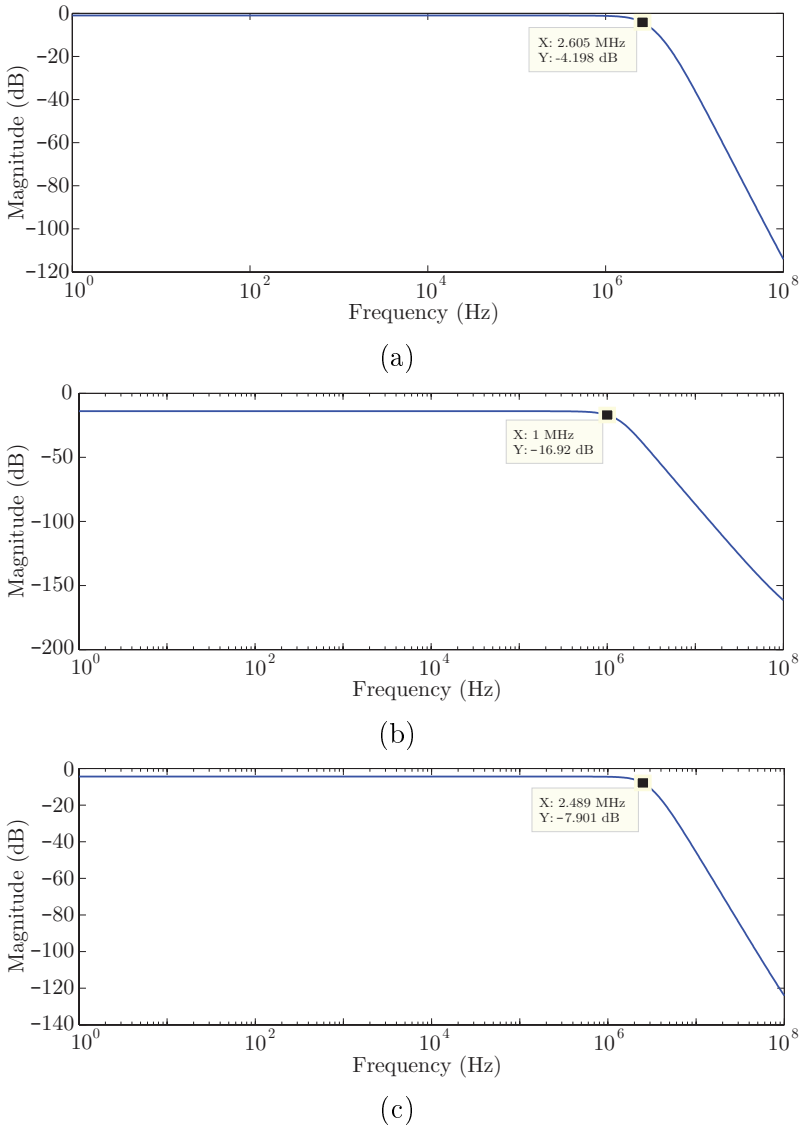
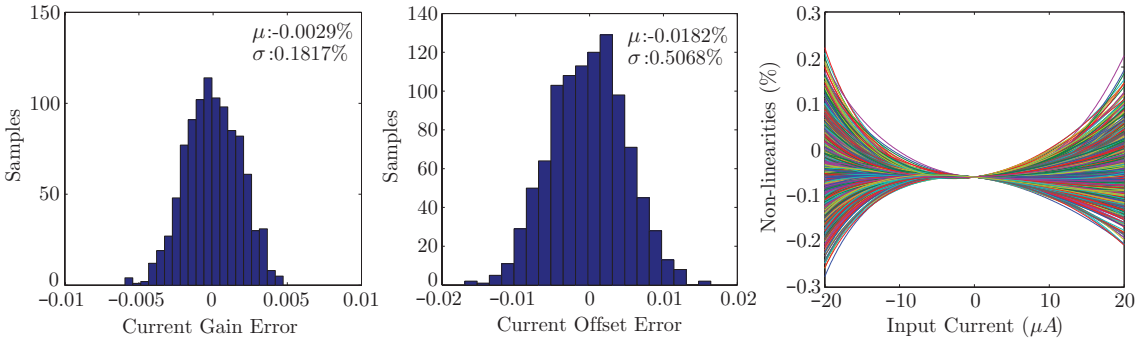


Figure 6.8: Frequency response for coefficient (a) $k_{11} = 8/9$, (b) $k_{12} = 1/5$ and (c) $k_{21} = 3/5$.

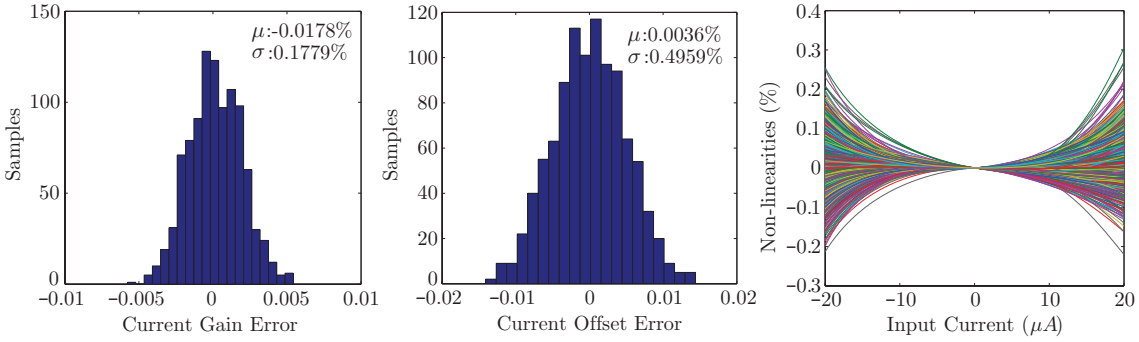
Finally, to observe the coefficient variation with transistor mismatch and process parameters variation, a Monte Carlo simulation was performed with 1000 samples. For each sample of each coefficient, a linear regression was performed and both current gain and offset were obtained. The results for coefficient k_{11}, k_{12} and k_{21} were presented in Fig. 6.9, 6.10 and 6.11, respectively. Each figure presents gain

error, offset and non-linearity errors normalized. The gain error standard deviation achieved was smaller than the aimed yield of $\sigma = 0.333\%$, and linearity errors were under 0.3% for the whole current operation.



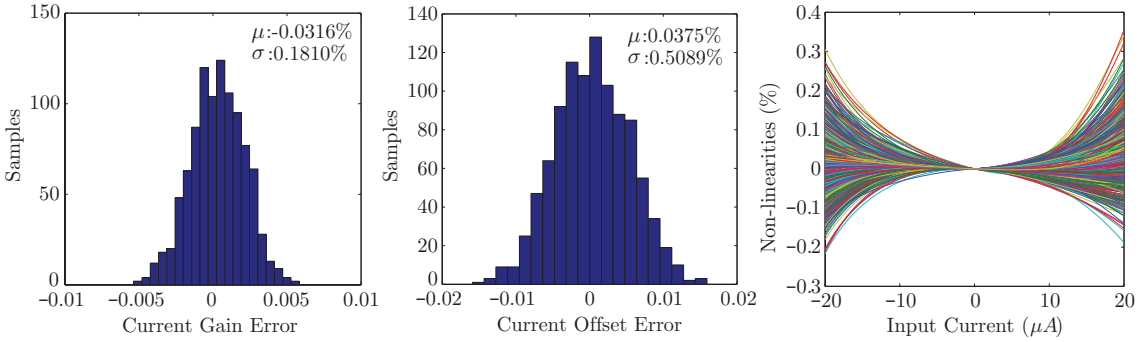
(a) (b) (c)

Figure 6.9: Results for Monte Carlo simulation for coefficient $k_{11} = 8/9$. (a) Gain error, (b) Offset error and (c) Non-linearity errors.



(a) (b) (c)

Figure 6.10: Results for Monte Carlo simulation for coefficient $k_{12} = 1/5$. (a) Gain error, (b) Offset error and (c) Non-linearity errors.



(a) (b) (c)

Figure 6.11: Results for Monte Carlo simulation for coefficient $k_{21} = 3/5$. (a) Gain error, (b) Offset error and (c) Non-linearity errors.

6.3 Differential and Output Copy Current Mirror

Both differential current mirror (DCM) and output copy current mirror (OCCM) are going to operate together as a single block, to copy the output value from the previous structurally all-pass section and generate both positive and negative copies of this value.

The differential current mirror (DCM) is responsible to create two copies of the structurally all-pass section (SAPS) input current. In Chapter 2.3.1, the DCM ideal implementation was presented, and it is repeated here for convenience.

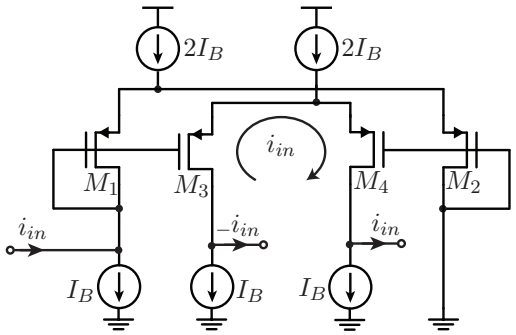


Figure 6.12: Differential current mirror ideal implementation.

This circuit is composed by two identical differential amplifiers, M_1-M_2 and M_3-M_4, with differential inputs connected together. The differential amplifier M_1-M_2 have both transistors diode-connected. The input current i_{in} of M_1-M_2 determines the input differential voltage, which is the same for M_3-M_4. So, a copy of i_{in} is generated in M_3-M_4, but with opposite directions, thus different polarities.

The main design issue from the ideal implementation is the grounded node at transistors M_2 and M_4 gates, which would bring the input node voltage to negative values when i_{in} is negative. A simple way to solve this issue is to bias the node with a higher potential. It is interesting to bias this node with the virtual ground voltage V_B from the memory cell, in order to mitigate channel-length modulation errors between M_2 and M_4, leading to the representation in Fig. 6.13a. To implement the low-impedance node, an amplifier on buffer configuration is used, leading to the implementation in Fig. 6.13b.

The task to be performed by the Output Copy Current Mirror (OCCM) is to copy a current stored by a current memory cell. On an ideal current memory cell, the voltage stored on the gate-source capacitance determines the current value stored by the memory cell. Thus, to copy it, a simple current mirror can be used, as shown in Fig. 6.14.

On the zero-voltage switching CMC used in this work, the voltage is stored by a suspended hold capacitor, and applied on the gates of a high-linearity differential pair. Thus, to generate a copy in the same manner, the whole differential pair should

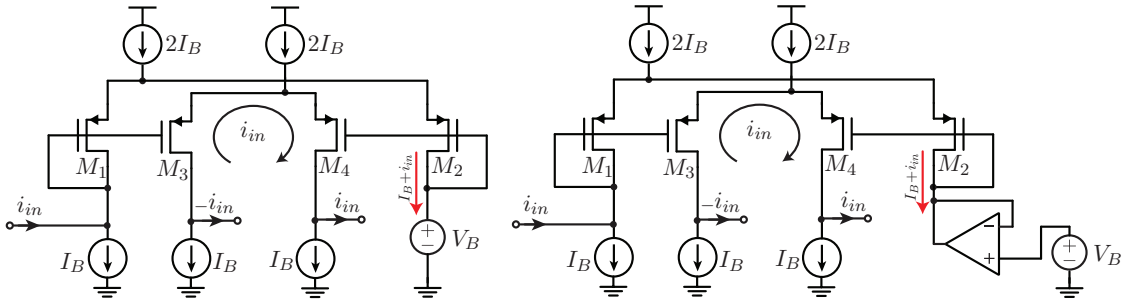


Figure 6.13: Differential current mirror implementation with (a) low-impedance biasing voltage and (b) voltage buffer.

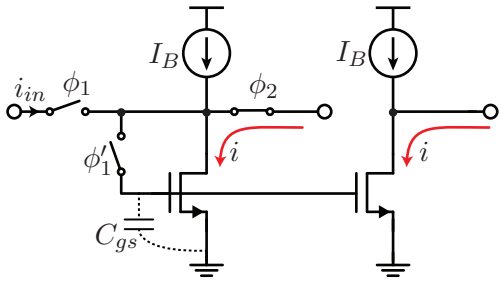


Figure 6.14: Output copy of an ideal current memory cell.

be copied, including its biasing current, making it area inefficient, Moreover, a small difference between the transconductance curves would generate errors in the copied current.

A more efficient manner to generate a copy from the ZVS-CMC is presented in Fig. 6.15. In Fig. 6.15a, when the loop is closed, one can see a current with value $I_B + i_{in}$ flowing into the ground node. If this current is mirrored and the bias current is subtracted, a copy of the stored current is obtained, as shown in Fig. 6.15b.

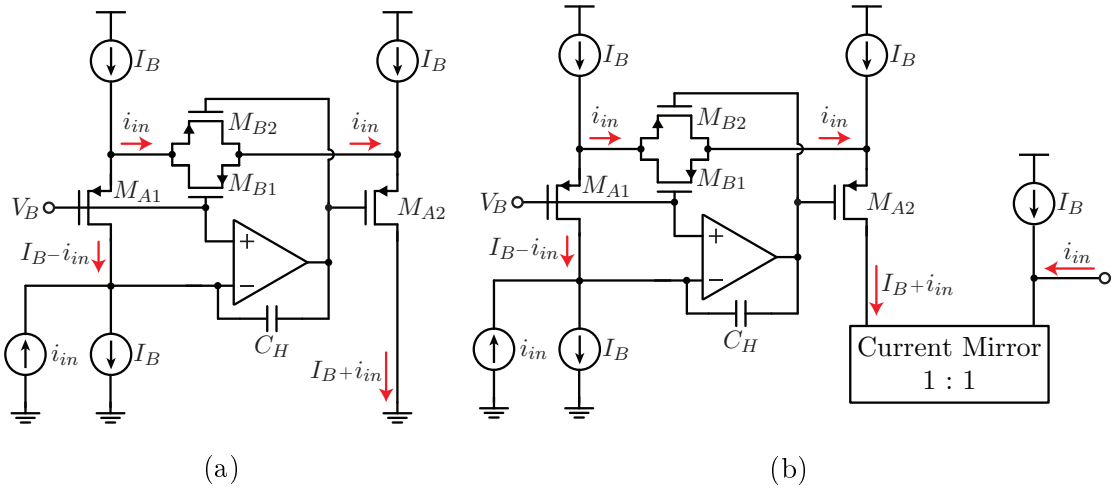


Figure 6.15: (a) Current flow of the zero-voltage switching current memory cell and (b) stored current copy.

The current mirror selected to perform the output copy was a wide-swing cascode current mirror [48, p. 144], due to high-precision and wide-swing of the output voltage. The circuit is presented in Fig. 6.16. The mismatch between transistors can be controlled using Pelgrom's rules [47].

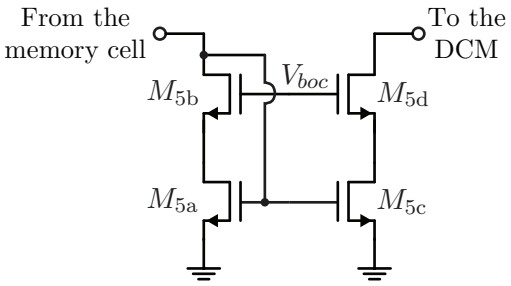


Figure 6.16: Output copy current mirror circuit implementation.

6.3.1 Circuit Design

Both OCCM and DCM make a single block, as pictured in Fig. 6.17. The circuit design of each one is related, thus they are performed together. The four transistors from the DCM (M_1, M_2, M_3 and M_4) have same dimensions, as well as the four transistors of the OCCM (M_{5a}, M_{5b}, M_{5c} and M_{5d}). Transistors transconductance constant will be specified as β_1 for DCM and β_5 for OCCM.

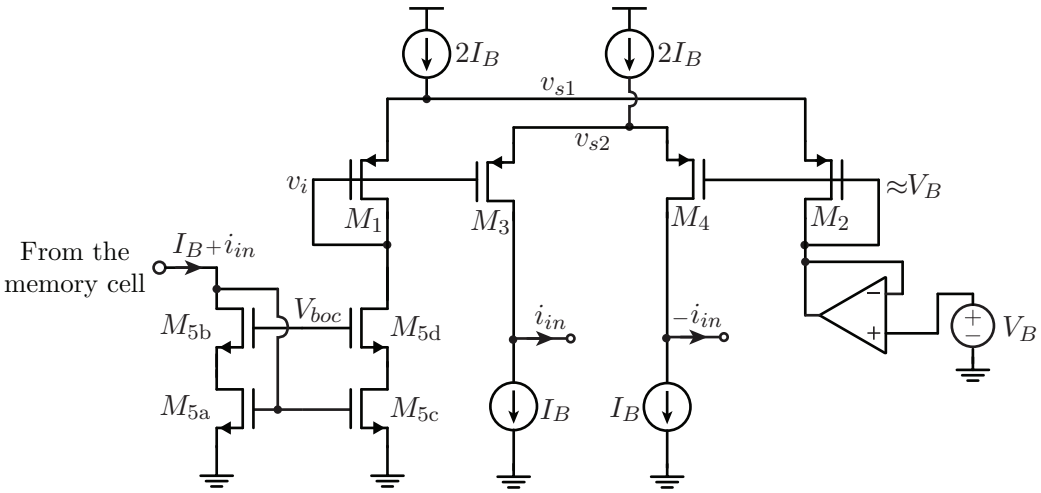


Figure 6.17: Single-block implementation of both differential current mirror and output copy current mirror.

From the circuit of Fig. 6.17, we have

$$I_{D1} = I_B + i_{in} = \frac{\beta_1}{2\alpha_p}\left(V_{s1} - V_i - |V_{T0p}|\right)^2 \tag{6.31}$$

$$I_{D2} = I_B - i_{in} = \frac{\beta_1}{2\alpha_p}\left(V_{s1} - V_B - |V_{T0p}|\right)^2 \tag{6.32}$$

Since V_B is a constant voltage, V_{s1} is given by

$$V_{s1} = \sqrt{\frac{2\alpha_p}{\beta_1}(I_B - i_{in})} + V_B + |V_{T0p}| \tag{6.33}$$

which depends on the input current. The maximum value of V_{s1} is achieved when the input current reaches its minimum value. Since the biasing currents are implemented by current mirrors, V_{s1} should be lower than the biasing current maximum voltage, specified in (6.3) as $V_{oP\text{MAX}}$. Therefore, the condition to be met is

$$\sqrt{\frac{2\alpha_p}{\beta_1}(I_B - i_{in})} + V_B + |V_{T0p}| \leq V_{oP\text{MAX}} \tag{6.34}$$

which can be manipulated to obtain a minimum W/L ratio for DCM transistors, given by

$$\left(\frac{W}{L}\right)_{M_1} \geq \frac{2\alpha_p I_B(1 - m_{i\text{MIN}})}{k_{pp}(V_{oP\text{MAX}} - V_B - |V_{T0p}|)^2} \tag{6.35}$$

where m_i is the modulation index, defined by $m_i = i_{in}/I_B$, and $m_{i\text{MIN}}$ was specified in the CMC design as -0.8. After applying the value for each variable, and transistor parameters from Appendix A, it leads to

$$\left(\frac{W}{L}\right)_{M_1} \geq 0.903 \tag{6.36}$$

To allow clearance for V_{s1}, the ratio chosen was $(W/L)_{M_1} = 2$. To size DCM's transistors, it was developed in Appendix D.6, a Pelgrom model for DCM gain error standard deviation was developed, and in D.7 a Pelgrom model for DCM current offset. The minimum transistor length to achieve a gain error and offset standard deviations of 0.333% (1% for 3σ) is given by

$$L_{M_1} \geq 8.8420\mu m \tag{6.37}$$

To ensure that the condition (6.37) is met loosely, the transistor size was defined by

$$\left(\frac{W}{L}\right)_{M_1,M_2,M_3,M_4} = \frac{30\mu m}{15\mu m} \tag{6.38}$$

The voltage swing of node V_i can be obtained after manipulating and subtracting (6.31) from (6.32), and it is expressed by

$$V_i = V_B + \sqrt{\frac{2\alpha_p I_B}{\beta_1}}\left(\sqrt{1 + m_i} - \sqrt{1 - m_i}\right) \tag{6.39}$$

Since m_i was limited in the CMC design between ± 0.8, the swing limits of V_i are given by

$$V_{i\text{MAX}} \approx V_B + 0.8945\sqrt{\frac{2\alpha_p I_B}{\beta_1}} = 1.555V \tag{6.40}$$

$$V_{i\text{MIN}} \approx V_B - 0.8945\sqrt{\frac{2\alpha_p I_B}{\beta_1}} = 0.645V \tag{6.41}$$

since $(\sqrt{1+0.8} - \sqrt{1-0.8}) \approx 0.8945$. $V_{i\text{MIN}}$ is a design constraint for the OCCM, which minimum realizable W/L ratio was derived in (B.22) and it is given by

$$\left(\frac{W}{L}\right)_{M_5} \geq \frac{2\alpha_n I_B}{k_{pn} V_{i\text{MIN}}^2}\left[\left(1+\frac{1}{\alpha_n}\right)\sqrt{1+0.8} - \left(1-\frac{1}{\alpha_n}\right)\sqrt{1-0.8}\right]^2 = 2.8252 \tag{6.42}$$

and to allow a wider range of voltages for V_{boc}, the ratio was set in $(W/L)_{M_5} = 5$. The V_{boc} range, obtained using (B.17), is given by

$$1.1935 \leq V_{boc} \leq 1.0445 \tag{6.43}$$

from which $V_{boc} = 1.13$ was chosen.

During the system design, it was specified a gain error lower than $\pm 1\%$ for a 3σ yield. Applying Pelgrom rules, described in D.3, into the OCCM, the minimum transistor length to deliver such yield is given by

$$L_{M_5} \geq 26.948\mu m \tag{6.44}$$

and to guarantee it with clearance, it was selected $L = 28\mu m$. Hence, OCCM transistors dimensions are given by

$$\left(\frac{W}{L}\right)_{M_{5a},M_{5b},M_{5c},M_{5d}} = \frac{140\mu m}{28\mu m} \tag{6.45}$$

The last part of the circuit block to be designed is the buffer. The topology selected was a Miller amplifier, two-stage amplifier with feedback capacitor, pictured in Fig. 6.18. The design procedure used here was derived by Allen in [60]. For simplicity, the biasing current of the first stage has the same value as other blocks, and it is provided by the biasing block.

The load capacitance for the amplifier , C_L, is defined by the gate-source capacitance of transistors M_2 and M_4 of the DCM. C_L is estimated by

$$C_L = 2 \times \frac{2}{3} C_{ox} W L \approx 2.8pF \tag{6.46}$$

The condition to achieve a 60° phase-margin is that $C_c > 0.22C_L$ [60], so it was

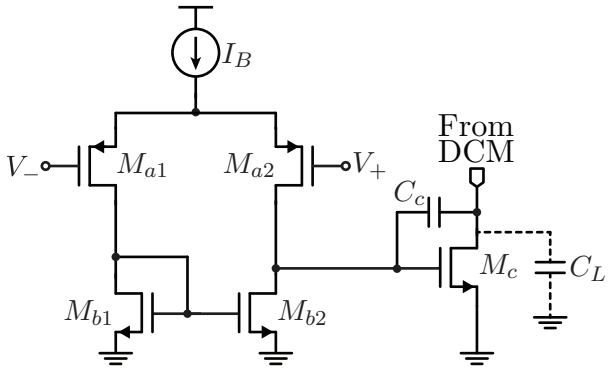


Figure 6.18: Circuit implementation of the differential current mirror amplifier.

chosen $C_c = 1pF$. The current mirror composed by $M_{b1} - M_{b2}$ must operate in strong inversion for good matching and noise properties [61]. Thus, we set

$$\left(\frac{gm}{I_D}\right)_{M_{b1}} = \left(\frac{gm}{I_D}\right)_{M_{b2}} = 10 \tag{6.47}$$

which leads to

$$\left(\frac{W}{L}\right)_{M_{b1,2}} \approx 2.5 \tag{6.48}$$

The same principle can be used for M_c, which has twice the current of M_{b1} and M_{b2}. Thus, the W/L ratio is given by

$$\left(\frac{W}{L}\right)_{M_c} \approx 5 \tag{6.49}$$

With the ratio of M_c defined, its transconductance is given by

$$gm_c = \sqrt{\frac{2I_B k_{pn} W}{\alpha_n L}} \approx 126.445\mu\Omega^{-1} \tag{6.50}$$

The condition to obtain 60° phase-margin is given by [60]

$$\frac{gm_c}{C_L} \geq 2.2\frac{gm_a}{C_c} \tag{6.51}$$

which leads to

$$gm_a \leq 20.52\mu\Omega^{-1} \rightarrow \left(\frac{W}{L}\right)_{M_{a1,2}} \leq 0.6899 \tag{6.52}$$

and the final choice was $(W/L)_{M_{a1,2}} = 0.5$. Transistor sizing for M_{b1}, M_{b2} and M_c is done by choosing its length at least five times higher than minimum size allowed by the technology to reduce channel length modulation effects, hence

$$\left(\frac{W}{L}\right)_{M_{b1,2}} = \frac{5\mu m}{2\mu m} \; ; \left(\frac{W}{L}\right)_{M_c} = \frac{10\mu m}{2\mu m} \tag{6.53}$$

To size the input differential pair, the offset standard deviation must be taken into account. Since the main purpose of the amplifier is to hold the voltage at the gates of M_2 and M_4 from the DCM, its offset should have a small variance. Using Pelgrom models derived in Appendix D.5, the minimum length to obtain an offset variation of $10mV$ ($\pm 3\sigma$) is given by

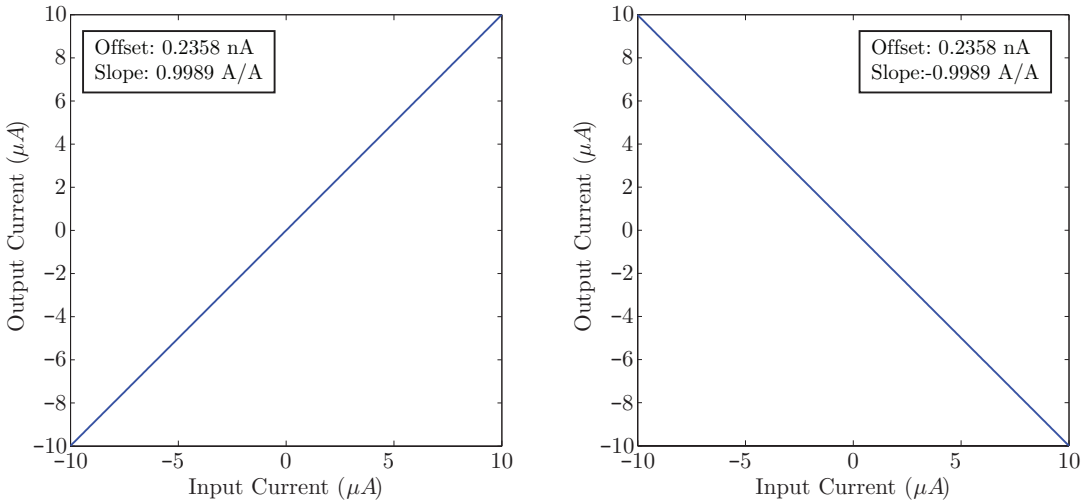
$$L_{a\text{MIN}} = \frac{1}{\sigma}\sqrt{\frac{\alpha I_B}{k_p R^2} \cdot \hat{A}_{k_p}^2 + \frac{2V_{T0}^2}{R} \cdot \hat{A}_{V_{T0}}^2} = 6.354\mu m \tag{6.54}$$

hence the final sizing is given by

$$\left(\frac{W}{L}\right)_{M_{a1,2}} = \frac{4\mu m}{8\mu m} \tag{6.55}$$

6.3.2 Simulation Results

To evaluate the building block composed by both output copy and differential current mirror, a DC sweep simulation was performed. The input current was swept from $-10\mu A$ to $10\mu A$. The result is presented in Fig. 6.19. Notice that the slope value is equal for both outputs, showing the symmetry properties of the block.



(a) (b)

Figure 6.19: Results for a DC sweep of the input current for (a) positive output current and (b) negative output current.

An AC sweep simulation was perform to observe the frequency limits. The results are presented in Fig. 6.20. The cutoff obtained of 872.2 kHz is much greater than the switching frequency of the system. Hence it has no issues with settling time.

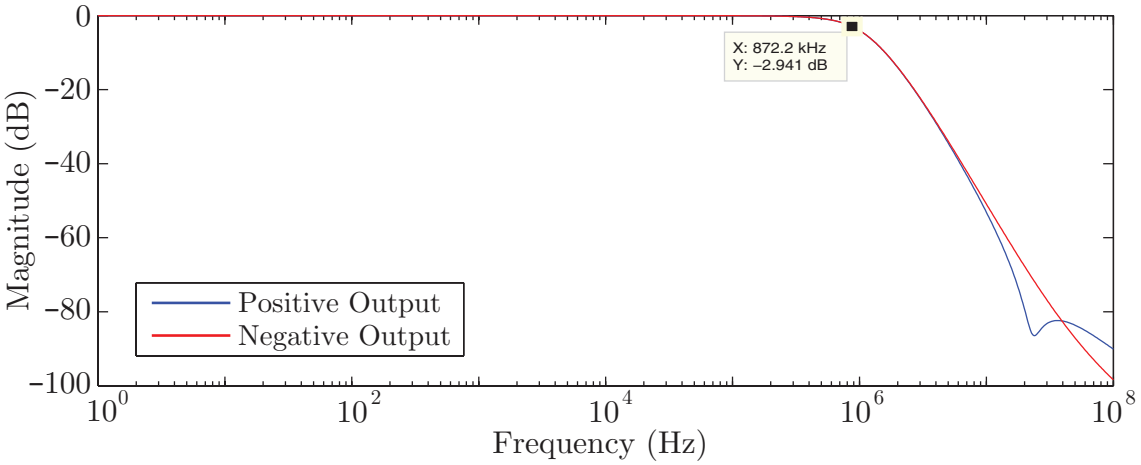


Figure 6.20: Frequency response for positive output (blue trace) and negative output (red trace).

Finally, to observe circuit behavior under mismatch and process parameters variation, a Monte Carlo simulation was performed with 1000 samples. The resulting curves are presented in Fig. 6.21. One can notice a small variation around the nominal curves.

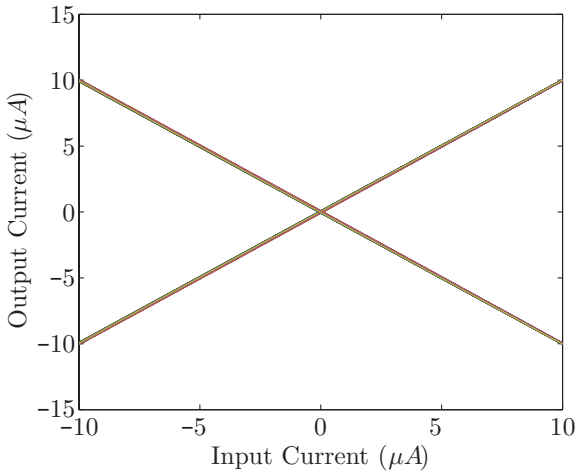


Figure 6.21: Monte Carlo simulation results for both outputs.

For each positive and negative output, a linear regression was performed using MATLAB to obtain gain and offset. The values for each sample were compared with the ideal values and both gain errors and offset were obtained. With a linear version of each output sample, non-linearity errors were obtained by subtracting the linear version from real output. The results are presented in Fig. 6.22 for the positive output and Fig. 6.23 for the negative output.

From the Monte Carlo result, it can be seen that both outputs have same offset and gain error standard deviation. The symmetry properties of the DCM is an important asset for a good operation of the system. Also, it can be seen that the

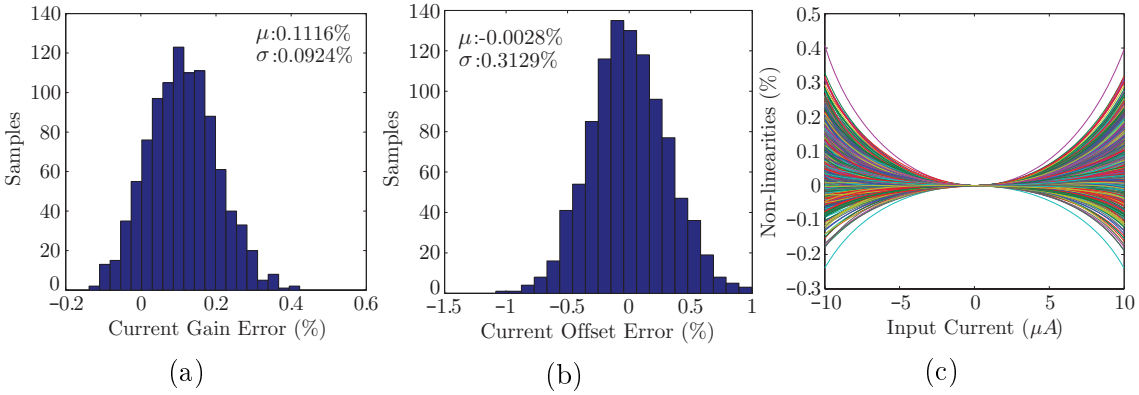


Figure 6.22: Results for Monte Carlo simulation for the positive output. (a) Gain error, (b) Offset error and (c) Non-linearity errors.

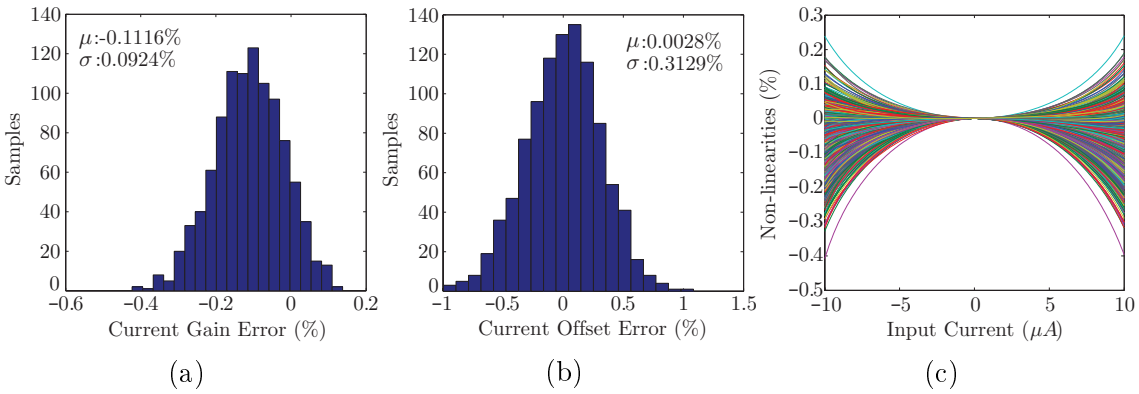


Figure 6.23: Results for Monte Carlo simulation for the negative output. (a) Gain error, (b) Offset error and (c) Non-linearity errors.

standard deviation were under the desired yield, validating the design.

6.4 Current Multiplier

The current multiplier is the last building to be implemented in our system. The circuit designed here is based on a work presented by Manganaro [62]. His current multiplier is interesting since it uses switched current techniques.

The multiplication of any two given current x and y is obtained by evaluating their quadratic terms, hence

$$(x+y)^2 - x^2 - y^2 = 2xy \tag{6.56}$$

The basic behavior of the circuit is presented in Fig. 6.24 and its switching sequence is pictured in Fig. 6.25. It operates in four phases, thus each current memory cell introduces a 1/4 unit delay. The main idea is to evaluate each quadratic term ($(x+y)^2$, x^2 and y^2) in each phase, occupying three phases. The other phase is used for systematic offset cancellation.

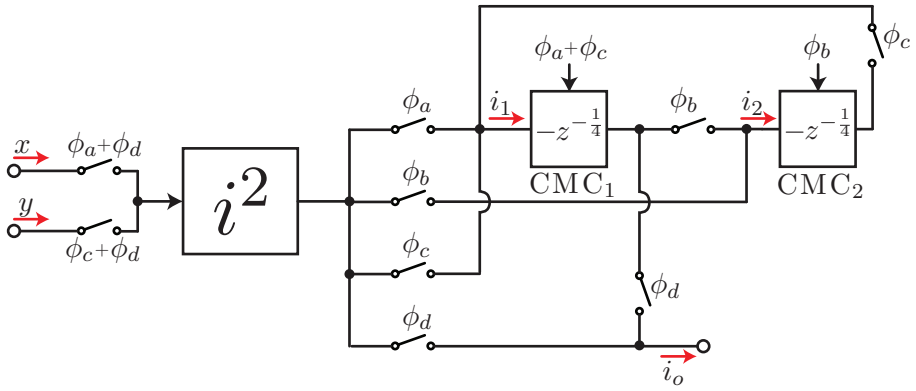


Figure 6.24: Current multiplier basic behavior.

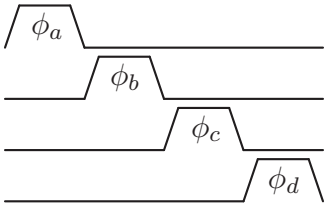


Figure 6.25: Current multiplier switching sequence.

For proper operation, x and y must be kept constant through four phases. It works as follows. Starting from phase ϕ_a, only current x is squared and is stored into CMC$_1$. Hence,

$$i_1(\phi_a) = x^2 \tag{6.57}$$

During the second phase ϕ_b, no current is squared. The previous current stored at CMC$_1$ is introduced at CMC$_2$ input. This phase will be used to cancel systematic offset on the actual transistor level implementation. Since the quarter-unit delay also introduces a signal inversion, we obtain

$$i_2(\phi_b) = -i_1(\phi_a) = -x^2 \tag{6.58}$$

During phase ϕ_c, only current y is squared and it is introduced at CMC$_1$ input, together with the previous current stored at CMC$_2$. Hence

$$i_1(\phi_c) = y^2 - i_2(\phi_b) = x^2 + y^2 \tag{6.59}$$

At the final phase ϕ_d, both inputs x and y are summed and squared. They are delivered at the output together with the previous current stored at CMC$_1$ to obtain the output i_o, given by

$$i_o = (x+y)^2 - i_1(\phi_c) = (x+y)^2 - y^2 - x^2 = 2xy \tag{6.60}$$

One of the biggest advantages of this architecture is the use of the same current squarer to obtain each quadratic component, therefore eliminating mismatch errors between current squarers that occurs in continuous time current multipliers. Also, the use of four phases eliminates some second order effects from transistors. The transistor level implementation is detailed on the next subsection.

6.4.1 Transistor Level Implementation

Since the current memory cells were already design, the challenge is to realize the current squarer. The circuit used here was presented in [62], and it is shown in Fig. 6.26. The current transfer was derived in Appendix B.3. The choice of using PMOS instead of NMOS is due to the connection of bulk and source of transistors M_{1a} and M_{1d}, therefore eliminating body effect. Also, to reduce channel length modulation effects in M_{1c}, a basic regulated cascode current mirror was used [63].

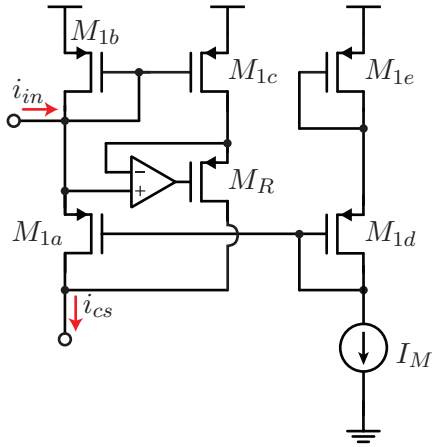


Figure 6.26: Current squarer circuit implementation.

From (B.56), the current transfer is given by

$$i_{cs} = 2I_M + \frac{i_{in}^2}{8I_M} \tag{6.61}$$

where I_M is a design choice. To subtract the DC term, a current source with value $2I_M$ is added at the output. The complete circuit is presented in Fig. 6.27. Since the output node of the current squarer is always connected to a current memory cell, there will be a virtual ground at node V_o in every phase. Also, as explained in Chapter 5.1.4, there are current switches and voltage switches, where the previous one requires overlap phases (subscript i) and the latter one non-overlap phases (subscript v).

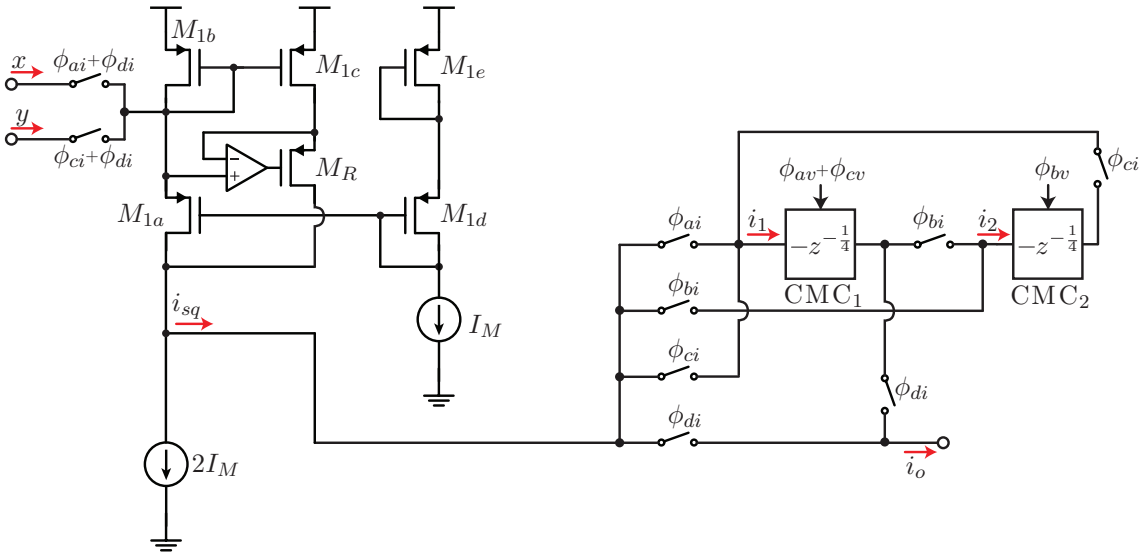


Figure 6.27: Complete circuit implementation of the current multiplier.

6.4.2 Systematic Error Cancellation

From the circuit of Fig. 6.27, one can see that

$$i_{sq} = \frac{i_{in}^2}{8I_M} \tag{6.62}$$

However, due to mismatch and second order effects this current curve might not be a perfect parabola. Instead, an offset and a linear term might also occur [62]. Consider i_{sq} to be expressed as

$$i_{sq} = a_0 i_{in}^2 + a_1 i_{in} + a_2 \tag{6.63}$$

which can be rearranged in the form

$$i_{sq} = I_{os1} + \frac{(i_{in} + I_{os2})^2}{8I'_M} \tag{6.64}$$

One can see that $a_0 = 1/8I'_M$, $a_1 = I_{os2}/4I'_M$ and $a_2 = I_{os1} + I_{os2}^2/8I'_M$, where I_{os1} and I_{os2} are offset currents and I'_M might differ from the actual I_M value due to mismatch errors. The same procedure executed before can be used again. Starting from phase ϕ_a, only current x is squared and is stored into CMC$_1$. Hence,

$$i_1(\phi_a) = I_{os1} + \frac{(x + I_{os2})^2}{8I'_M} \tag{6.65}$$

During the second phase ϕ_b, no current is introduced to the system. However, the independent terms are added to the output, together with the previous current stored at CMC$_1$. Since the quarter-unit delay also introduces a signal inversion, we obtain

$$i_2(\phi_b) = I_{os1} + \frac{I_{os2}^2}{8I'_M} - i_1(\phi_a) = \frac{I_{os2}^2}{8I'_M} - \frac{(x + I_{os2})^2}{8I'_M} \tag{6.66}$$

During phase ϕ_c, only current y is squared and it is introduced at CMC_1 input, together with the previous current stored at CMC_2. Hence

$$i_1(\phi_c) = I_{os1} + \frac{(y + I_{os2})^2}{8I'_M} - i_2(\phi_b) \tag{6.67}$$

At the final phase ϕ_d, both inputs x and y are summed and squared. They are delivered at the output together with the previous current stored at CMC_1 to obtain the output i_o, given by

$$i_o = I_{os1} + \frac{(x + y + I_{os2})^2}{8I'_M} - i_1(\phi_c) \tag{6.68}$$

$$i_o = \frac{(x + y + I_{os2})^2}{8I'_M} - \frac{(y + I_{os2})^2}{8I'_M} - \frac{(x + I_{os2})^2}{8I'_M} + \frac{I_{os2}^2}{8I'_M} \tag{6.69}$$

Each quadratic term can be expanded, leading to

$$i_o = \frac{1}{8I'_M}\left[(x + y + I_{os2})^2 - (y + I_{os2})^2 - (x + I_{os2})^2 + I_{os2}^2\right] \tag{6.70}$$

$$i_o = \frac{1}{8I'_M}\left[x^2 + y^2 + I_{os2}^2 + 2xy + 2xI_{os2} + 2yI_{os2} - (y^2 + I_{os2}^2 + 2yI_{os2})\right.$$
$$\left. - (x^2 + I_{os2}^2 + 2xI_{os2}) + I_{os2}^2\right] \tag{6.71}$$

Most of the terms can be canceled, and the final result is given by

$$i_o = \frac{xy}{4I'_M} \tag{6.72}$$

As it was showed, most of the systematic errors are eliminated in the multiplication process. Also, a deviation from I_M can be considered a gain error, and it can be compensated with a calibration routine, as explained earlier in Chapter 4.3.3. It is also mitigated using Pelgrom models for current mirrors. With the gain error, i_o can be expressed by

$$i_o = (1 + \alpha_M)\frac{xy}{4I_M} \tag{6.73}$$

hence

$$I'_M = \frac{I_M}{1 + \alpha_M} \tag{6.74}$$

6.4.3 Circuit Design

Besides the amplifier, the main design to be executed is to size squarer's transistor. From Fig. 6.26, transistors M_{1a}, M_{1b}, M_{1c}, M_{1d} and M_{1e} must have the same dimension. Transistor M_R is only responsible to regulate the voltage at M_{1c} drain, so it can have a different size if necessary. The equations used here were derived in Appendix B.3.

The maximum input current is given when both x and y have maximum values. Since x and y are provided by current memory cells, we have

$$i_{in\text{MAX}} = 10\mu A + 10\mu A = 20\mu A \tag{6.75}$$

Also, the output node from the current squarer operates on a virtual ground, since it always load on a current memory cell. Hence

$$V_{o\text{MAX}} = 1.1 \tag{6.76}$$

With these information, we can obtain the minimum biasing current I_M, which is given by (B.77) and its repeated here, hence

$$I_{M\text{MIN}} = \frac{i_{in\text{MAX}}}{4}\left[\frac{(1+\alpha_p\sqrt{A_v})^2 - A_v}{1 - A_v(\alpha_p+1)^2}\right] \tag{6.77}$$

where A_v is given by (B.72) and it can be adapted for PMOS transistors, leading to

$$A_v = \frac{40\phi_T^2}{(V_{DD} - V_{o\text{MAX}} - V_{T0p})^2} \approx 1.2789 \cdot 10^{-2} \tag{6.78}$$

which leads $I_{M\text{MIN}}$ to

$$I_{M\text{MIN}} = 7.005\mu A \tag{6.79}$$

Since the final result of the multiplication is inversely proportional to the biasing current, the bigger the biasing current I_M, less dynamic range is obtained at the output. Thus, it was selected $I_M = 10\mu A$. With I_M defined, the ratio for transistors M_{1a}-M_{1e} is upper-bounded by (B.61) and lower-bounded by (B.69). Hence it can be between the range

$$2.0451 \leq \left(\frac{W}{L}\right)_1 \leq 0.6357 \tag{6.80}$$

and the final choice was $(W/L)_1 = 1.4$. Using Pelgrom models for current mirrors, to have a small deviation from I_M value in the output, a yield of 0.5% for 3σ was specified. The minimum length for such yield is obtained using (D.25), which leads to

$$L_{1\text{MIN}} = 27.736\mu m \tag{6.81}$$

and the final dimension for transistors M_{1a}-M_{1e} is given by

$$\left(\frac{W}{L}\right)_{1a,1b,1c,1d,1e} = \frac{42\mu m}{30\mu m} \tag{6.82}$$

To reduce ΔV_{sg} of M_R, the length was reduced. Width was kept to improve matching, leading to

$$\left(\frac{W}{L}\right)_R = \frac{42\mu m}{5\mu m} \tag{6.83}$$

To design the amplifier, a similar procedure from the DCM amplifier was used. However, since the input voltage levels are quite high, the input differential pair was implemented with NMOS transistors. The amplifier implementation is presented in Fig. 6.28.

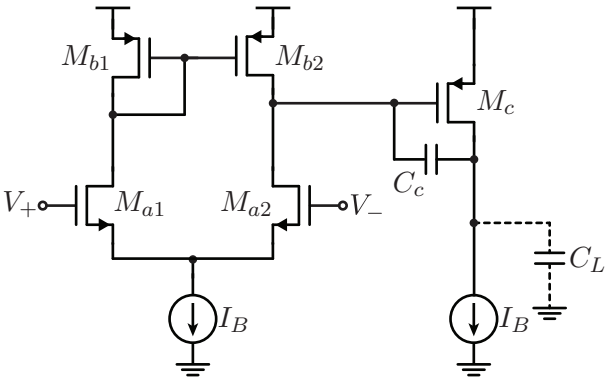


Figure 6.28: Circuit implementation of the regulated cascode amplifier.

The load capacitance for the amplifier, C_L, is defined by the gate-source capacitance of transistor M_R. C_L is estimated by

$$C_L = \frac{2}{3} C_{ox} W L \approx 650fF \tag{6.84}$$

The condition to achieve a 60° phase-margin is that $C_c > 0.22C_L$ [60], so it was chosen $C_c = 300fF$. The current mirror composed by $M_{b1} - M_{b2}$ must operate in strong inversion, and to guarantee it, the inversion coefficient from EKV model is used. Hence

$$IC_{M_{b1}} = IC_{M_{b2}} = \frac{\frac{I_B}{2}}{2\alpha_p \phi_T^2 k_{pp} (\frac{W}{L})_b} \geq 10 \tag{6.85}$$

which leads to

$$\left(\frac{W}{L}\right)_{M_{b1,2}} \leq 5.112 \tag{6.86}$$

from which it was chosen $(W/L)_b = 4$. To avoid channel length modulation effects, the final size is given by

$$\left(\frac{W}{L}\right)_{M_{b1,2}} = \frac{4\mu m}{1\mu m} \tag{6.87}$$

The same principle can be used for M_c, which has twice the current of M_{b1} and M_{b2}. Thus, for equilibrium, the W/L ratio is given by

$$\left(\frac{W}{L}\right)_{M_c} = \frac{8\mu m}{1\mu m} \tag{6.88}$$

With the ratio of M_c defined, its transconductance is given by

$$gm_c = \sqrt{\frac{2I_B k_{pp} W}{\alpha_n L}} \approx 98.848\mu\Omega^{-1} \tag{6.89}$$

The condition to obtain 60° phase-margin is given by [60]

$$\frac{gm_c}{C_L} \geq 2.2\frac{gm_a}{C_c} \tag{6.90}$$

which leads to

$$gm_a \leq 20.737\mu\Omega^{-1} \rightarrow \left(\frac{W}{L}\right)_{M_{a1,2}} \leq 0.2689 \tag{6.91}$$

and the final choice was $(W/L)_{M_{a1,2}} = 1/4$. To improve matching properties,

$$\left(\frac{W}{L}\right)_{M_{a1,2}} = \frac{1\mu m}{4\mu m} \tag{6.92}$$

6.4.4 Circuit Simulation

To evaluate the current multiplier, both the current squarer and the whole multiplier must be evaluated. Starting with the current squarer, the first simulation was a DC Sweep. The input current was swept from $-20\mu A$ to $20\mu A$ and the output was observed. The result is presented in Fig. 6.29.

From the result, a curve fit was performed in MATLAB, and it was obtained

$$i_{sq-fit} = 0.011984 i_{in}^2 - 1.34854 \cdot 10^{-4} i_{in} - 0.012835 \tag{6.93}$$

where i_{in} and i_{sq} are given in μA. From these terms, both offsets and gain error can be obtained, hence

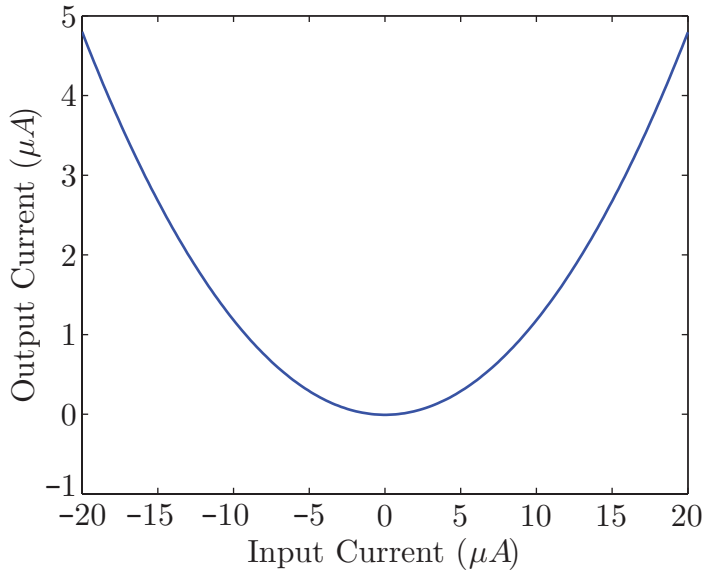


Figure 6.29: Output current result for a DC sweep of the input current.

$$\alpha_M = -0.041277;\ I_{os1} = -12.8355nA;\ I_{os2} = -5.6264nA \tag{6.94}$$

The difference between the fitted curve and the actual curve is considered non-linearity. The non-linearity curve is expressed by

$$\mathrm{NL}(\%) = \frac{i_{sq} - i_{sq-fit}}{i_{sq\mathrm{MAX}}} \tag{6.95}$$

and results in Fig. 6.30.

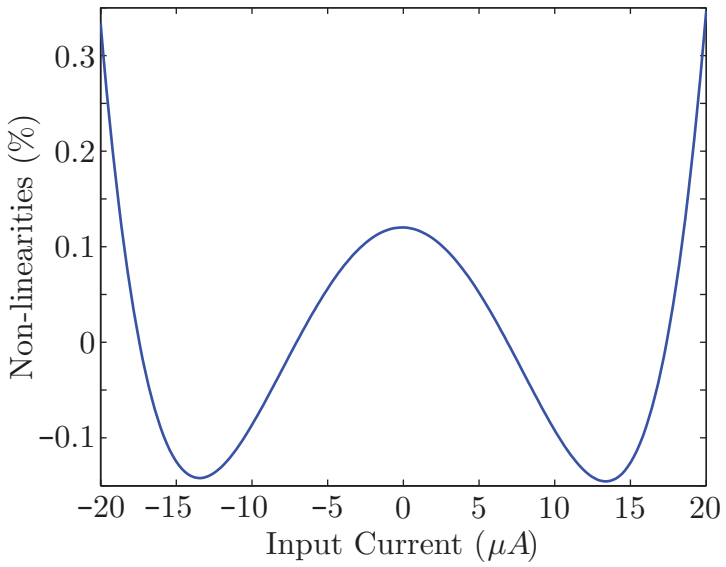


Figure 6.30: Non-linearity errors for the current squarer.

An interesting simulation to observe the squaring behavior is to introduce a saw-tooth waveform at the input and observe a formation of parabolas at the output. A

transient simulation was performed with a $1kHz$ saw-tooth input from $-20\mu A$ to $20\mu A$. The results are shown in Fig 6.31.

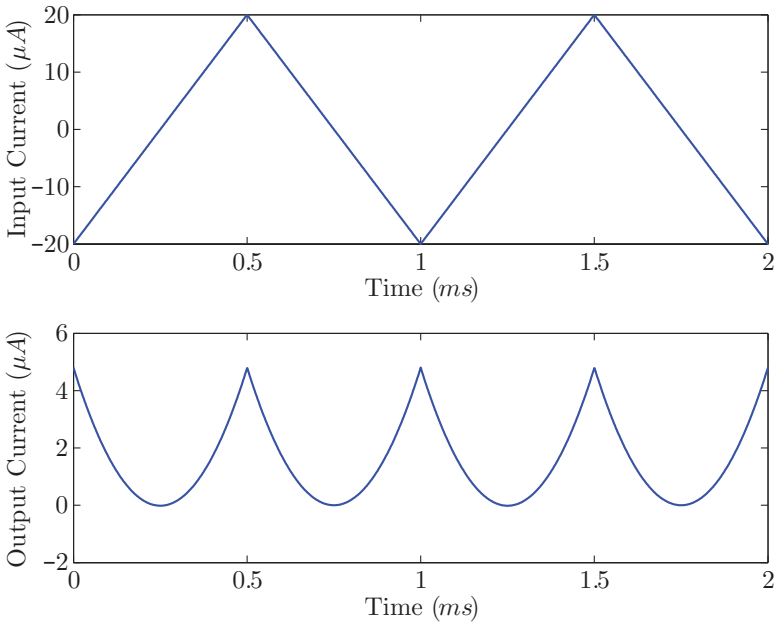


Figure 6.31: Transient results for an $1kHz$ saw-tooth input.

To observe the behavior of the current squarer under mismatch and process parameters variation, a Monte Carlo simulation with 1000 samples was executed. For the Monte Carlo, the input was swept from $-20\mu A$ to $20\mu A$ and the output was observed, resulting into the plot from Fig. 6.32.

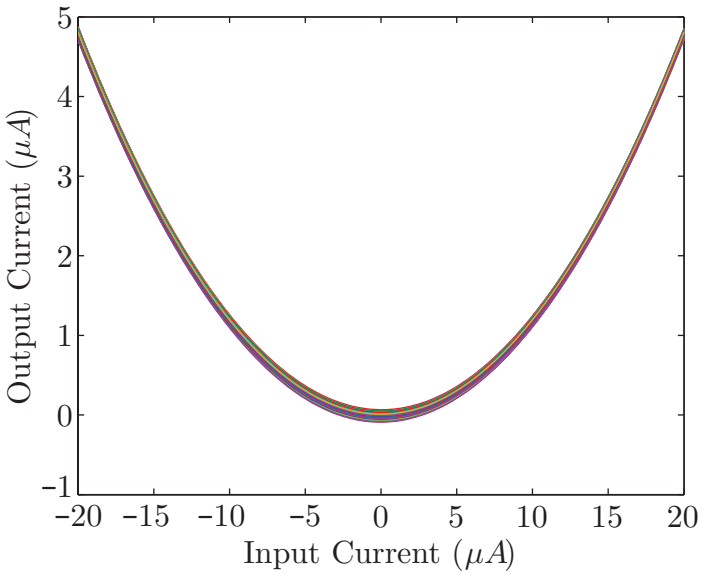
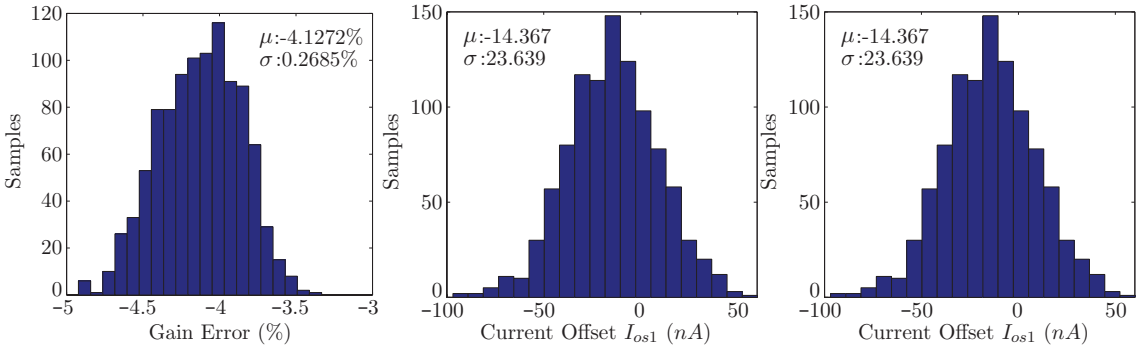


Figure 6.32: Monte Carlo result for the current transfer curve of the current squarer.

For each resulting curve of Fig. 6.32, a curve fitting was performed and data for gain and offsets were obtained. The data histogram is presented in Fig. 6.33.



(a) (b) (c)

Figure 6.33: Histograms for the curve fit of the Monte Carlo simulation resultant data. (a) Gain error α_M, (b) Current offset I_{os1} and (c) Current offset I_{os2}.

With the fitted curve, non-linearity errors can be obtained using (6.95), plotted in Fig. 6.34. The current squarer behavior in the Monte Carlo simulation was very robust, presenting small variation when compared with the nominal result. Also, since only one squarer is needed to implement the current multiplier, further error reduction is expected.

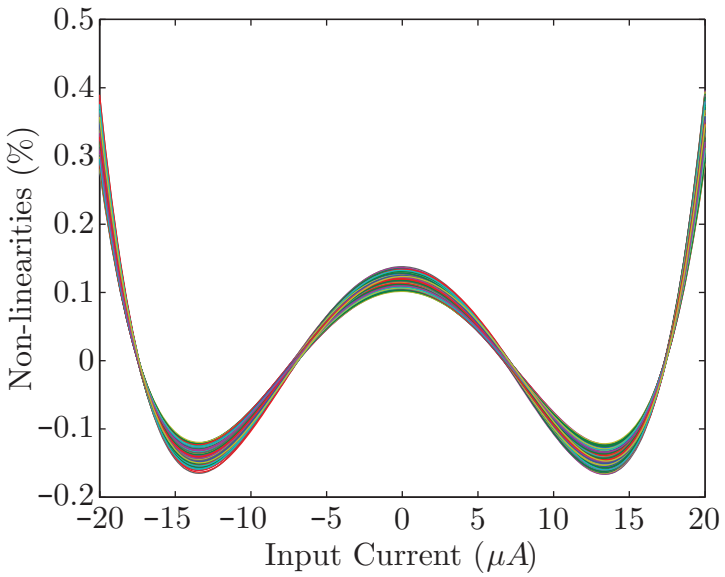


Figure 6.34: Monte Carlo results for the non-linearity errors.

After evaluating the current squarer, the whole multiplier block is also tested. Since it is a dynamic block and requires four phases to operate, a transient analysis must be performed to obtain the multiplication result. To test the circuit, the input x was kept at a constant level and a staircase waveform was introduced at input y. Since x is kept constant, the multiplier output is expected to be linear dependent to y. This analysis was made for 5 different values of x, resulting in Fig. 6.35.

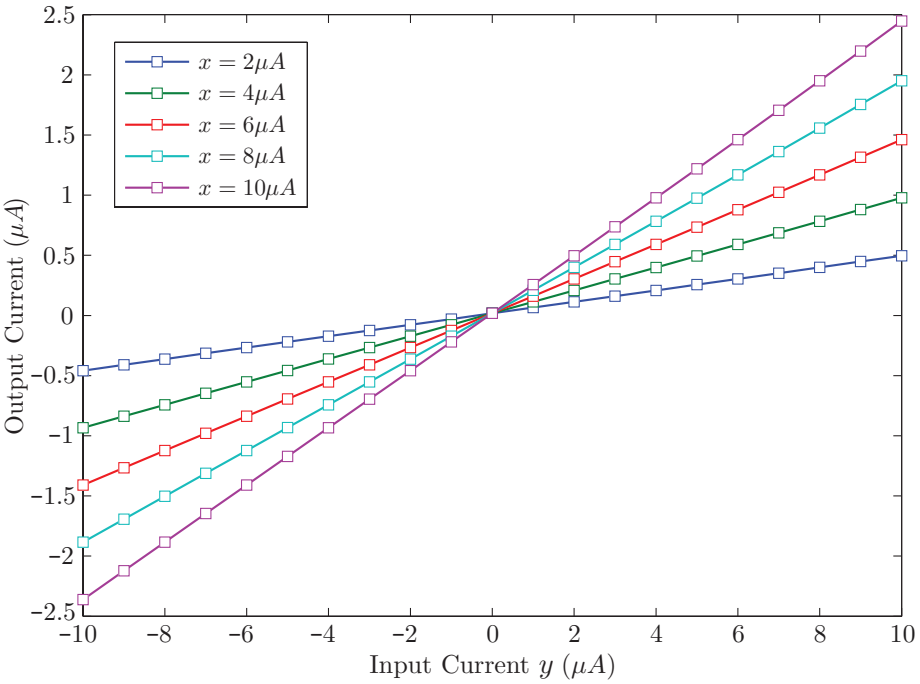


Figure 6.35: Simulated transfer characteristics of the current multiplier, i_o vs. y. x is kept constant at different levels detailed by plot legend.

Finally, to evaluate the multiplier behavior with mismatch and parameters variation, a Monte Carlo simulation with 100 samples was performed. Instead of 5 different values of x, this time it was a fixed DC current of $5\mu A$. The result of the Monte Carlo is presented in Fig. 6.36. One can see that the deviation is very small, showing strong robustness of the multiplier.

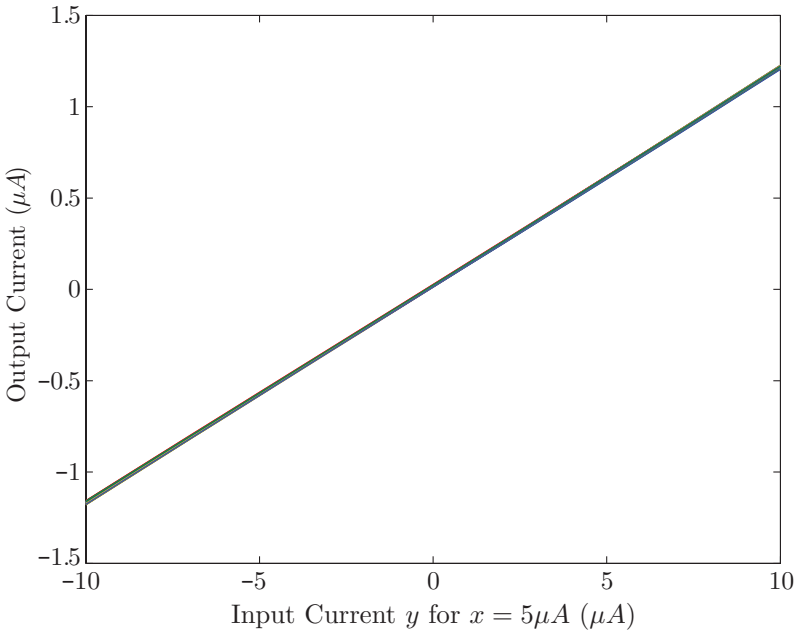


Figure 6.36: Monte Carlo simulation results of the transfer characteristics of i_o vs. y when $x = 5\mu A$.

To observe the deviation, a linear regression was performed to obtain the slope of each sample. The slope results were displayed in the histogram from Fig. 6.37, with a standard deviation of $\sigma = 3.9569 \cdot 10^{-4}$, very small when compared with the mean slope of $\mu = 0.1191$.

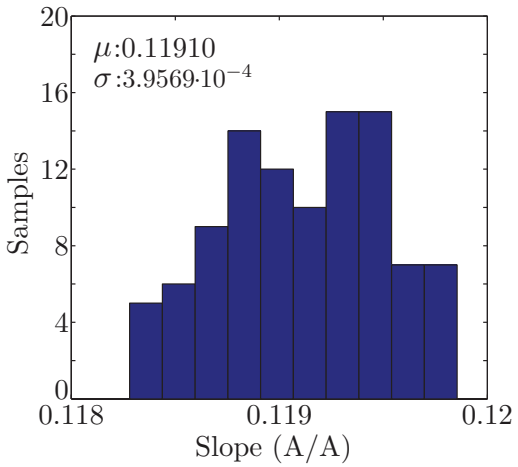


Figure 6.37: Histogram of the slope obtained for each Monte Carlo output sample.

Chapter 7

System Simulation

In this chapter, a series of simulations were performed to characterize the proposed Reactive Power Measurement System (RPMS). First, an overview of the complete system is performed, followed by a filter characterization. Many transient simulation results are presented, as well as a Monte Carlo simulation to observe circuit variability.

7.1 Final System

The RPMS with a shared multiplier was presented in Fig. 4.4 and is repeated here for convenience.

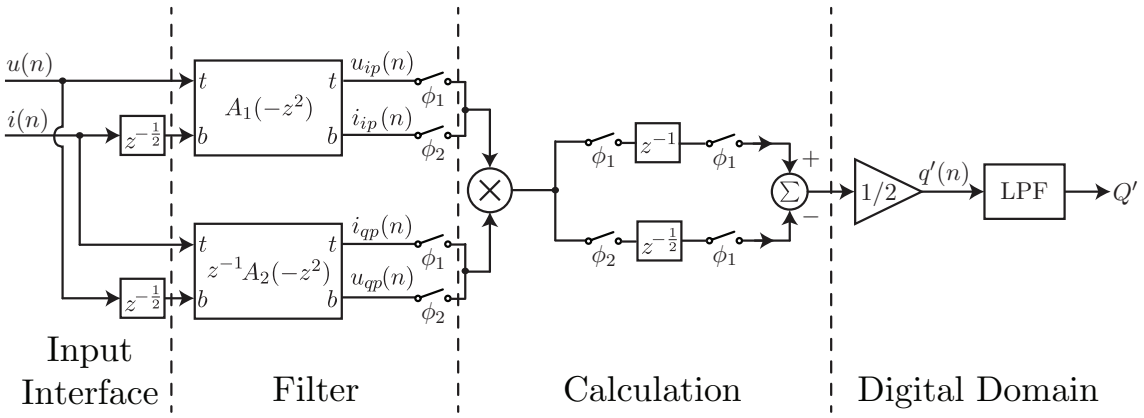


Figure 7.1: Reactive power measurement system block diagram.

The system can be separated into four parts: Input Interface, Filter, Calculation and Digital Domain. As explained before, our focus is the analog-domain signal processing, and MATLAB will be used to perform the digital domain operation. The other three parts were implemented using the circuit blocks designed in the two previous chapters, represented using the blocks in Fig. 7.2 The 'copy' port in the current memory cell is used to obtained the current copy, as explained in Chapter 6.3.

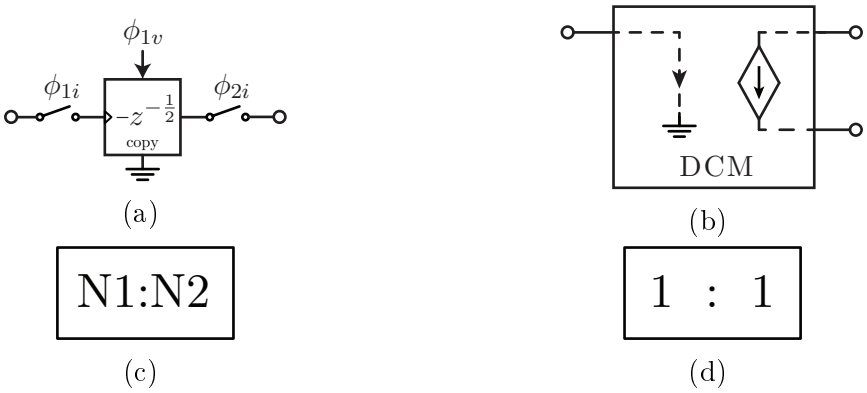


Figure 7.2: Representation of each circuit block. (a) Current Memory Cell, (b) Differential Current Mirror, (c) Coefficient Gain Block and (d) Output Copy Current Mirror.

The input interface part is implemented using the diagram of Fig. 7.3. The first memory cell is a current sample and hold, to transform a continuous time signal into a discrete time signal. To split the current into two paths, the differential current mirror is used and a current memory cell is put at its output to compensate the signal inversion of the current sample and hold.

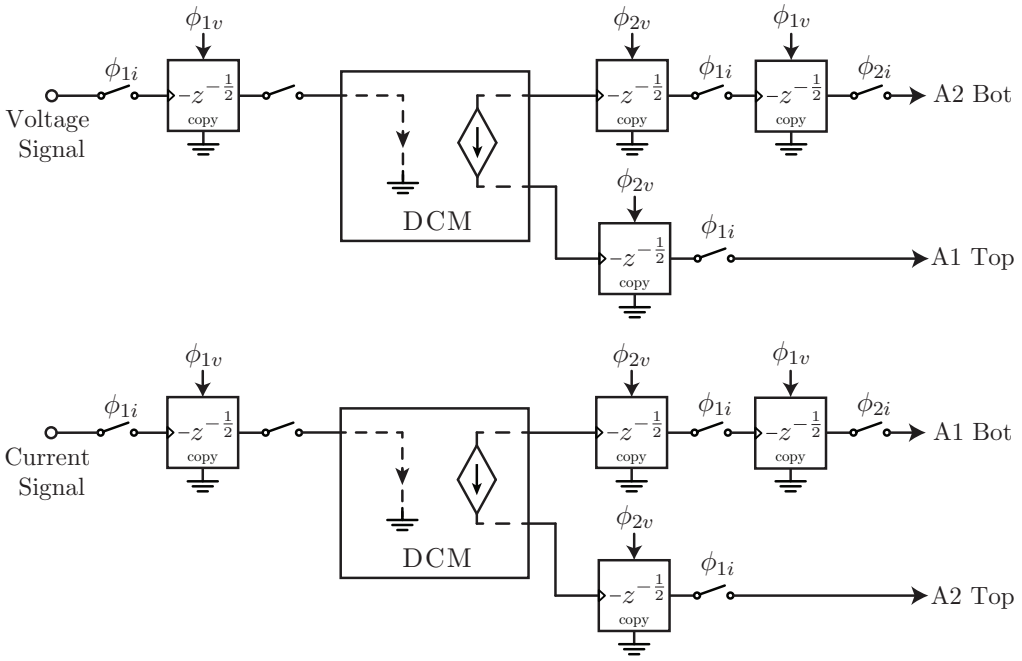


Figure 7.3: Reactive power measurement system input interface diagram.

The filter part is implemented using the diagram of Fig. 7.4. Notice that both differential current mirror (DCM) and output copy current mirror (OCCM) are shared by each filter path. This allows some gain error cancellation, as explained in the Error Analysis from Appendix C.

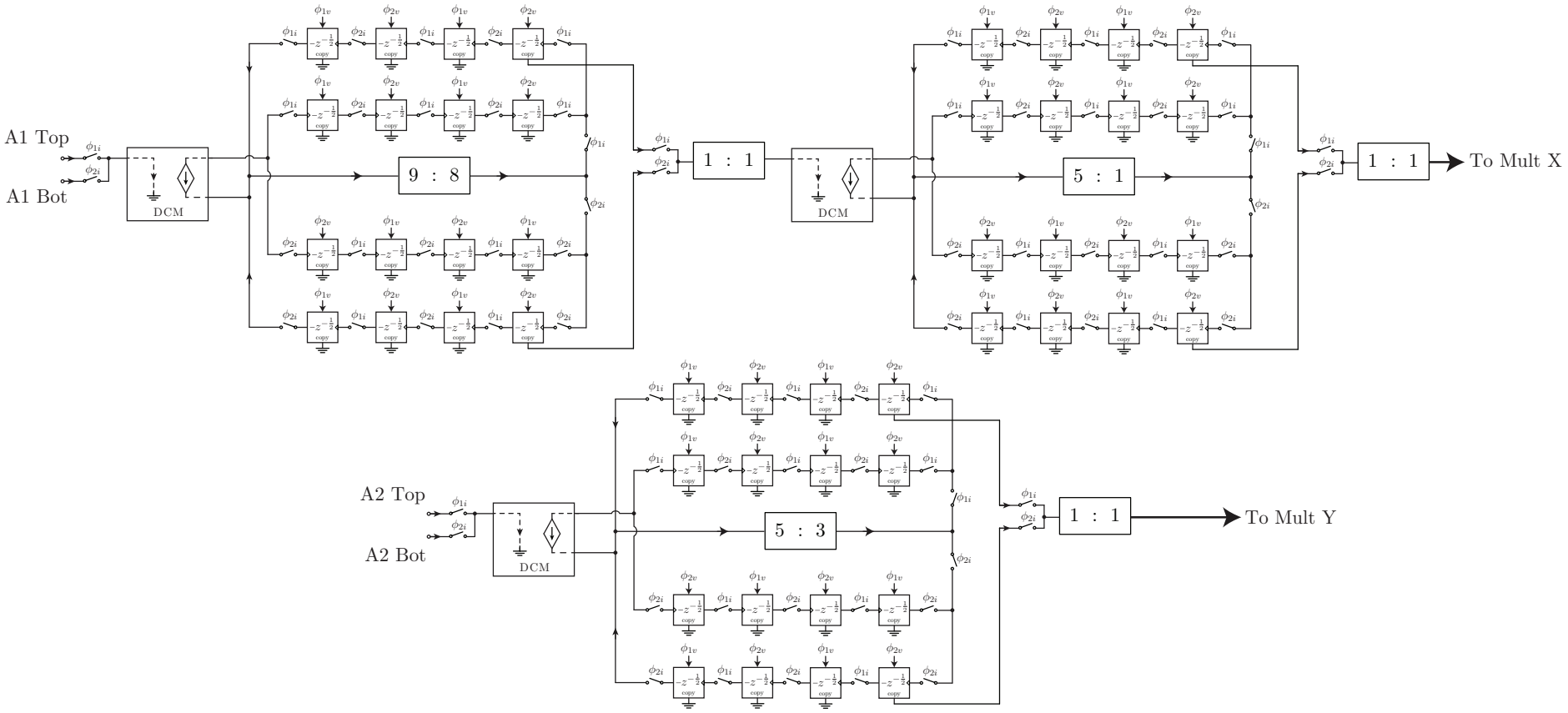


Figure 7.4: Reactive power measurement system filter diagram.

The calculation part is implemented using the diagram of Fig. 7.5. Both input paths are already directed by the filter part, and the memory cells are used to correct the half-unit delay added by the interface part to allow processing in both phases. We took advantage of the signal inversion generated by the current memory cell to implement the subtraction of each signal.

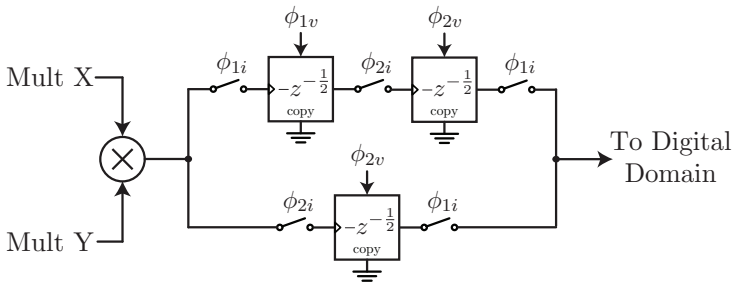


Figure 7.5: Block diagram of the calculation part of the reactive power measurement system.

To evaluate the RPMS, several simulation were performed and they are presented in the next sections.

7.2 Frequency Response

Evaluate frequency domain response of a discrete-time analog system is a challenging task, since the standard AC sweep cannot be used. Thus, it requires specific software to perform such task like the ASIZ [31]. The Cadence (R) suite has a powerful tool to allow frequency domain evaluation of discrete-time systems, which are the periodic steady state analysis (PSS) and periodic the AC analysis (PAC), that allow us to evaluate magnitude and phase components of discrete-time filters. These analysis were used to evaluate the filter part of our reactive power measurement system, and the phase results are shown in Fig. 7.6.

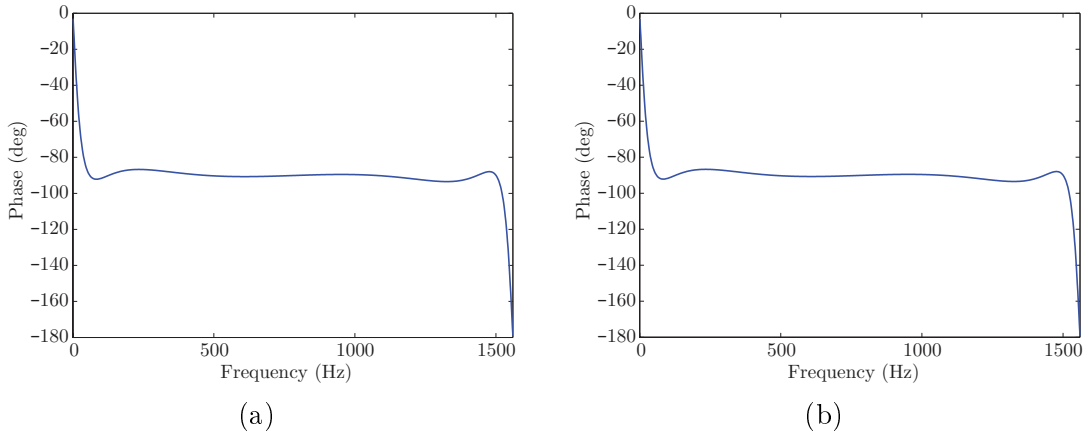


Figure 7.6: Phase plot of the frequency response of the (a) top and (b) bottom path.

One can see that the phase response of both top and bottom path have the expected behavior, with a small ripple around -90 degrees. More important than comparing with the ideal result expected on Chapter 4.3.2, it is fundamental to observe how different both paths are from each other. The phase difference between top and bottom path is presented in Fig. 7.7. One can see a phase difference is in the order of micro-degrees, which guarantees a good behavior of the two-transformers system presented in Chapter 3.

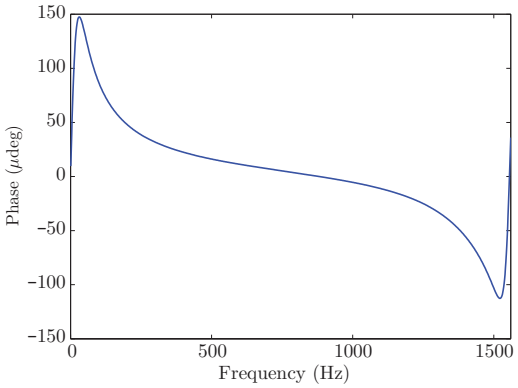


Figure 7.7: Phase difference between top and bottom path.

7.3 Transient Analysis

To evaluate the complete system, due to its non-linear behavior, a series of transient simulations are used. To observe system's precision, simulations were performed with different combinations of input levels and phase difference between both inputs. First, the whole transient results are presented and the process to obtain the reactive power final value is explained. Then, this process will be repeated for the other input values.

For the first analysis, a sinusoidal input was used for simplicity. The input frequency of both signals was fixed at 500 Hz to allow faster evaluation of the system, since transient simulations demand high computational power. Both signal levels were set at $5\mu A$ and the phase difference between voltage and current signal was set at 30°.

With those inputs, a transient simulation was performed and the results are presented. First, both signals pass through the sample and hold, leading to Fig. 7.8. The continuous time sinusoidal signal becomes a discrete-time signal. Notice that the current signal is lagging the voltage signal.

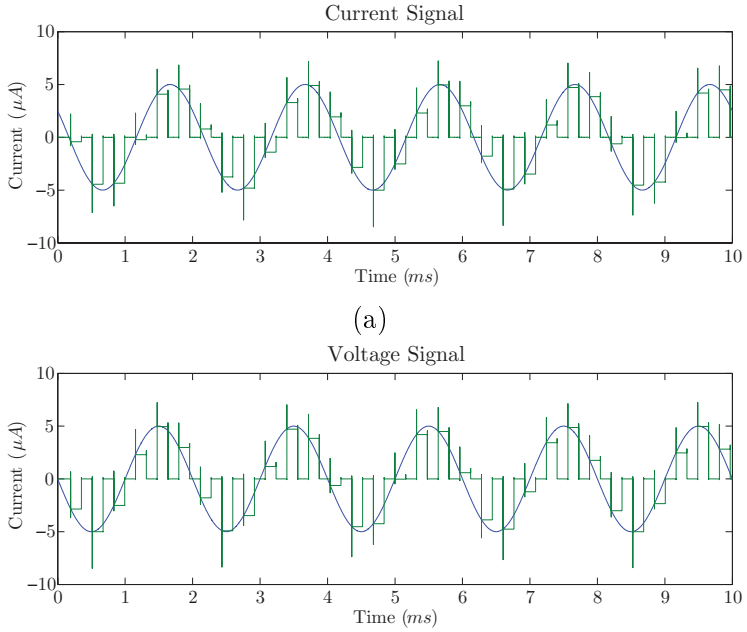


Figure 7.8: Continuous-time and sampled representation of the (a) current input signal and (b) voltage input signal.

The discrete-time signal is distributed to each proper path. After the Hilbert transformer filter, each signal has an in-phase component and a quadrature-phase component. After the filter, the calculation is performed leading to the final result presented in Fig. 7.9a. A sample can be taken at the middle of each output pulse, to better observe the signal behavior, resulting on Fig. 7.9b.

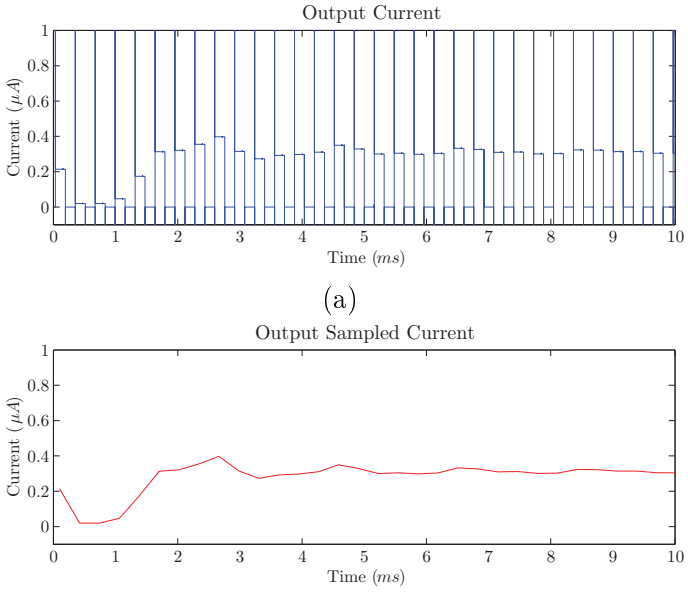
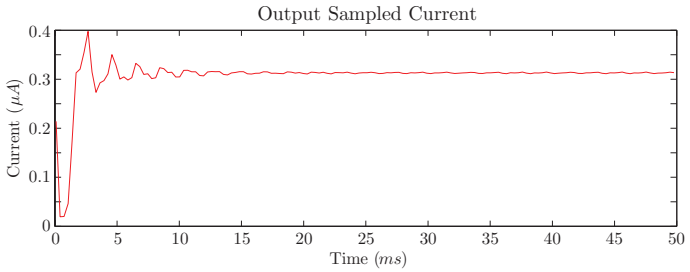
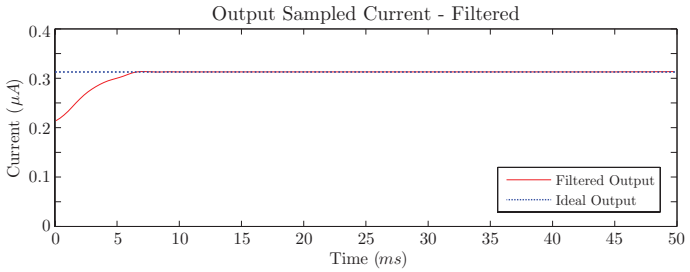


Figure 7.9: Reactive power measurement system output result. (a) Output current proportional to reactive power and (b) sampled representation.

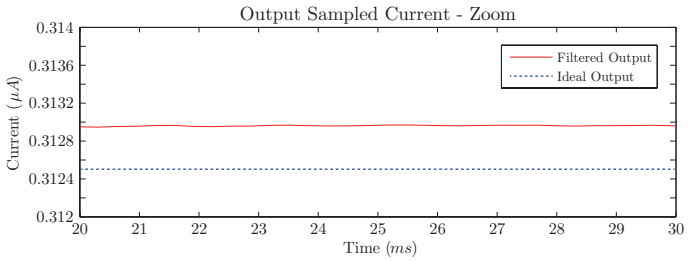
For better results, the system was simulated for a longer period of time, 50 ms. The resulting output sampled current is presented in Fig. 7.10a. It can be seen that it has a step behavior, with a constant DC term and a ripple term. This happens since the product of two sinusoidal signals generates a low-frequency term (DC) and a high-frequency term. To obtain the DC term, a digital filtering was performed with MATLAB, using a simple moving average filter. The filtered output is compared with the ideal result on Fig. 7.10b. One can see that the filtered result is very close to the ideal result. A zoom of Fig. 7.10b is presented in Fig. 7.10c. Even though results are close, there is an error in the measurement, which will be analyzed in the next section.



(a)



(b)



(c)

Figure 7.10: (a) Sampled representation, (b) sample representation filtered and (c) sample representation filtered zoomed.

7.3.1 Constant Phase Difference, Variable RMS Current

Recalling from Chapter 3, the reactive power was defined by

$$Q = \sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k) \tag{7.1}$$

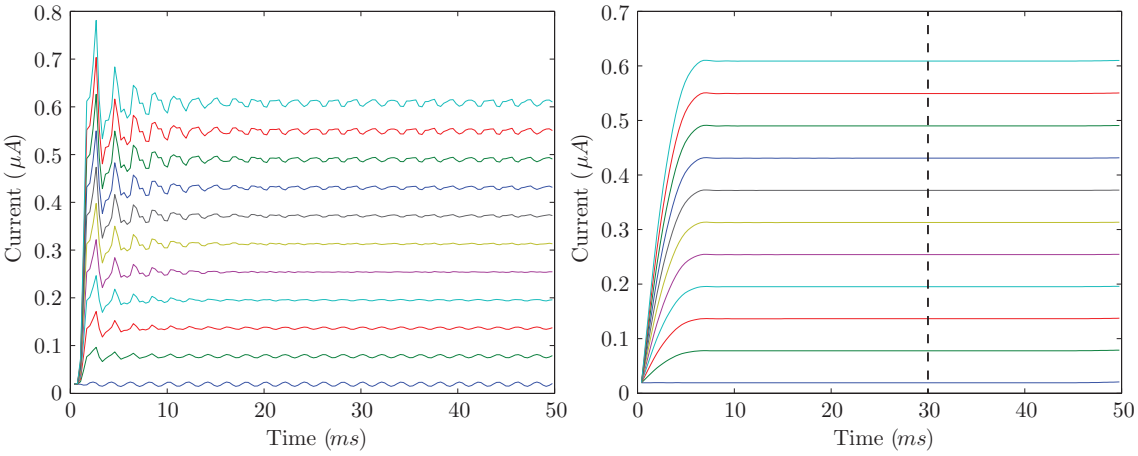
where V_k and I_k are the RMS values of the kth voltage and current harmonic component, and φ_k is the phase difference between each of them. However, since the multiplier introduce a factor of $1/4I_M$ in the multiplication, where I_M is the biasing current of the squarer, and also the $1/2$ gain factor is implemented in the digital domain, the ideal value that should be obtained by the circuit is given by

$$Q_{\text{IDEAL}} = \frac{1}{2I_M} \sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k) \tag{7.2}$$

To compare the circuit output with the ideal result, a series of simulations were executed. Both voltage signal and phase difference were kept constant and the current signal amplitude was swept. It is a reasonable assumption to consider the voltage signal at a constant level, since the voltage delivered by the electricity provider is well controlled. However, we will test the system under two different values of voltage signal, since a voltage peak might occur. This setup was executed for four combinations of voltage signal and phase difference. The nominal voltage signal considered on $5\mu A$ and the peak is considered at $10\mu A$.

Voltage Signal = 5μA and Phase difference (φ) = 30°

With the voltage signal fixed in $5\mu A$ and the phase difference fixed in 30°, a series of transient simulation were performed with different values for the current signal, sweeping from 0 to the maximum of $10\mu A$. The sampled output currents is shown in Fig. 7.11a, where the top trace corresponds to a current signal of $10\mu A$ and the bottom trace to a current signal of 0. These sampled output currents were filtered by a moving average filter, resulting in Fig. 7.11b.



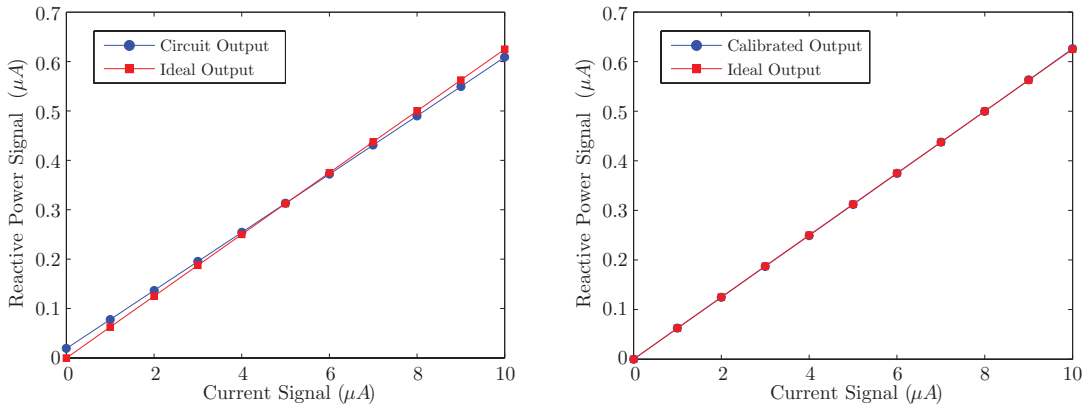
(a) (b)

Figure 7.11: Different circuit outputs for a $I_{volt} = 5\mu A$ and $\varphi = 30°$. (a) Sampled output and (b) Filtered output with the points under the dashed line (30ms) selected for next plots.

Some oscillatory transient can be observed prior the filtering. This happens since the multiplication of two sinusoidals generate a low-frequency (DC) and a high-frequency component. The usage of two Hilbert transformers mitigate the high-frequency component under sinusoidal conditions, however some residue is observed due to the cross-product between sinusoidal and offsets. This effect is more detailed in Appendix C.

One point of each filtered output was taken at the 30ms dashed line. Since the system was relaxed, the choice of 30ms was done to allow enough time for the transient to settle. Only one point was picked, so there are no averaging on the next results. These points can be plot with respect to the current signal level, leading to Fig. 7.12a. One can see that the circuit output has a different slope than the ideal output, due to gain error and offset.

Comparing both curves, we can obtain a gain error of $\alpha = -0.058492$ and an offset of $\beta = 19.228nA$. The calibration is performed in MATLAB by subtracting the offset and dividing the output by $(1 + \alpha)$, leading to Fig. 7.12b. For the next simulations, the calibration will be performed using the same factors ($\alpha = -0.058492$ and $\beta = 19.228nA$), since real systems cannot calibrate every time a new input is introduced at the system.



(a) (b)

Figure 7.12: Reactive power signal vs. current signal level for $I_{volt} = 5\mu A$ and $\varphi = 30°$ (a) before and (b) after calibration.

With the calibrated output, the remaining errors are considered non-linearities. The non-linearities are obtained by

$$\text{Non-linearities} = \frac{Q_{\text{CALIBRATED}} - Q_{\text{IDEAL}}}{Q_{\text{IDEAL}}} \tag{7.3}$$

For the configuration of Fig. 7.12, the resulting non-linearity errors are presented in Fig. 7.13. One can see that the relative error is under 0.5%, which is much less than the 2% required for a class 2 meter by the IEC.

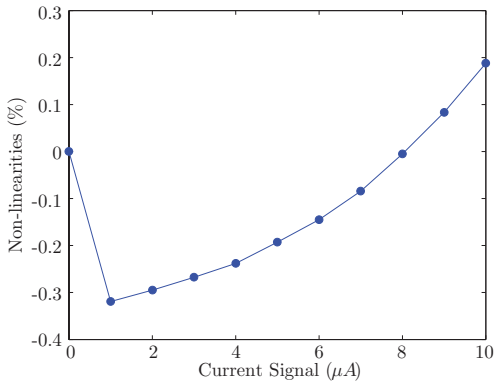
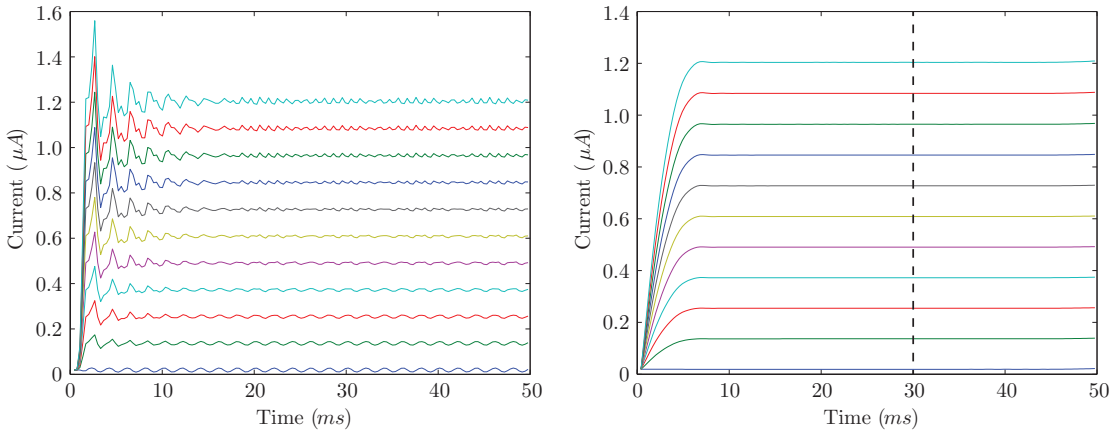


Figure 7.13: Non-linearity errors after calibration vs. current signal level for $I_{volt} = 5\mu A$ and $\varphi = 30°$.

Voltage Signal = 10μA and Phase difference (φ) = 30°

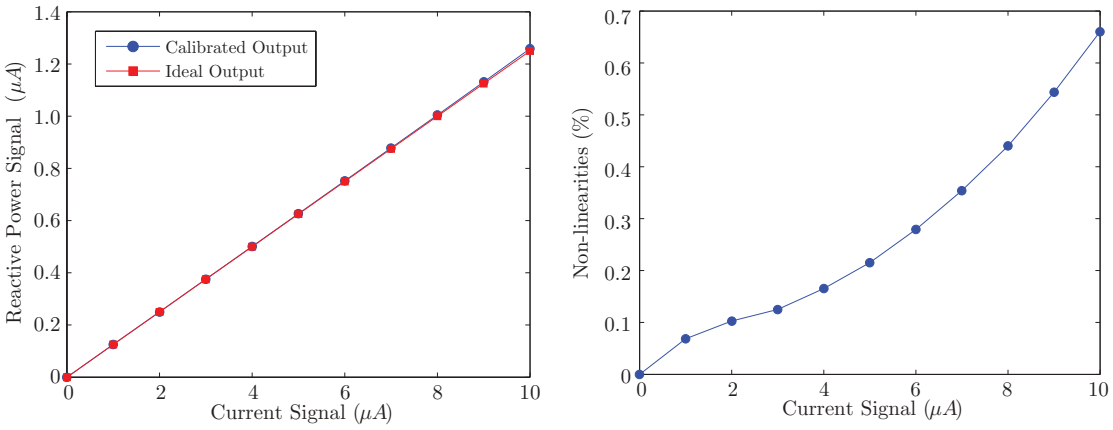
With the voltage signal fixed in $10\mu A$ and the phase difference fixed in 30°, a series of transient simulation were performed with different values for the current signal, sweeping from 0 to the maximum of $10\mu A$. The sampled output currents is shown in Fig. 7.14a, where the top trace corresponds to a current signal of 0 and the bottom trace to a current signal of $10\mu A$. These sampled output currents were filtered by a moving average filter, resulting in Fig. 7.14b.



(a) (b)

Figure 7.14: Different circuit outputs for a $I_{volt} = 10\mu A$ and $\varphi = 30°$. (a) Sampled output and (b) Filtered output with the points under the dashed line (30ms) selected for next plots.

As done before, one point of each filtered output was taken at the dashed line, at 30 ms, and calibrated using the same factors from the previous setup ($\alpha = -0.058492$ and $\beta = 19.228nA$), leading to Fig. 7.15a. The resulting non-linearity errors are presented in Fig. 7.15b. One can see that the relative error is slightly higher than the previous one. This is expected since the non-linearities of the current memory cell is higher at the maximum current of $10\mu A$. However, it keeps under the 2% required for a class 2 meter by the IEC.



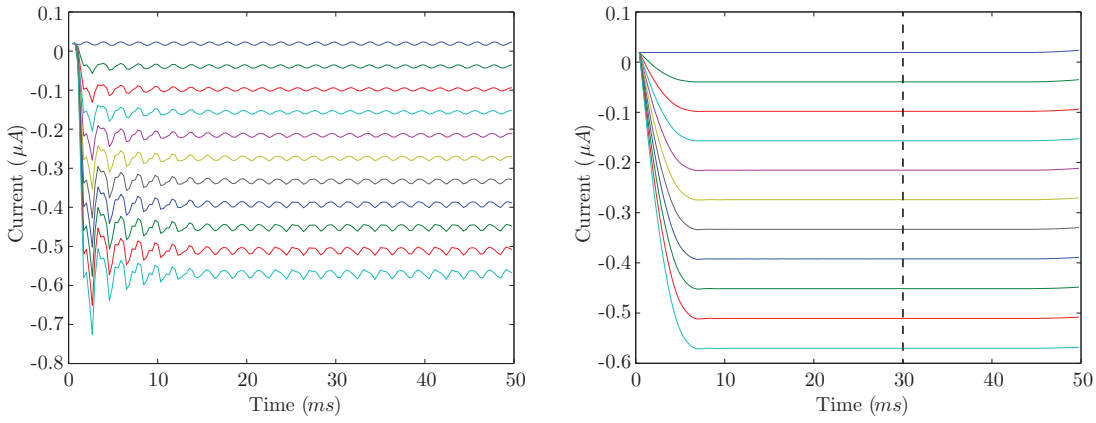
(a) (b)

Figure 7.15: (a) Reactive power signal vs. current signal level after calibration and (b) Non-linearity errors for $I_{volt} = 10\mu A$ and $\varphi = 30°$.

Voltage Signal = 5μA and Phase difference (φ) = $-30°$

With the voltage signal fixed in $5\mu A$ and the phase difference fixed in $-30°$, a series of transient simulation were performed with different values for the current signal, sweeping from 0 to the maximum of $10\mu A$. With a negative phase difference, the reactive power becomes a negative quantity.

The sampled output currents is shown in Fig. 7.16a, where the top trace corresponds to a current signal of 0 and the bottom trace to a current signal of $10\mu A$. These sampled output currents were filtered by a moving average filter, resulting in Fig. 7.16b.

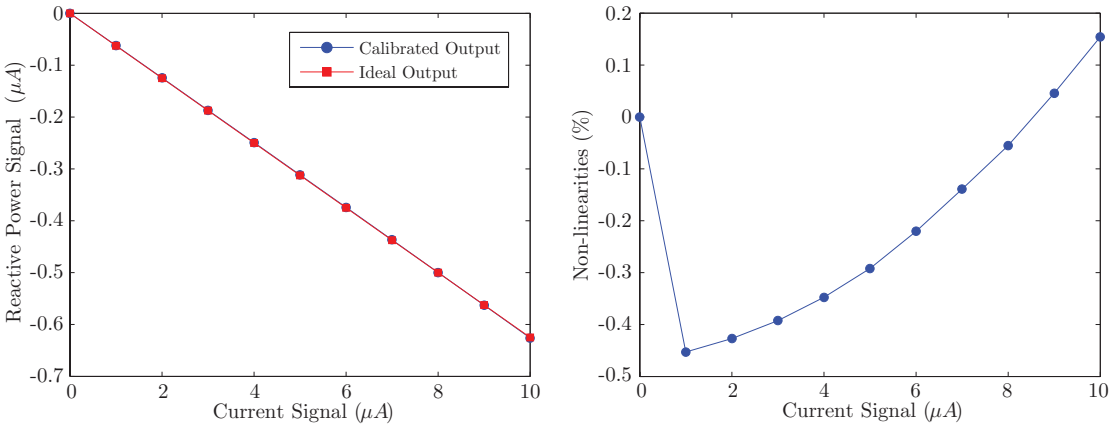


(a) (b)

Figure 7.16: Different circuit outputs for a $I_{volt} = 5\mu A$ and $\varphi = -30°$. (a) Sampled output and (b) Filtered output with the points under the dashed line (30ms) selected for next plots.

As done before, one point of each filtered output was taken at the dashed line, at 30 ms, and calibrated using the same factors from the previous setup ($\alpha = -0.058492$

and $\beta = 19.228nA$), leading to Fig. 7.17a. The resulting non-linearity errors are presented in Fig. 7.17b. Again, the errors obtained were under 0.5%, however slightly higher than with the positive angle, which is expected since the calibration was obtained for the positive angle. However, it keeps under the 2% required for a class 2 meter by the IEC.



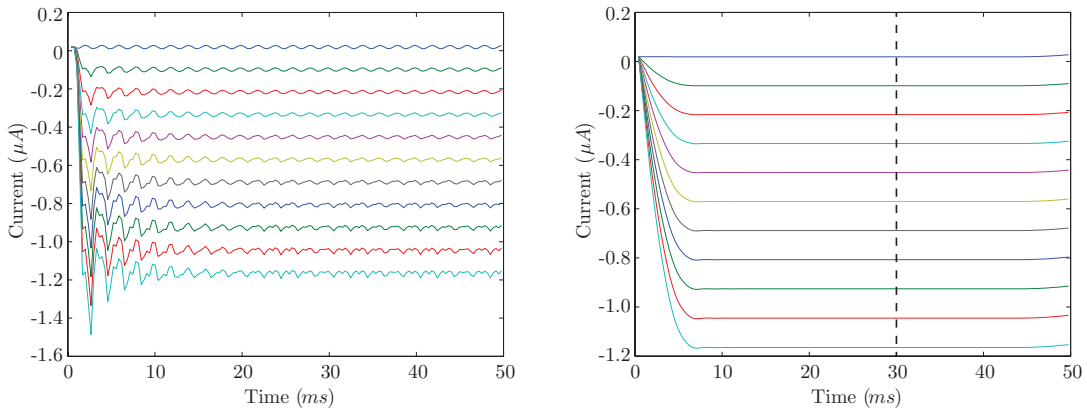
(a) (b)

Figure 7.17: (a) Reactive power signal vs. current signal level after calibration and (b) Non-linearity errors for $I_{volt} = 5\mu A$ and $\varphi = -30°$.

Voltage Signal = 10μA and Phase difference (φ) = $-30°$

With the voltage signal fixed in $10\mu A$ and the phase difference fixed in $-30°$, a series of transient simulation were performed with different values for the current signal, sweeping from 0 to the maximum of $10\mu A$.

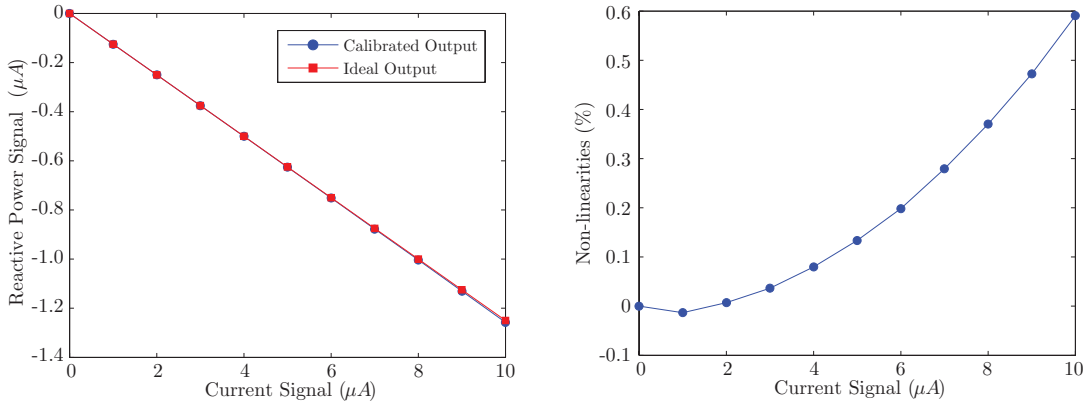
The sampled output currents is shown in Fig. 7.18a, where the top trace corresponds to a current signal of 0 and the bottom trace to a current signal of $10\mu A$. These sampled output currents were filtered by a moving average filter, resulting in Fig. 7.18b.



(a) (b)

Figure 7.18: Different circuit outputs for a $I_{volt} = 10\mu A$ and $\varphi = -30°$. (a) Sampled output and (b) Filtered output with the points at 30ms selected for next plots.

As done before, one point of each filtered output was taken at the dashed line, at 30 ms, and calibrated using the same factors from the previous setup ($\alpha = -0.058492$ and $\beta = 19.228nA$), leading to Fig. 7.19a. The resulting non-linearity errors are presented in Fig. 7.19b. As expected, the errors obtained were higher since the maximum input is used for one of the signals. Still, it keeps under the 2% required for a class 2 meter by the IEC.

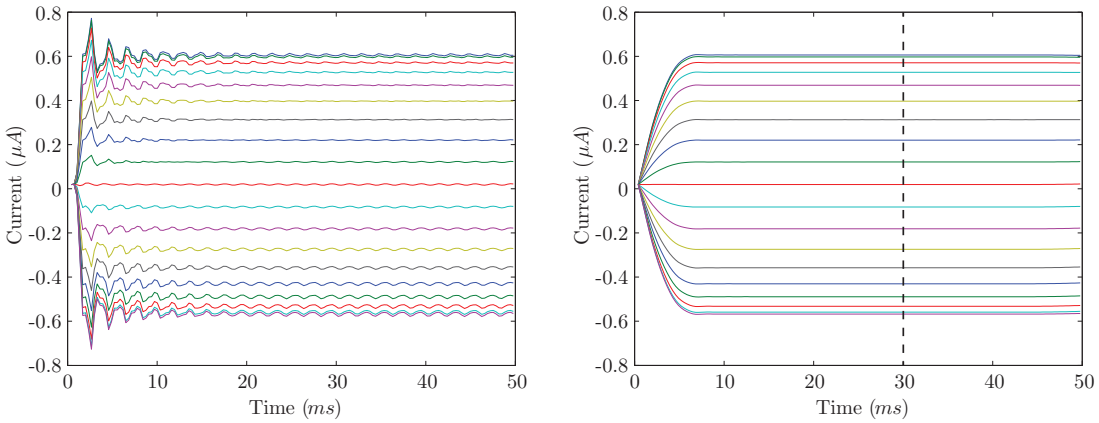


(a) (b)

Figure 7.19: (a) Reactive power signal vs. current signal level after calibration and (b) Non-linearity errors for $I_{volt} = 10\mu A$ and $\varphi = -30°$.

7.3.2 Variable Phase Difference, Constant Signal Level

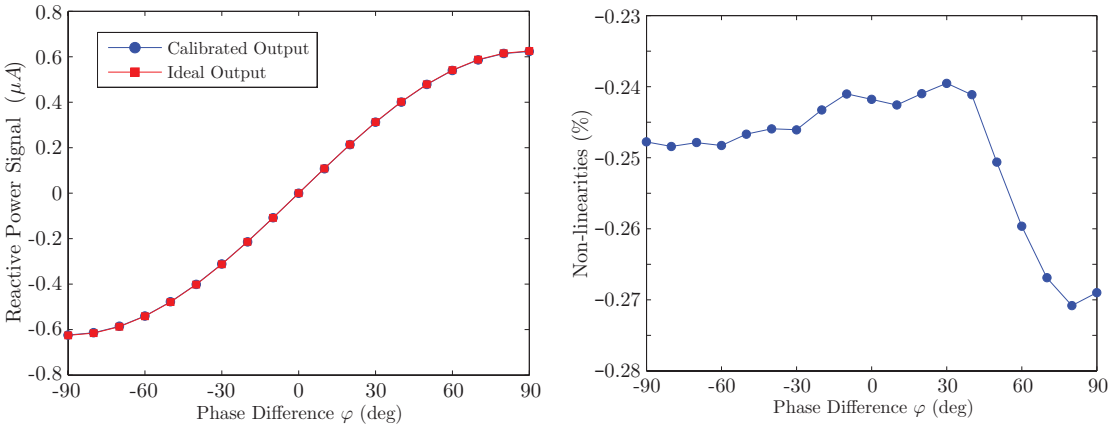
For this simulation, both voltage and current signal were fixed in $5\mu A$ and the phase different was swept from $-90°$ to $90°$. The sampled output currents is shown in Fig. 7.20a, where the top trace corresponds to a $90°$ phase difference and the bottom trace to a $-90°$ phase difference. These sampled output currents were filtered by a moving average filter, resulting in Fig. 7.20b.



(a) (b)

Figure 7.20: Different circuit outputs for a $I_{volt} = 5\mu A$, $I_{cur} = 5\mu A$ and a variety of phase differences. (a) Sampled output and (b) Filtered output with the points under the dashed line (30ms) selected for next plots.

As done previously, one point of each filtered output was taken at the dashed line, at 30 ms, and calibrated using the same factors from the previous setup ($\alpha = -0.058492$ and $\beta = 19.228nA$), leading to Fig. 7.21a. The resulting non-linearity errors are presented in Fig. 7.21b. One can see that the relative error is under 0.3%. It meets the 2% specification of the IEC Class 2 meter and the 1% specified in the project design.



(a) (b)

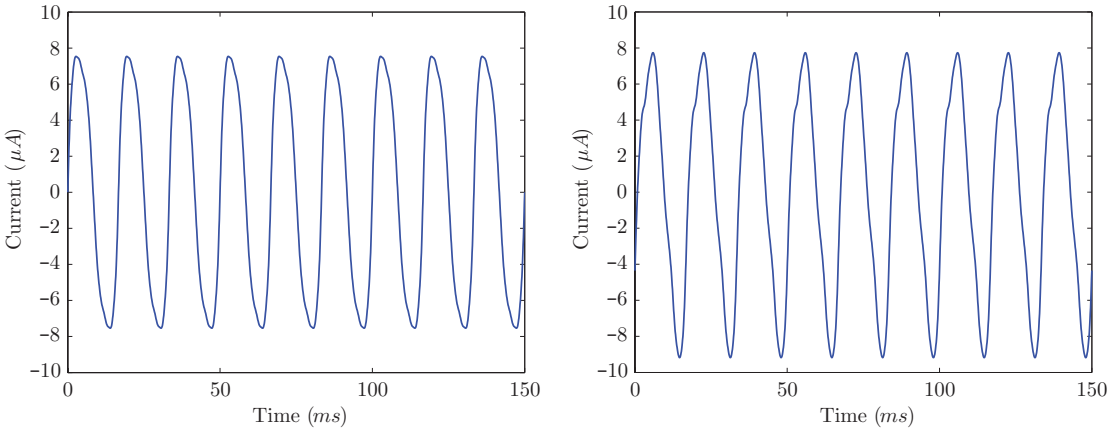
Figure 7.21: (a) Reactive power signal vs. phase difference φ after calibration and (b) Non-linearity errors for $I_{volt} = 5\mu A$ and $I_{cur} = 5\mu A$.

7.4 Non-sinusoidal Input (Wideband Signal)

One of the big advantages of our system is the measurement under non-sinusoidal conditions. For further evaluation, a non-sinusoidal test input was introduced at the system. The test input characteristics are given in Table 7.1. The test input plot is presented in Fig. 7.22. As it can see, both inputs are heavily distorted sinusoidal signals.

Table 7.1: Wideband input signals characteristics.

Frequency (Hz)	**Voltage Signal** (μA)	**Current Signal** (μA)	**Phase Difference** φ **(deg)**	**Reactive Power Harmonic** (μA)
60	8	8	30	0.800000
120	1	1	15	$6.4704 \cdot 10^{-3}$
180	1	1	-10	$-4.3412 \cdot 10^{-3}$
240	0.2	0.2	40	$6.4278 \cdot 10^{-4}$
300	0.15	0.15	60	$4.8714 \cdot 10^{-4}$
360	0.1	0.1	10	$4.3412 \cdot 10^{-5}$
420	0.05	0.05	-85	$-6.2262 \cdot 10^{-5}$
480	0.05	0.05	-15	$-1.6176 \cdot 10^{-5}$
540	0.05	0.05	20	$2.1376 \cdot 10^{-5}$
600	0.05	0.05	45	$4.4194 \cdot 10^{-5}$



(a) (b)

Figure 7.22: (a) Voltage and (b) current non-sinusoidal input signals.

The total reactive power to be measured at the output is the sum of each reactive power harmonic, leading to

$$Q_{\text{IDEAL}} = 0.803289742703454 \tag{7.4}$$

Since the main component is at 60 Hz, the transient simulation was performed for a longer period of 400 ms. The sampled output current for the wideband inputs is presented in Fig. 7.23. The ripple is much higher than the previous simulations, since more components are introduced on its composition.

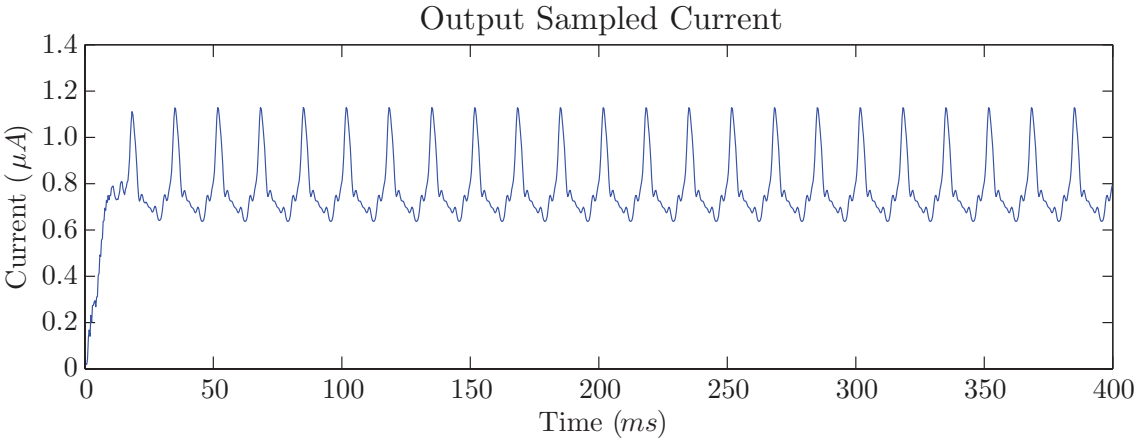


Figure 7.23: Sampled output current for non-sinusoidal inputs.

The sampled output current is filtered and compared with the ideal reactive power value of (7.4) in Fig. 7.24. It can be noticed that the filtered output is slightly different than the ideal result. However, this figure is prior to the calibration setup.

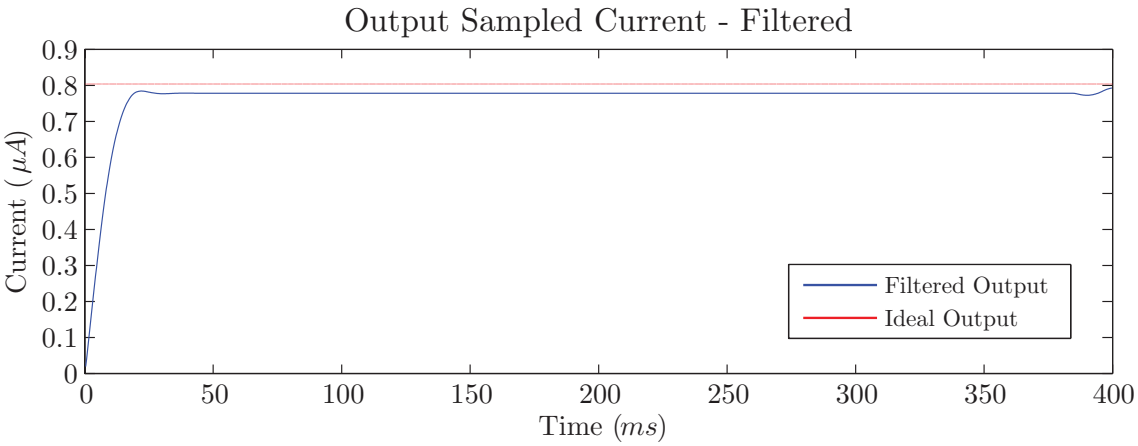


Figure 7.24: Filtered output current for non-sinusoidal inputs.

The calibration was performed using the same factors from the previous setup ($\alpha = -0.058492$ and $\beta = 19.228nA$), resulting in Fig. 7.25. To compare the ideal with the calibrated output, a point at 200ms was selected, after the relaxed system has settled. The calibrated result was $Q_{\text{CALIBRATED}} = 0.80612465$. The relative error obtained, given by (7.3), was $NL = 0.35291\%$, which is much lower the 2% specification for the Class 2 meter standard of the IEC.

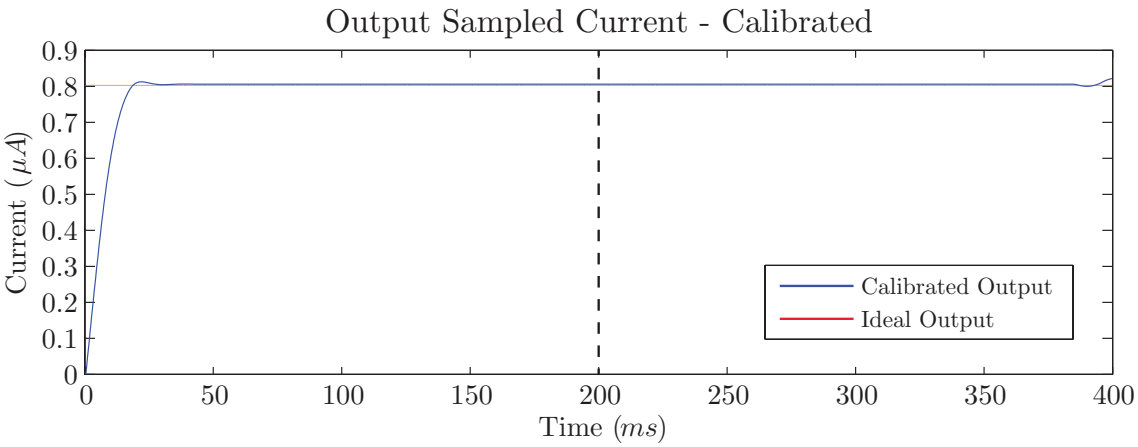
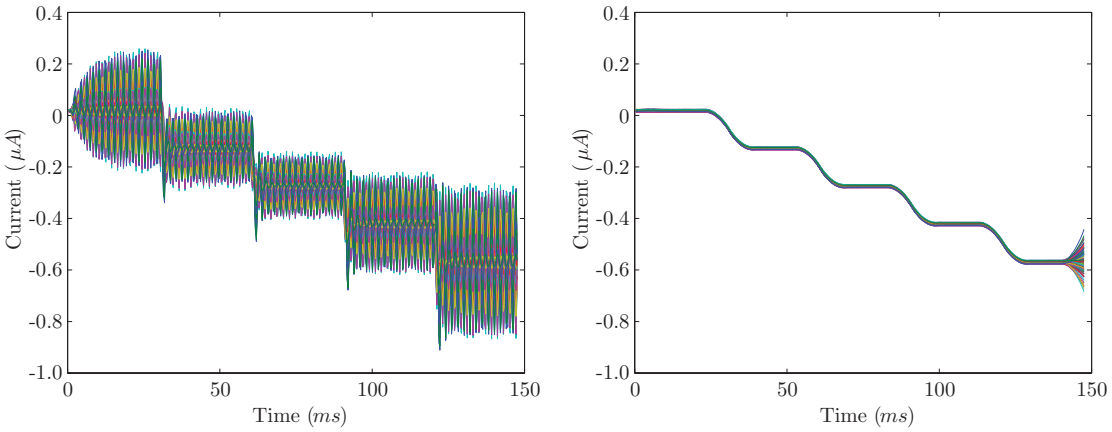


Figure 7.25: Calibrated output current for non-sinusoidal inputs.

7.5 Monte Carlo simulation

To evaluate the circuit behavior with transistor mismatch and process parameters variations, a Monte Carlo simulation was performed with 100 samples was executed. To perform this analysis, the voltage signal was fixed in $5\mu A$ and the phase difference was fixed in $-30°$, while the current signal varied progressively over time, from 0 to $10\mu A$, by steps of $2.5\mu A$. This resulted in five different points of measurements for each Monte Carlo sample.

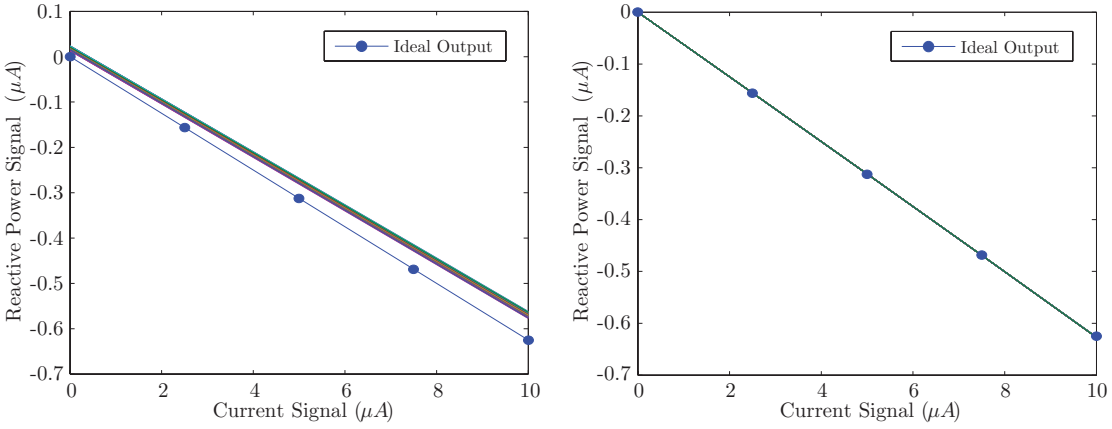
The sampled output current for the Monte Carlo simulation is presented in Fig. 7.26a. It is possible to see a staircase with five steps together with a high ripple. As done before, the sampled output current is filtered by a moving average filter, resulting in Fig. 7.26b. With the attenuation of the ripple, the staircase waveform is easily observed.



(a) (b)

Figure 7.26: Monte Carlo simulation results for a transient simulation with variable current signal level, $I_{volt} = 5\mu A$ and $\varphi = -30°$. (a) Sampled output and (b) Filtered output.

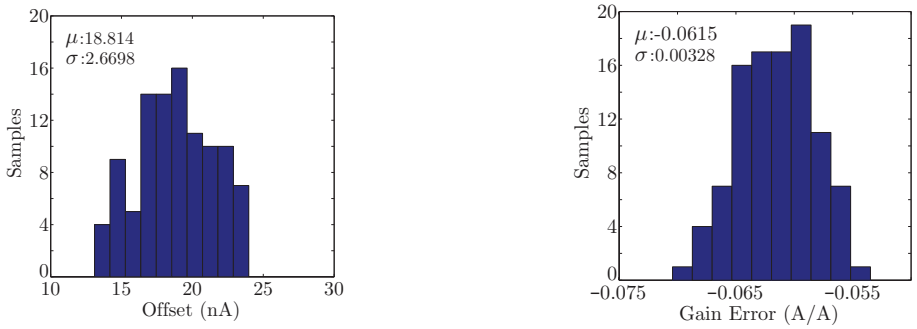
A point at the middle of each step was taken for each Monte Carlo sample and plotted with respect to the current signal level, as presented in Fig. 7.27a. The ideal output is also compared with the real values of each Monte Carlo sample. As done previously, the result for each Monte Carlo sample should be calibrate to compensate gain error and offset. Each sample is assumed to be on a different energy meter, thus a calibration is performed for each individual sample and not universally. The calibration results are presented in Fig. 7.27b.



(a) (b)

Figure 7.27: Reactive power signal vs. current signal level for each Monte Carlo sample (a) before and (b) after calibration.

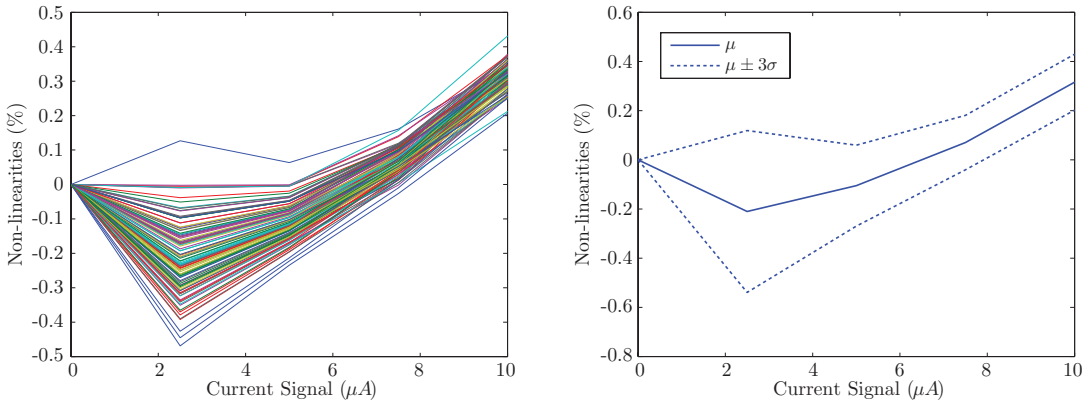
Both gain error and offset obtained for each Monte Carlo sample are distributed on a histogram and presented in Fig. 7.28.



(a) (b)

Figure 7.28: Histograms for (a) offset and (b) gain error of the reactive power measurement system.

After calibrating each Monte Carlo sample the non-linearities can be obtained using (7.3). The results are shown in Fig. 7.29a. One can see that the non-linearity errors are under 1% for every Monte Carlo sample, which shows that the proposed measurement system is very robust against mismatch and parameter variation. The mean and standard deviation for the non-linearity curves are also obtained and displayed in Fig. 7.29b. For a 3σ variation, the non-linearity errros are also under 1%, validating the proposed structure and design implemented in this work.



(a) (b)

Figure 7.29: (a) Non-linearity errors after calibration vs. current signal level for Monte Carlo simulation and (b) statistical distribution of the non-linearity errors.

A summary with the reactive power measurement system parameters can be observed in Table 7.2.

Table 7.2: Reactive Power Measurement System parameters.

Parameter	**Value**
Power Supply (V)	3.3
Static Power Consumption (mW)	≈ 13
Input Signal Limits (μA)	± 10
Nominal Gain ($1/\mu A$)	0.025
Offset Error (nA) ($\mu \pm 3\sigma$)	18.814 ± 8.01
Gain Error (%) ($\mu \pm 3\sigma$)	-6.15 ± 0.984
Measurement Error Max. @ $I_{volt} = 5\mu A$	0.45%
Measurement Error Max. @ $I_{volt} = 10\mu A$	0.7%
Measurement Bandwidth (Hz)	60 - 1500
Number of Harmonics	25

Chapter 8

Conclusion and Future Work

This dissertation presented a novel reactive power measurement system which uses the switched-current Hilbert transformer introduced in Chapter 2. The implemented Hilbert transformer achieved very low-sensitivity to transistor mismatch due to the use of structurally all-pass section.

A pair of switched-current Hilbert transformers was utilized to implement the novel method. Since they were implemented using structurally all-pass sections, the coefficient of each section of both transformers could be implemented by the same block, and each transformer shares this block. This way, perfect matching between both Hilbert transformers is achieved even in analog domain and under transistor mismatch.

The circuit design of the proposed method was detailed, starting by the system specification to meet international regulatory agencies standards. To achieve those standards, a novel current memory cell was developed to achieve 13 bits with a power consumption of 165 μW, a low consumption for switched-current standards.

The proposed system was validated using circuit simulation, where the obtained non-linearity errors were under 0.5% for normal voltage signal levels ($I_{volt} = 5\mu A$) and under 1% for voltage peaks ($I_{volt} = 10\mu A$). The system was also simulated under non-sinusoidal inputs, where it performed with similar precision to the sinusoidal input. Monte Carlo simulation was perform to observe non-linearity errors under mismatch, and the obtained results showed errors under 1% for a 3σ deviation.

To achieve the high-precision result, an offset and gain error correction must be executed. However, most commercial analog-to-digital converters have the option for such correction.

Comparing our work with the implemented in [7], which achieved a 0.2% measurement error on a system implemented with high-performance A/D converter and DSP, our work presents a higher measurement error, which is expected since analog circuits are subject to manufacturing imperfections and non-ideal effects. However, since our implementation does the signal processing on analog domain, it does not

require a high-performance A/D converter neither a high-performance DSP, reducing manufacturing costs.

The main advantages of the proposed method relies in the analog approach, which can represent a low-cost and low-complexity option when compared with commercial DSPs and FPGAs with expensive price and hardware demanding algorithm. The main drawback is the inability to achieve the high-precision required for Class 0.5 or Class 0.2 meters, therefore it cannot be used for any power meter. Therefore, the proposed system is a good choice to implement low-cost Class 1 and Class 2 meters.

8.1 Future Work

In this dissertation, a more theoretical approach towards reactive power measurement system using switched-current was presented. Since the proposed circuitry was validated through simulation, the next natural step is the physical design of an integrated circuit to obtain actual measurement results.

The calibration routine should be better studied to observe the optimal way to perform it. Not only on digital domain, but the calibration in analog domain to compensate mismatch should also be considered [64, 65].

The implementation of a sigma-delta modulator employing the proposed memory cell seems promising for this application.

Some improvements in the circuit can be also made. For instance, the differential current mirror can be substituted by using sub-phases, since the system operates in a low-frequency. The gain error introduced by it can therefore be eliminated. However, the addition of sub-phases may introduce glitches in the operation, so it must be implemented carefully.

A future research possibility is to observe if the coefficient sharing technique can be implemented with switched capacitors. It represent a possibility of a system with low-power consumption while achieving systematic high-precision. Another possibility is the use of weak-inversion current memory cells for the same reason.

Bibliography

[1] LANTERO, A. "The War of the Currents: AC vs. DC Power". Disponível em: <http://energy.gov/articles/war-currents-ac-vs-dc-power>.

[2] DAVIES, M., DOMMASCHK, M., DORN, J., et al. "HVDC PLUS – Basics and Principle of Operation", *Siemens Ag*, pp. 1–24, 2011.

[3] AGÊNCIA NACIONAL DE ENERGIA ELÉTRICA, A. "Procedimentos de Distribuição de Energia Elétrica no Sistema Elétrico Nacional – PRODIST Módulo 8 – Qualidade da Energia Elétrica", 2015.

[4] MOULIN, E. "Measuring reactive power in energy meters". 2002. Disponível em: <http://communications.analog.com/static/imported-files/tech_articles/16242282714726reactive_energy_metering_international_edition.pdf>.

[5] BORGHESE, F. "Automated Meter Management roll-out Enel's experience". 2010. Disponível em: <http://www.fstrf.ru/eng/international_activity/meropr/4/4/1/04_-_Automated_Meter_Management_roll-out_borghese_fabio.pdf>.

[6] GALLO, D., LANDI, C., PASQUINO, N., et al. "A new methodological approach to quality assurance of energy meters under non-sinusoidal conditions", *Conference Record - IEEE Instrumentation and Measurement Technology Conference*, pp. 1626–1631, 2006. ISSN: 10915281. doi: 10.1109/IMTC.2006.237118.

[7] HAO, P., ZANJI, W., JIANYE, C. "A measuring method of the single-phase AC frequency, phase, and reactive power based on the Hilbert filtering", *IEEE Transactions on Instrumentation and Measurement*, v. 56, n. 3, pp. 918–923, 2007. ISSN: 00189456. doi: 10.1109/TIM.2007.894885.

[8] XIAO, Y., YUAN, H., CHEN, Z. "FPGA Realization of Reactive Power Measurement System Based on Phase-shift", *2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, v. 0, n. 1, pp. 2029–2033, 2011.

[9] ANĐELKOVIĆ, B., DAMNJANOVIĆ, M. "Design of hilbert transformer for solid-state energy meter", *Proc. XLVIII ETRAN Conference*, v. I, pp. 83–86, 2004.

[10] OZDEMIR, A., FERIKOGLU, A. "Low cost mixed-signal microcontroller based power measurement technique", *IEE Proceedings - Science, Measurement and Technology*, v. 151, n. 4, pp. 253–258, 2004. ISSN: 13502344. doi: 10.1049/ip-smt:20040242. Disponível em: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=1315466&queryText=Low+cost+mixed-signal+microcontroller+based+power+measurement+technique+A.>.

[11] YUAN, H., BI, M., CHEN, Z. "FPGA Realization of Reactive Power Measurement System Based on FFT", *2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pp. 2018–2022, 2012.

[12] YOON, W.-K., DEVANEY, M. J. "Reactive power measurement using the wavelet transform", *IEEE Transactions On Instrumentation And Measurement*, v. 49, n. 2, pp. 246–252, 2000. ISSN: 00189456. doi: 10.1109/19.843057. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=843057>.

[13] ABIYEV, A. N., DIMILILER, K. "Reactive power measurement in sinusoidal and nonsinusoidal conditions by use of the walsh functions", *Conference Record - IEEE Instrumentation and Measurement Technology Conference*, pp. 89–94, 2008. ISSN: 10915281. doi: 10.1109/IMTC.2008.4547010.

[14] MA, S., ZHAO, R., XU, Q. "ANF-based single-phase reactive power measurement in the presence of harmonics", *DRPT 2011 - 2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies*, pp. 1580–1585, 2011. doi: 10.1109/DRPT.2011.5994149.

[15] ANSARI, R. "IIR discrete-time Hilbert transformers", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, v. 35, n. 8, pp. 1116–1119, 1987. ISSN: 0096-3518. doi: 10.1109/TASSP.1987.1165250.

[16] DAUBERT, S. J., VALLANCOURT, D., TSIVIDIS, Y. P. "Current copier cells", *Electronics Letters*, v. 24, n. 25, pp. 1560–1562, 1988.

[17] HUGHES, J. B., BIRD, N. C., MACBETH, I. C. "Switched Currents - a New Technique for Analog Sampled-Data Signal-Processing", *1989 Ieee International Symposium on Circuits and Systems, Vols 1-3*, pp. 1584–1587, 1989. ISSN: 02714310.

[18] TSE, C., CHOW, M. "A new clock-feedthrough cancellation method for second-generation switched-current circuits". In: *Proceedings of ISCAS'95 - International Symposium on Circuits and Systems*, v. 3, pp. 2104–2107, 1995. ISBN: 0-7803-2570-2. doi: 10.1109/ISCAS.1995.523840. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=523840>.

[19] HUGHES, J., MOULDING, K. "S2I: a switched-current technique for high performance", *Electronics Letters*, v. 29, n. 16, pp. 1400, 1993. ISSN: 00135194. doi: 10.1049/el:19930938. Disponível em: <http://digital-library.theiet.org/content/journals/10.1049/el_19930938>.

[20] ERIKSSON, S., TAN, N. "Low-voltage fully differential class-AB SI circuits with common-mode feedforward", *Electronics Letters*, v. 30, n. 25, pp. 2090–2091, 1994. ISSN: 0013-5194. doi: 10.1049/el:19941426. Disponível em: <http://digital-library.theiet.org/content/journals/10.1049/el_19941426>.

[21] NAIRN, D. "A high-linearity sampling technique for switched-current circuits", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, v. 43, n. 1, pp. 49–52, 1996. ISSN: 10577130. doi: 10.1109/82.481474. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=481474>.

[22] ANJOS, E. V. P., BARÚQUI, F. "High-Linearity Zero-Voltage Switching Current Memory Cell for Measurement Applications". In: *VII IEEE LATIN AMERICAN SYMPOSIUM ON CIRCUITS AND SYSTEMS (LASCAS)*, pp. 311–314, 2016.

[23] ANJOS, E., BARÚQUI, F. "Low-sensitivity recursive Hilbert transformer using switched-current techniques", *Electronics Letters*, v. 51, n. 12, pp. 894–895, 2015. ISSN: 0013-5194. doi: 10.1049/el.2015.0826. Disponível em: <http://digital-library.theiet.org/content/journals/10.1049/el.2015.0826>.

[24] GOMES, J. G. R. C., PETRAGLIA, A. "An analog sampled-data DSB to SSB converter using recursive Hilbert transformer for accurate I and Q channel matching", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, v. 49, n. 3, pp. 177–187, 2002. ISSN: 10577130. doi: 10.1109/TCSII.2002.1013864.

[25] STOYANOV, G. K., NIKOLOVA, K. S. "Improved Accuracy and Low-Sensitivity Design of Digital Allpass based Hilbert Transformers", 2013.

[26] MITRA, S. K. *Digital Signal Processing: A Computer Based Approach.* 2001. ISBN: 978-0072513783.

[27] PETRAGLIA, A., BARÚQUI, F. A. P., MITRA, S. K. "Recursive switched-capacitor Hilbert transformers", *1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, v. 1, n. 2, pp. 496–499, 1998.

[28] RENFORS, M., SARAMAKI, T. "Recursive Nth-Band Digital Filters - Part I : Design and Properties", *Tcas*, v. 34, n. 1, pp. 24–39, 1987. ISSN: 0098-4094. doi: 10.1109/TCS.1987.1086034.

[29] OPPENHEIM, A. V., SCHAFER, R. W. *Discrete-Time Signal Processing.* Prentice-Hall, 2009. ISBN: 0131988425.

[30] REGALIA, P. A., MITRA, S. K., VAIDYANATHAN, P. P. "Digital All-Pass Filter: a Versatile Signal Processing Building Block." *Proceedings of the IEEE*, v. 76, n. 1, pp. 19–37, 1988. ISSN: 00189219. doi: 10.1109/5.3286.

[31] DE QUEIROZ, A. C. M., PINHEIRO, P. R. M., CALÔBA, L. P. "Nodal analysis of switched-current filters", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, v. 40, n. 1, pp. 10–18, 1993. ISSN: 10577130. doi: 10.1109/82.215356.

[32] AHMED, A.-H. "A Novel Circuit for Electronic Measurements", *Electrical Engineering*, , n. December, pp. 1049, 1955.

[33] DREW, A., GALPIN, R. "A New Approach to the Measurement of Power, Reactive Volt-Amperes, and Volt-Amperes by Electronic Analog Multiplication", *IEEE Transactions on Instrumentation and Measurement*, , n. 2 & 3, pp. 103–107, 1964.

[34] DJOKIC, B., BOSNJAKOVIC, P., BEGOVIC, M. "New method for reactive power and energy measurement", *IEEE Transactions on Instrumentation and Measurement*, v. 41, n. 2, pp. 280–285, 1992. ISSN: 0018-9456. doi: 10.1109/19.137361.

[35] PENESCU, C. "Digital Measurement of Active and Reactive Power", *IEEE Transactions on Power Apparatus and Systems*, v. 84, n. 7, 1965. ISSN: 0018-9510. doi: 10.1109/TPAS.1965.4766232.

[36] BUDEANU, C. *Puissances Reactives et Fictives*. Tese de Doutorado, Instytut Romain de l'Energie, 1927.

[37] COMMITTEE, M. *IEEE Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal , Nonsinusoidal , Balanced*, v. 40. 2000. ISBN: 0738119628. doi: 10.1109/TIA.2004.827452.

[38] CZARNECKI, L. S. "What is wrong with the Budeanu concept of reactive and distortion power and why it should be abandoned", *IEEE Transactions on Instrumentation and Measurement*, v. IM-36, n. 3, pp. 834–837, 1987. ISSN: 0018-9456. doi: 10.1109/TIM.1987.6312797.

[39] SOCIETY, E. *IEEE Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal , Non- Sinusoidal , Balanced , or Unbalanced Conditions*. N. October. 2009. ISBN: 0738119628. doi: 10.1109/IEEESTD.2010.5439063.

[40] WILLEMS, J. L. "Budeanu's reactive power and related concepts revisited", *IEEE Transactions on Instrumentation and Measurement*, v. 60, n. 4, pp. 1182–1186, 2011. ISSN: 00189456. doi: 10.1109/TIM.2010.2090704.

[41] JELTSEMA, D. "Budeanu's concept of reactive and distortion power revisited". In: *2015 International School on Nonsinusoidal Currents and Compensation (ISNCC)*, v. 90, pp. 1–6, 2015. doi: 10.1109/ISNCC.2015.7174697. Disponível em: <`http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7174697`>.

[42] HAO, P., ZANJI, W., JIANYE, C., et al. "Method of Reactive Power Measurement Based on Two Pairs of Hilbert Digital Filters", *Automation of Electric Power Systems*, v. 30, n. 18, pp. 45–48, 2006.

[43] KING, C. L. "AN994: IEC Compliant Active-Energy Meter Design Using the MCP3905/6". 2005. Disponível em: <`http://ww1.microchip.com/downloads/en/AppNotes/00994a.pdf`>.

[44] COPEL, D. D. M. A. D. D. A. "ETC 4.03 - ESPECIFICAÇÃO TÉCNICA PARA MEDIDOR ELETRÔNICO PARA MEDIÇÃO DE ENERGIA ATIVA, REATIVA E DEMANDA". 2015.

[45] SOARES, C. F. T. *Métodos para Aprimorar o Projeto e o Layout de Filtros Analógicos em Circuitos Integrados CMOS*. Tese de Doutorado, 2009.

[46] FIORELLI, R., ARNAUD, A., GALUP-MONTORO, C. "Series-parallel association of transistors for the reduction of random offset in non-unity

gain current mirrors". In: *2004 IEEE International Symposium on Circuits and Systems*, v. 1, pp. I–881–4, 2004. ISBN: 078038251X. doi: 10.1109/ISCAS.2004.1328336. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1328336>.

[47] PELGROM, M. J. M., DUINMAIJER, A. C. J., WELBERS, A. P. G. "Matching properties of MOS transistors", *IEEE Journal of Solid-State Circuits*, v. 24, n. 5, pp. 1433–1440, 1989. ISSN: 00189200. doi: 10.1109/JSSC.1989.572629.

[48] RAZAVI, B. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Higher Education, 2001. ISBN: 0-07-118839-8.

[49] GARRARD, M., RYAN, P. "AN2989: Design , Accuracy , and Calibration of Analog to Digital Converters on the MPC5500 Family". 2010. Disponível em: <http://cache.freescale.com/files/32bit/doc/app_note/AN2989.pdf>.

[50] SAWIGUN, C., SERDIJN, W. A. "Analysis and design of a low-voltage, low-power, high-precision, class-AB current-mode subthreshold CMOS sample and hold circuit", *IEEE Transactions on Circuits and Systems I: Regular Papers*, v. 58, n. 7, pp. 1615–1626, 2011. ISSN: 15498328. doi: 10.1109/TCSI.2011.2158491.

[51] TOUMAZOU, C., HUGHES, J. B., PATTULLO, D. M. "Regulated cascode switched-current memory cell", v. 26, n. 5, pp. 303–305, 1990. ISSN: 00135194. doi: 10.1049/el:19900200.

[52] JONSSON, B. *Switched-current circuits: from building blocks to mixed analog-digital systems*. Tese de Doutorado, Royal Institute of Technology, 1999. Disponível em: <http://kth.diva-portal.org/smash/record.jsf?pid=diva2:8471>.

[53] MARTINS, J., DIAS, V. "Very low-distortion fully differential switched-current memory cell", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, v. 46, n. 5, pp. 640–643, 1999. ISSN: 10577130. doi: 10.1109/82.769814. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=769814>.

[54] BALACHANDRAN, G., ALLEN, P. "Switched-current circuits in digital CMOS technology with low charge-injection errors", *IEEE Journal of Solid-State Circuits*, v. 37, n. 10, pp. 1271–1281, 2002. ISSN: 0018-9200.

doi: 10.1109/JSSC.2002.803019. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1035941>.

[55] DE QUEIROZ, A., PINHEIRO, P. "Switching sequence effects in switched-current filters". In: *1993 IEEE International Symposium on Circuits and Systems*, pp. 982–985, 1993. ISBN: 0-7803-1281-3. doi: 10.1109/ISCAS.1993.393888. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=393888>.

[56] SHAH, P., TOUMAZOU, C. "A new high speed low distortion switched-current cell", *1996 IEEE International Symposium on Circuits and Systems. Circuits and Systems Connecting the World. ISCAS 96*, v. 1, pp. 421–424, 1996. doi: 10.1109/ISCAS.1996.539974. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=539974>.

[57] KRUMMENACHER, F., JOEHL, N. "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning", *IEEE Journal of Solid-State Circuits*, v. 23, n. 3, pp. 750–758, 1987. ISSN: 00189200. doi: 10.1109/4.315.

[58] ASSAAD, R. S., SILVA-MARTINEZ, J. "The recycling folded cascode: A general enhancement of the folded cascode amplifier", *IEEE Journal of Solid-State Circuits*, v. 44, n. 9, pp. 2535–2542, 2009. ISSN: 00189200. doi: 10.1109/JSSC.2009.2024819.

[59] JOHNS, D., MARTIN, K. *Analog Integrated Circuit Design*. Wiley, 1996. ISBN: 0-471-14448-7.

[60] ALLEN, P. E., HOLBERG, D. R. *CMOS Analog Circuit Design*. Oxford University Press Inc, 2002. ISBN: 0·19·511644-5.

[61] CORTES, F. P., FABRIS, E., BAMPI, S. "Analysis and design of amplifiers and comparators in CMOS 0.35 um technology", *Microelectronics Reliability*, v. 44, n. 4, pp. 657–664, 2004. ISSN: 00262714. doi: 10.1016/j.microrel.2003.10.014.

[62] MANGANARO, G., DE GYVEZ, J. "A four-quadrant S2I switched-current multiplier", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, v. 45, n. 7, pp. 791–799, 1998. ISSN: 10577130. doi: 10.1109/82.700926. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=700926>.

[63] CHARLON, O., REDMAN-WHITE, W. "Ultra high-compliance CMOS current mirrors for low voltage charge pumps and references", *Proceedings of the 30th European Solid-State Circuits Conference*, pp. 227–230, 2004. doi: 10.1109/ESSCIR.2004.1356659.

[64] DATTA, T., ABSHIRE, P. "Mismatch compensation of CMOS current mirrors using floating-gate transistors", *Proceedings - IEEE International Symposium on Circuits and Systems*, pp. 1823–1826, 2009. ISSN: 02714310. doi: 10.1109/ISCAS.2009.5118132.

[65] SANDER, D., DATTA, T., ABSHIRE, P. "Mismatch compensation of a subthreshold CMOS current normalizer", *ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems*, pp. 3409–3412, 2010. doi: 10.1109/ISCAS.2010.5537862.

[66] TSIVIDIS, Y., MCANDREW, C. *Operation and Modeling of the MOS Transistor*. Oxford University Press Inc, 2012.

[67] LATHI, B. P. *Sinais e Sistemas Lineares*. Bookman, 2006.

[68] KINGET, P. R. "Device mismatch and tradeoffs in the design of analog circuits", *IEEE Journal of Solid-State Circuits*, v. 40, n. 6, pp. 1212–1224, 2005. ISSN: 00189200. doi: 10.1109/JSSC.2005.848021.

[69] DRENNAN, P. G., MCANDREW, C. C. "Understanding MOSFET mismatch for analog design", *IEEE Journal of Solid-State Circuits*, v. 38, n. 3, pp. 450–456, 2003. ISSN: 00189200. doi: 10.1109/JSSC.2002.808305.

Appendix A

Transistor Parameters

In this Appendix, the models for PMOS and NMOS transistors are presented. They were extracted using a curve fitting of the level 3 model into the simulated curves using BSIM3.3 model implemented in Cadence for the 0.35 μm process utilized in this thesis. The capacitance parameters (C_{ox} and C_{ov}) and mismatch parameters were obtained from the process manual. This simpler model helps designing the circuit by hand [66].

The MOS transistor is a four-terminals device, symbolized by Fig. A.1. G is the gate terminal, S is the source, D is the drain and B is the bulk of the transistor. V_{DS} is the drain-source voltage, V_{GS} is the gate-source voltage, V_{SB} is the source-bulk voltage, and I_D is the drain current.

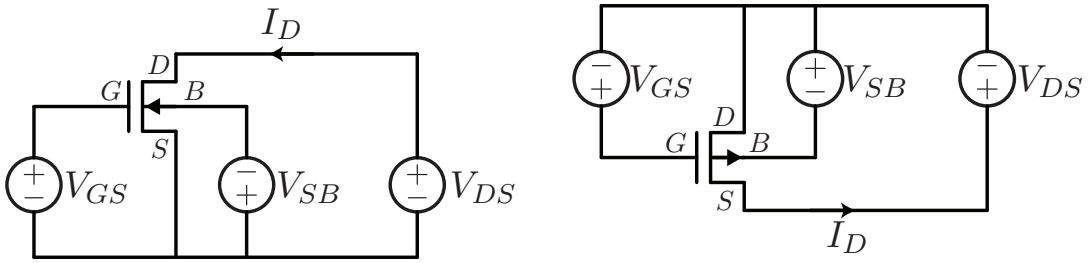


Figure A.1: MOS transistor symbol. (a) NMOS and (b) PMOS.

To be in the triode region, the condition is that $0 \leq V_{DS} \leq V_{DSat}$, and the drain current equation is given by

$$I_D = \frac{k_p W}{2\alpha L(1+\theta(V_{GS}-V_T))}\left((V_{GS}-V_T)V_{DS} - \frac{\alpha}{2}V_{DS}\right)^2 \tag{A.1}$$

and to be in the saturation region, the condition is that $V_{DS} \geq V_{DSat}$, and the train current is given by

$$I_D = \frac{k_p W}{L(1+\theta(V_{GS}-V_T))}(V_{GS}-V_T)^2 \tag{A.2}$$

where

$$\alpha = 1 + \frac{\gamma}{2\sqrt{\phi_0 + V_{SB}}} \tag{A.3}$$

$$V_T = V_{T0} + \gamma(\sqrt{\phi_0 + V_{SB}} - \sqrt{\Phi_0}) \tag{A.4}$$

$$V_{DSat} = \frac{V_{GS} - V_T}{\alpha} \tag{A.5}$$

The inversion coefficient (IC) can also be defined to observe if the transistor is operating in weak or strong inversion [48]. To be on strong inversion, $IC \gg 1$ and to be on weak inversion, $IC \ll 1$. The inversion coefficient is defined as

$$IC = \frac{I_D}{2\alpha\phi_T^2 k_p \frac{W}{L}} \tag{A.6}$$

Notice that the equations are suitable for both PMOS and NMOS transistors, however, for the PMOS transistor, the gate-source, drain-source and source-bulk voltages are negative values. The equation parameters for the NMOS are given in Table A.1, and the process parameters are given in Table A.2 and for the PMOS in Table A.3 and Table A.4.

Table A.1: NMOS transistor equation parameters.

Parameter	**Triode Region**	**Saturation Region**
$k_p(\mu A/V^2)$	198.3	165
V_{T0} (V)	0.55	0.49
θ	0.15	0.087
$\alpha\|_{V_{SB}=0}$	1.29	1.29
$\gamma(\sqrt{V})$	0.67	0.67
ϕ_0 (V)	1.3	1.3

Table A.2: NMOS transistor process parameters.

Parameter	**Value**
$C_{ox}(F/m^2)$	$4.558 \cdot 10^{-3}$
$C_{ov}(F/m)$	$1.2 \cdot 10^{-10}$
ϕ_t (V)	0.027
$\hat{A}_{kp} = \sigma_{kp}^2/k_p^2(m^{-2})$	$24 \cdot 10^{-18}$
$\hat{A}_{V_{T0}} = \sigma_{V_{T0}}^2/V_{T0}^2(m^{-2})$	$181 \cdot 10^{-18}$

Table A.3: PMOS transistor equation parameters.

Parameter	Triode Region	Saturation Region
$k_p(\mu A/V^2)$	54.6	64
V_{T0} (V)	-0.74	-0.69
θ	-0.13	-0.12
$\alpha\|_{V_{SB}=0}$	1.31	1.31
$\gamma(V^{-1/2})$	-0.44	-0.44
ϕ_0 (V)	0.52	0.52

Table A.4: PMOS transistor process parameters.

Parameter	Value
$C_{ox}(F/m^2)$	$4.453 \cdot 10^{-3}$
$C_{ov}(F/m)$	$1.2 \cdot 10^{-10}$
ϕ_t (V)	0.027
$\hat{A}_{kp} = \sigma^2_{kp}/k^2_p(m^{-2})$	$50.4 \cdot 10^{-18}$
$\hat{A}_{V_{T0}} = \sigma^2_{V_{T0}}/V^2_{T0}(m^{-2})$	$222 \cdot 10^{-18}$

Appendix B

Derivations

In this Appendix, the main circuit formulas are derived. The derivations will be based in the transistor equation presented in Appendix A.

B.1 Wide Swing Cascode Current Mirror

The Wide Swing cascode current mirror is the circuit shown in Fig. B.1. In this appendix, it is derived the minimum ratio W/L to implement the current mirror, as well as the biasing voltage range. The derivation will be executed for a NMOS current mirror, but it can be easily applicable for PMOS current mirrors as well.

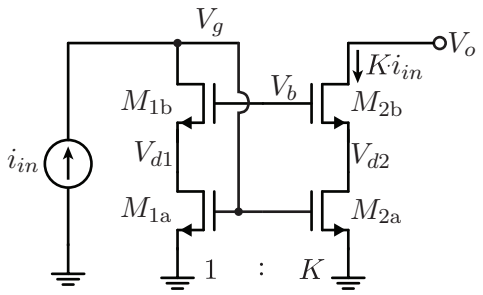


Figure B.1: Wide swing cascode current mirror circuit.

We can define the input current i_{in} to range from i_{MIN} to i_{MAX}. The output voltage V_o lowest value is defined by $V_{o\text{MIN}}$. From the circuit, it can be seen that $V_{d1} \approx V_{d2}$. Also, other relationships can be extracted, such as

$$V_{T1a} = V_{T2a} = V_{Ta} \tag{B.1}$$

$$V_{T1b} = V_{T2b} = V_{Tb} \tag{B.2}$$

$$\beta_2 = K\beta_1 \tag{B.3}$$

To ensure proper operation of the current mirror, each transistor must operate

in the saturation region. Transistors M_{1a} and M_{2a} operate in the saturation region if

$$V_d \geq \frac{V_g - V_{Ta}}{\alpha} \tag{B.4}$$

To keep M_{1b} in saturation, the condition to be met is

$$V_g - V_d \geq \frac{V_b - V_d - V_{Tb}}{\alpha} \tag{B.5}$$

Also, to keep M_{2b} in saturation, the condition to be met is

$$V_{o\text{MIN}} - V_d \geq \frac{V_b - V_d - V_{Tb}}{\alpha} \tag{B.6}$$

The current equations for the transistors are

$$i_{in} = \frac{\beta_1}{2\alpha}\left(V_g - V_{Ta}\right)^2 \tag{B.7}$$

$$i_{in} = \frac{\beta_1}{2\alpha}\left(V_b - V_d - V_{Tb}\right)^2 \tag{B.8}$$

from which we can obtain

$$V_g = \sqrt{\frac{2\alpha i_{in}}{\beta_1}} + V_{Ta} \tag{B.9}$$

$$V_d = V_b - V_{Tb} - \sqrt{\frac{2\alpha i_{in}}{\beta_1}} \tag{B.10}$$

Applying (B.9) and (B.10) in conditions (B.4) a lower-bound for V_b can be expressed as

$$V_b \geq V_{Tb} + \left(1 + \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{in}}{\beta_1}} \tag{B.11}$$

which must be true for every value of i_{in}. However, since the maximum value of i_{in} is given by i_{MAX}, if (B.12) is true for $i_{in} = i_{\text{MAX}}$, it is true for every value of i_{in}. Thus, it can be written

$$V_b \geq V_{Tb} + \left(1 + \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}} \tag{B.12}$$

The other two conditions give different upper-bounds for V_b, expressed as

$$V_b \leq \left(2 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{in}}{\beta_1}} + V_{Ta} + V_{Tb} \tag{B.13}$$

$$V_b \leq V_{o\text{MIN}} + V_{Tb} + \left(1 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{in}}{\beta_1}} \tag{B.14}$$

which must be true for every value of i_{in}. However, since the minimum value of i_{in} is given by i_{MIN}, if both upper-bounds are true for $i_{in} = i_{\text{MIN}}$, it is true for every value of i_{in}. Thus, they can be rewritten as

$$V_b \leq \left(2 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}} + V_{Ta} + V_{Tb} \tag{B.15}$$

$$V_b \leq V_{o\text{MIN}} + V_{Tb} + \left(1 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}} \tag{B.16}$$

Depending on the value of $V_{o\text{MIN}}$, one upper-bound is more restrictive than the other, which leads to two cases.

B.1.1 Case 1: (B.16) is stronger than (B.15)

In this case, V_b will range between

$$V_{o\text{MIN}} + V_{Tb} + \left(1 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}} \geq V_b \geq V_{Tb} + \left(1 + \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}} \tag{B.17}$$

where, in order to be a realizable circuit, the following must be true

$$V_{o\text{MIN}} + V_{Tb} + \left(1 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}} \geq V_{Tb} + \left(1 + \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}} \tag{B.18}$$

which can be simplified to

$$V_{o\text{MIN}} \geq \left(1 + \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}} - \left(1 - \frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}} \tag{B.19}$$

$$V_{o\text{MIN}} \geq \sqrt{\frac{2\alpha}{\beta_1}}\left[\left(1 + \frac{1}{\alpha}\right)\sqrt{i_{\text{MAX}}} - \left(1 - \frac{1}{\alpha}\right)\sqrt{i_{\text{MIN}}}\right] \tag{B.20}$$

Squaring both sides leads to

$$V_{o\text{MIN}}^2 \geq \frac{2\alpha}{\beta_1}\left[\left(1+\frac{1}{\alpha}\right)\sqrt{i_{\text{MAX}}}-\left(1-\frac{1}{\alpha}\right)\sqrt{i_{\text{MIN}}}\right]^2 \tag{B.21}$$

from which β_1 equation can be applied, finally leading to

$$\left(\frac{W}{L}\right)_{M_1} \geq \frac{2\alpha}{k_p V_{o\text{MIN}}^2}\left[\left(1+\frac{1}{\alpha}\right)\sqrt{i_{\text{MAX}}}-\left(1-\frac{1}{\alpha}\right)\sqrt{i_{\text{MIN}}}\right]^2 \tag{B.22}$$

where α and k_p are process parameters and $V_{o\text{MIN}}$ and i_{in} are design variables. A special situation happens when the input current is constant, where $i_{\text{MAX}} = i_{\text{MIN}} = i_{in}$. Thus, (B.22) simplifies to

$$\left(\frac{W}{L}\right)_{M_1} \geq \frac{8 i_{in}}{\alpha k_p V_{o\text{MIN}}^2} \tag{B.23}$$

B.1.2 Case 2: (B.14) is stronger than (B.13)

In this case, V_b will range between

$$\left(2-\frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}}+V_{Ta}+V_{Tb} \geq V_b \geq V_{Tb}+\left(1+\frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}} \tag{B.24}$$

where, in order to be a realizable circuit, the following must be true

$$\left(2-\frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}}+V_{Ta}+V_{Tb} \geq V_{Tb}+\left(1+\frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}} \tag{B.25}$$

which can be simplified to

$$V_{Ta} \geq \left(1+\frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MAX}}}{\beta_1}}-\left(2-\frac{1}{\alpha}\right)\sqrt{\frac{2\alpha i_{\text{MIN}}}{\beta_1}} \tag{B.26}$$

$$V_{Ta} \geq \sqrt{\frac{2\alpha}{\beta_1}}\left[\left(1+\frac{1}{\alpha}\right)\sqrt{i_{\text{MAX}}}-\left(2-\frac{1}{\alpha}\right)\sqrt{i_{\text{MIN}}}\right] \tag{B.27}$$

Squaring both sides leads to

$$V_{Ta}^2 \geq \frac{2\alpha}{\beta_1}\left[\left(1+\frac{1}{\alpha}\right)\sqrt{i_{\text{MAX}}}-\left(2-\frac{1}{\alpha}\right)\sqrt{i_{\text{MIN}}}\right]^2 \tag{B.28}$$

from which β_1 equation can be applied, finally leading to

$$\left(\frac{W}{L}\right)_{M_1} \geq \frac{2\alpha}{k_p V_{Ta}^2}\left[\left(1+\frac{1}{\alpha}\right)\sqrt{i_{\text{MAX}}}-\left(2-\frac{1}{\alpha}\right)\sqrt{i_{\text{MIN}}}\right]^2 \tag{B.29}$$

where α, V_{Ta} and k_p are process parameters and i_{in} is a design variable. A special situation happens when the input current is constant, where $i_{\text{MAX}} = i_{\text{MIN}} = i_{in}$. Thus, (B.29) simplifies to

$$\left(\frac{W}{L}\right)_{M_1} \geq \frac{2(2-\alpha)^2 i_{in}}{\alpha k_p V_{Ta}^2} \tag{B.30}$$

In both cases, the right hand side of the inequality represents the minimum ratio for a feasible current mirror. However, choosing a ratio close to the minimum represents a short range of values for V_b, which can be a problem with fabrication imperfections. It is best to use a ratio slightly higher than minimum to allow a wider range of values for V_b.

B.2 Differential Pair Transconductance

The simple differential pair implemented with PMOS transistors is presented in Fig. B.2. Both transistors have same dimensions, hence $\beta_a = \beta_b = \beta$. Also, they have bulk-source connections to avoid body effect.

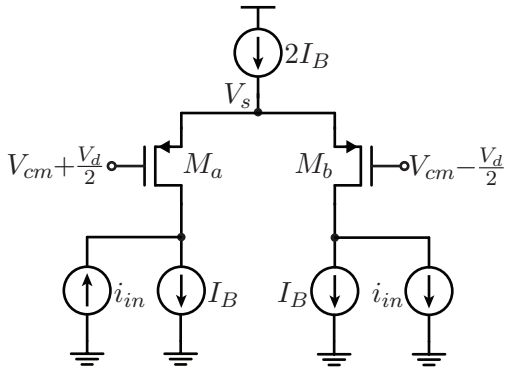


Figure B.2: Differential pair circuit.

The current equations, considering each transistor operating in the saturation region, are given by

$$I_B - i_{in} = \frac{\beta}{2\alpha}\left(V_s - V_{cm} - \frac{V_d}{2} - V_{T0p}\right)^2 \tag{B.31}$$

$$I_B + i_{in} = \frac{\beta}{2\alpha}\left(V_s - V_{cm} + \frac{V_d}{2} - V_{T0p}\right)^2 \tag{B.32}$$

This equation system can be rewritten by square-rooting both sides, leading to

$$\sqrt{\frac{2\alpha}{\beta}(I_B - i_{in})} = V_s - V_{cm} - \frac{V_d}{2} - V_{T0p} \tag{B.33}$$

$$\sqrt{\frac{2\alpha}{\beta}(I_B + i_{in})} = V_s - V_{cm} + \frac{V_d}{2} - V_{T0p}. \tag{B.34}$$

By subtracting (B.33) from (B.34), it leads to

$$V_d = \sqrt{\frac{2\alpha}{\beta}(I_B + i_{in})} - \sqrt{\frac{2\alpha}{\beta}(I_B - i_{in})} \tag{B.35}$$

which can be rewritten as

$$V_d = \sqrt{\frac{2\alpha I_B}{\beta}} \left(\sqrt{1 + \frac{i_{in}}{I_B}} - \sqrt{1 - \frac{i_{in}}{I_B}} \right) \tag{B.36}$$

The transconductance can be obtained using

$$Gm_{\text{SDP}} = \left(\frac{dV_d}{di_{in}} \right)^{-1} \tag{B.37}$$

and the derivative is given by

$$\frac{dV_d}{di_o} = \sqrt{\frac{2\alpha I_B}{\beta}} \left(\frac{1}{2I_B} \frac{1}{\sqrt{1 + \frac{i_{in}}{I_B}}} + \frac{1}{2I_B} \frac{1}{\sqrt{1 - \frac{i_{in}}{I_B}}} \right) \tag{B.38}$$

$$\frac{dV_d}{di_o} = \frac{1}{2I_B} \sqrt{\frac{2\alpha I_B}{\beta}} \left(\frac{\sqrt{1 + \frac{i_{in}}{I_B}} + \sqrt{1 - \frac{i_{in}}{I_B}}}{\sqrt{1 - \left(\frac{i_{in}}{I_B} \right)^2}} \right) \tag{B.39}$$

Applying (B.39) to (B.37), the transconductance is finally given by

$$Gm_{\text{SDP}} = \sqrt{\frac{\beta I_B}{2\alpha}} \frac{2\sqrt{1 - \left(\frac{i_{in}}{I_B} \right)^2}}{\sqrt{1 + \frac{i_{in}}{I_B}} + \sqrt{1 - \frac{i_{in}}{I_B}}} \tag{B.40}$$

B.3 Current Squarer

The current squarer is a part of the current multiplier. The circuit is presented in Fig. B.3. All the transistor have same dimensions, thus $\beta_{1a} = \beta_{1b} = \beta_{1c} = \beta_{1d} = \beta_{1e} = \beta$. Transistors M_{1b} and M_{1c} constitute a current mirror, and transistors M_{1d} and M_{1e} are responsible to set voltage node V_M. To be realizable, transistors must be bulk-source connected, thus canceling body effect. The derivation performed here is easily applicable to a PMOS implementation.

From the circuit it can be obtained

$$i_o = I_{D1a} + I_{D1c} \tag{B.41}$$

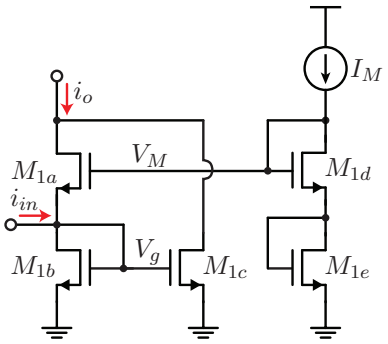


Figure B.3: Current squarer circuit.

and M_{1b} and M_{1c} constitute a current mirror, $I_{D1c} = I_{D1b} = I_{D1a} + i_{in}$. Hence

$$i_o = 2I_{D1a} + i_{in} \tag{B.42}$$

Considering every transistor operating in the saturation region, we have

$$I_{D1a} = \frac{\beta}{2\alpha}\left(V_M - V_g - V_T\right)^2 \tag{B.43}$$

and V_g is given by

$$V_g = V_T + \sqrt{\frac{2\alpha(I_{D1a} + i_{in})}{\beta}} \tag{B.44}$$

which can be applied to (B.43), leading to

$$I_{D1a} = \frac{\beta}{2\alpha}\left(V_M - V_T - \sqrt{\frac{2\alpha(I_{D1a} + i_{in})}{\beta}} - V_T\right)^2 \tag{B.45}$$

To simplify, let $V_X = V_M - 2V_T$. (B.45) can be expanded to

$$\frac{\cancel{2\alpha I_{D1a}}}{\cancel{\beta}} = \left(V_X^2 - 2V_X\sqrt{\frac{2\alpha(I_{D1a} + i_{in})}{\beta}} + \frac{\cancel{2\alpha I_{D1a}}}{\cancel{\beta}} + \frac{2\alpha i_{in}}{\beta}\right) \tag{B.46}$$

$$2V_X\sqrt{\frac{2\alpha(I_{D1a} + i_{in})}{\beta}} = V_X^2 + \frac{2\alpha i_{in}}{\beta} \tag{B.47}$$

$$\sqrt{\frac{2\alpha(I_{D1a} + i_{in})}{\beta}} = \frac{V_X}{2} + \frac{\alpha i_{in}}{\beta V_X} \tag{B.48}$$

Squaring both sides of (B.48) leads to

$$\frac{2\alpha I_{D1a}}{\beta} + \frac{2\alpha i_{in}}{\beta} = \frac{V_X^2}{4} + \frac{\alpha i_{in}}{\beta} + \left(\frac{\alpha i_{in}}{\beta V_X}\right)^2 \tag{B.49}$$

$$\frac{2\alpha I_{D1a}}{\beta} = \frac{V_X^2}{4} - \frac{\alpha i_{in}}{\beta} + \left(\frac{\alpha i_{in}}{\beta V_X}\right)^2 \tag{B.50}$$

$$I_{D1a} = \frac{\beta V_X^2}{8\alpha} - \frac{i_{in}}{2} + \frac{\alpha i_{in}^2}{2\beta V_X^2} \tag{B.51}$$

Finally, (B.51) can be applied to (B.42), leading to

$$i_o = \frac{\beta V_X^2}{4\alpha} - i_{in} + \frac{\alpha i_{in}^2}{\beta V_X^2} + i_{in} \tag{B.52}$$

where V_X can be applied, and (B.52) is rewritten as

$$i_o = \frac{\beta(V_M - 2V_T)^2}{4\alpha} + \frac{\alpha i_{in}^2}{\beta(V_M - 2V_T)^2} \tag{B.53}$$

The voltage V_M is obtained from transistors M_{1d} and M_{1e}. From the circuit, we obtain

$$V_M = V_{gs1d} + V_{gs1e} = 2V_T + 2\sqrt{\frac{2\alpha I_M}{\beta}} \tag{B.54}$$

and applying it to (B.53) leads to

$$i_o = \frac{\beta\frac{8\alpha I_M}{\beta}}{4\alpha} + \frac{\alpha i_{in}^2}{\beta\frac{8\alpha I_M}{\beta}} \tag{B.55}$$

$$i_o = 2I_M + \frac{i_{in}^2}{8I_M} \tag{B.56}$$

The final results shows that the output is proportional to i_{in}^2 scaled by the current I_M. A DC term is also presented at the output.

B.3.1 Biasing Current Limits

The current through M_{1a} must be observed for proper operation. Applying V_X to (B.51) leads to

$$I_{D1a} = \frac{\beta\frac{8\alpha I_M}{\beta}}{8\alpha} - \frac{i_{in}}{2} + \frac{\alpha i_{in}^2}{2\beta\frac{8\alpha I_M}{\beta}} = I_M - \frac{i_{in}}{2} + \frac{i_{in}^2}{16I_M} \tag{B.57}$$

which can be expressed in a compact way by

$$I_{D1a} = \frac{1}{I_M}\left(I_M - \frac{i_{in}}{4}\right)^2 \tag{B.58}$$

For seamless operation, M_{1a} must be kept into strong inversion through whole input range. The inversion coefficient IC from model EKV is a great way to define the

type of inversion. To guarantee strong inversion, $IC \geq 10$. From Appendix A, where transistors parameters are displayed, we obtain

$$\frac{I_{D1a}}{2\alpha\phi_T^2 k_p \frac{W}{L}} \geq 10 \tag{B.59}$$

$$\frac{\left(I_M - \frac{i_{in}}{4}\right)^2}{2I_M\alpha\phi_T^2 k_p \frac{W}{L}} \geq 10 \tag{B.60}$$

where an upper-bound for $\frac{W}{L}$ ratio is given by

$$\frac{W}{L} \leq \frac{\left(I_M - \frac{i_{in}}{4}\right)^2}{20I_M\alpha\phi_T^2 k_p} \tag{B.61}$$

The biasing voltage V_M is determined by the biasing current I_M. If the voltage V_M is too high, M_{1a} may operate in triode. To operate in the saturation region, the following must be true

$$V_{o\text{MIN}} - V_g \geq \frac{V_M - V_g - V_T}{\alpha} \tag{B.62}$$

$$\alpha V_{o\text{MIN}} \geq V_M + (\alpha - 1)V_g - V_T \tag{B.63}$$

where V_M is given by (B.54). V_g is given by (B.44), which depends on I_{D1a}. Applying (B.58) leads to

$$V_g = V_T + \sqrt{\frac{2\alpha}{\beta I_M}\left(I_M + \frac{i_{in}}{4}\right)^2} \tag{B.64}$$

The inequality becomes

$$\alpha V_{o\text{MIN}} \geq \alpha V_T + 2\sqrt{\frac{2\alpha I_M}{\beta}} + (\alpha - 1)\sqrt{\frac{2\alpha}{\beta I_M}\left(I_M + \frac{i_{in}}{4}\right)^2} \tag{B.65}$$

or on a compact form

$$\alpha(V_{o\text{MIN}} - V_T) \geq \sqrt{\frac{2\alpha}{\beta I_M}}\left[2I_M + (\alpha - 1)\left(I_M + \frac{i_{in}}{4}\right)\right] \tag{B.66}$$

$$\alpha(V_{o\text{MIN}} - V_T) \geq \sqrt{\frac{2\alpha}{\beta I_M}}\left[(\alpha + 1)I_M + (\alpha - 1)\frac{i_{in}}{4}\right] \tag{B.67}$$

Squaring both sides leads to

$$\alpha^2(V_{o\text{MIN}} - V_T)^2 \geq \frac{2\alpha}{\beta I_M}\left[(\alpha + 1)I_M + (\alpha - 1)\frac{i_{in}}{4}\right]^2 \tag{B.68}$$

Thus, an lower bound for W/L is given by

$$\frac{W}{L} \geq \frac{2}{k_p I_M \alpha (V_{o\text{MIN}} - V_T)^2} \left[(\alpha+1) I_M + (\alpha-1)\frac{i_{in}}{4} \right]^2 \tag{B.69}$$

In order to be realizable, the lower bound should be less than the upper bound. Thus, the condition is given by

$$\frac{\left(I_M - \frac{i_{in}}{4}\right)^2}{20 I_M \alpha \phi_T^2 k_p} \geq \frac{2}{k_p I_M \alpha (V_{o\text{MIN}} - V_T)^2} \left[(\alpha+1) I_M + (\alpha-1)\frac{i_{in}}{4} \right]^2 \tag{B.70}$$

which simplifies to

$$\left(I_M - \frac{i_{in}}{4} \right)^2 \geq \frac{40\phi_T^2}{(V_{o\text{MIN}} - V_T)^2} \left[(\alpha+1) I_M + (\alpha-1)\frac{i_{in}}{4} \right]^2 \tag{B.71}$$

Let

$$A_v = \frac{40\phi_T^2}{(V_{o\text{MIN}} - V_T)^2} \tag{B.72}$$

Thus the inequality is rearranged to

$$\left(I_M - \frac{i_{in}}{4} \right)^2 - A_v \left[(\alpha+1) I_M + (\alpha-1)\frac{i_{in}}{4} \right]^2 \geq 0 \tag{B.73}$$

Expanding the squared terms leads to

$$I_M^2 \left[1 - A_v(\alpha+1)^2\right] - \frac{I_M i_{in}}{2} \left[1 + A_v(\alpha^2-1)\right] + \frac{i_{in}^2}{16} \left[1 - A_v(\alpha-1)^2\right] \geq 0 \tag{B.74}$$

where the minimum biasing current, $I_{M\text{MIN}}$ leads to a second degree equation. The solutions are given by

$$I_{M\text{MIN}} = \frac{i_{in}}{4} \left[\frac{1 + A_v(\alpha^2-1) \pm 2\alpha\sqrt{A_v}}{1 - A_v(\alpha+1)^2} \right] \tag{B.75}$$

or on a more compact way

$$I_{M\text{MIN}} = \frac{i_{in}}{4} \left[\frac{(1 \pm \alpha\sqrt{A_v})^2 - A_v}{1 - A_v(\alpha+1)^2} \right] \tag{B.76}$$

Since A_v must be positive, the maximum solution is given for the maximum input current $i_{in\text{MAX}}$ and for the positive sign. Hence

$$I_{M\text{MIN}} = \frac{i_{in\text{MAX}}}{4} \left[\frac{(1 + \alpha\sqrt{A_v})^2 - A_v}{1 - A_v(\alpha+1)^2} \right] \tag{B.77}$$

Appendix C

Error Analysis

The goal of this Appendix is to observe how non-ideal effects on the circuit building blocks affects the measurement result. To begin this analysis, we must establish a way to model these non-ideal effects that can affect the final measurement result. These errors falls into two categories: deterministic errors and random errors. Deterministic errors are derived from Mosfet's second-order effects, such as channel modulation, body effect and parasitic components [66]. Even though they are possible to determine, attempting to consider them while designing the circuit would lead to extensive calculations, due to its complexity. Thus, we consider them *non-linearities*.

Random errors arise from imperfections during manufacturing which result in different characteristics between identically design circuits [66, p. 585-592]. These imperfections are expressed by two class of errors: mismatch and process parameters variation. While the latter one affects the circuits globally and it can be avoided with a careful physical design (layout), mismatch is very unpredictable and it affects the circuit locally (from building block to building block) and also globally (from circuit dye to circuit dye). Nonetheless, due to great research work done by Pelgrom [47], it is possible to design the circuit considering mismatch statistical variation and achieve a desired fabrication yield, making manufacture possible.

Throughout this analysis, we will work with the first order errors, so that linearity properties of the system are kept. Higher order errors will be considered as non-linearities and will not be treated in this analysis. First order errors, on the other hand, are expressed in the analysis by a gain error and an offset error.

The *gain error* behaves as a constant term multiplying the transfer function of the system. Since most of our circuit are composed current mirrors, mismatch will be the main cause of gain error.

The *offset* behaves as a constant term added into the system. Therefore, when no signal is applied to the system, a constant output is observed. Due to linearity properties, this offset is often modeled as another input into the system. However,

to analyze the discrete-time system using a unilateral Z-transform, the offset must be a causal input, thus it must be multiplied by a Heaviside step function $u[n]$, where

$$u[n] = \begin{cases} 0, n < 0 \\ 1, n \geq 0 \end{cases} \tag{C.1}$$

and it is represented on the Z-domain by $U(z)$, where

$$U(z) = \frac{1}{1 - z^{-1}} \tag{C.2}$$

To simplify the analysis, we will use superposition theorem for linear systems [67, p. 106] which allows a separate analysis for each system input. Thus, the final gain error will be obtained with an offset equal to zero and the final offset will be obtained with an system input equal to zero.

To perform this analysis we adopt an bottom-top strategy, going from building blocks to all-pass section, passing through the all-pass transfer function, until we reach the whole system. The greek letters α and β were used to denote gain error and offset, respectively.

C.1 Non-Ideal Effects on Building Blocks

Four building blocks were used to build the structurally all-pass section (SAPS) that composes the Hilbert transformer. The current memory cell, differential current mirror, output copy and the coefficient gain block. However, the consequences of errors into the coefficient are much bigger, since it affects the transfer function directly. That was the main reason to develop the coefficient sharing technique presented on Chapter 3.3. Thus, the coefficient error is not considered on this analysis.

C.1.1 Current Memory Cell

Ideally, a current memory cell (CMC) is a perfect half-unit delay with a signal inversion, as pictured in Fig C.1a. However,the need for a larger loop gain led the choice of a Zero-Voltage Switching (ZVS) architecture, as explained in Chapter 5.1. The main advantage of the chosen CMC is the absence of signal dependent error (or high-attenuation, making it negligible). Therefore, the ZVS-CMC is only affected by offset error, and it results into the system of Fig C.1b. Since the CMCs are used into the all-pass section as a cascade of four CMCs, as shown in Fig C.1c, to simplify system analysis we will condensate them into a single block and observe the offset

behavior.

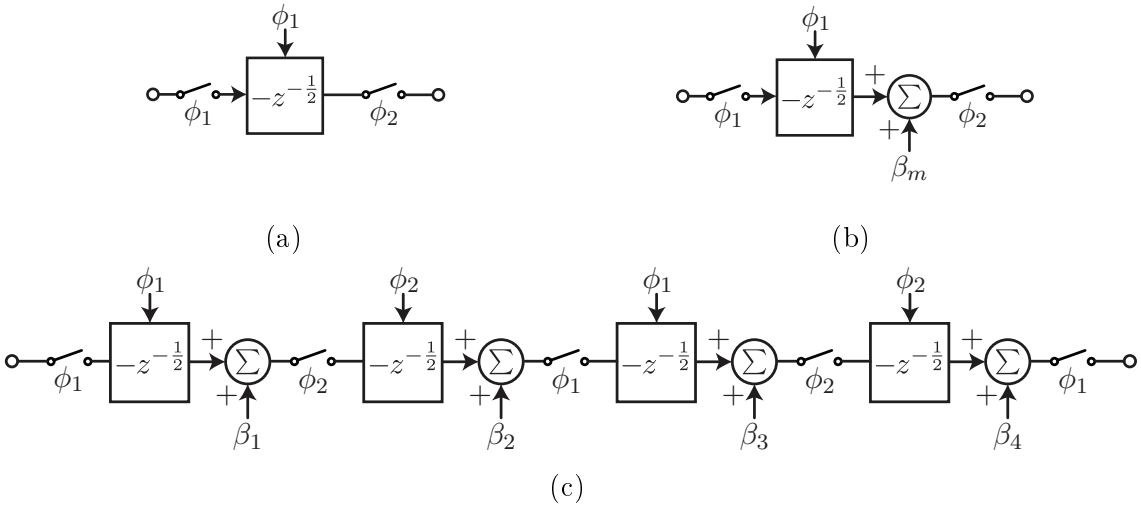


Figure C.1: Block representation of an ideal current memory cell (a) and a Zero-voltage switching current memory cell (b). A cascade of four ZVS-CMC blocks (c).

To find the cascade's final offset we use superposition, hence the input current is grounded and the output is observed. From Fig C.1c, we obtain

$$\beta_{\mathrm{CD}}(z) = \left[-\beta_1 z^{-\frac{3}{2}} + \beta_2 z^{-1} - \beta_3 z^{-\frac{1}{2}} + \beta_4\right] U(z) \tag{C.3}$$

To obtain the offset value after the transient, we can use the final value theorem (FVT), which states [67, p. 460]

$$\lim_{t\to\infty} f(t) = \lim_{z\to 1}(z-1)F(z) \tag{C.4}$$

Applying the FVT to $\beta_{\mathrm{CD}}(z)$, we obtain

$$\beta_{\mathrm{CD}} = \lim_{z\to 1} \cancel{(z-1)} \left[-\beta_1 z^{-\frac{3}{2}} + \beta_2 z^{-1} - \beta_3 z^{-\frac{1}{2}} + \beta_4\right] \frac{z}{\cancel{z-1}} \tag{C.5}$$

$$\beta_{\mathrm{CD}} = -\beta_1 + \beta_2 - \beta_3 + \beta_4 \tag{C.6}$$

The offset of a single CMC is not deterministic, and not only can have a local variation - i.e between current memory cells inside the same integrated circuit - due to mismatch and process gradient, but also can have a global variation - i.e between different integrated circuit - due to process parameters variation. So, it is modeled using a normal distribution with a non-zero mean value, since the zero-voltage switching architecture is being used. However, each offset has same average and standard deviation, which are expressed by

$$\overline{\beta_m} = \overline{\beta_{\mathrm{CMC}}}, \quad \text{for m=1,2,3,4.} \tag{C.7}$$

and

$$\sigma_{\beta_m} = \sigma_{\beta_{\mathrm{CMC}}}, \quad \text{for m=1,2,3,4.} \tag{C.8}$$

A sum of normal distributions is also a normal distribution, with the mean value given by

$$\overline{\beta_{\mathrm{CD}}} = -\overline{\beta_1} + \overline{\beta_2} - \overline{\beta_3} + \overline{\beta_4} = 0 \tag{C.9}$$

and variance given by

$$\sigma^2_{\beta_{\mathrm{CD}}} = \sigma^2_{\beta_1} + \sigma^2_{\beta_2} + \sigma^2_{\beta_3} + \sigma^2_{\beta_4} = 4\sigma^2_{\beta_{\mathrm{CMC}}} \tag{C.10}$$

The cascade of CMCs will be represented by the block diagram from Fig. C.2.

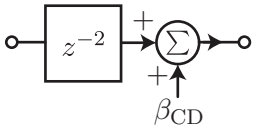


Figure C.2: Block representation of a cascade of four current memory cells.

C.1.2 Differential Current Mirror

The differential current mirror (DCM) is a crucial block in our system, since it is responsible for creating both positive and negative copies of the input signal. Its ideal implementation is shown in Fig. C.3, but is repeated here for clarity.

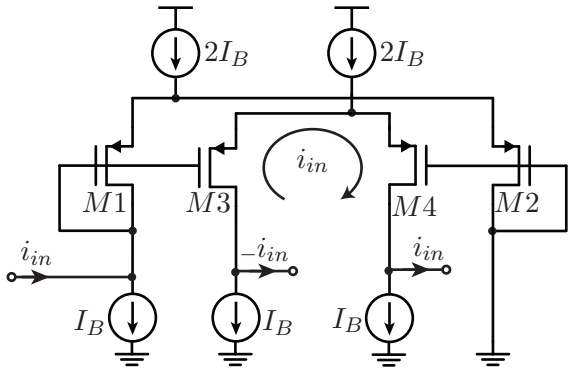


Figure C.3: Differential Current Mirror implementation.

The transistor matching in this circuit is essential for the well-behavior of the whole system. However, because of its structure, some interesting properties are

maintained. The use of two differential pairs, M1-M2 and M3-M4, generates a symmetry between both output curves. A mismatch between transistors on the same pair does not affect the differential signal, and it creates a common-mode, which will be modeled as an offset. Mismatch between the mirrors, i.e M1-M3 and M2-M4, will introduce a gain error into the current transfer curve. Nonetheless, this gain error can be designed to meet the desired yield using Pelgrom's mismatch models [47].

The key point on this circuit is that, since the input current circulates through M3-M4, the gain error will be equal for both output paths, and therefore not affecting the coefficient value of the all-pass section.

Another mismatch that can occur is between the current sources. Since they will be implemented by transistors as well, they are subject to non-ideal effects as well. Thus, the offset on each output can be different. A possible block diagram representation of the DCM with gain and offset is presented on Fig. C.4a. The two offset components, β_1 and β_2 can be distributed using linearity properties of linear systems, and leading to the representation of Fig. C.4b.

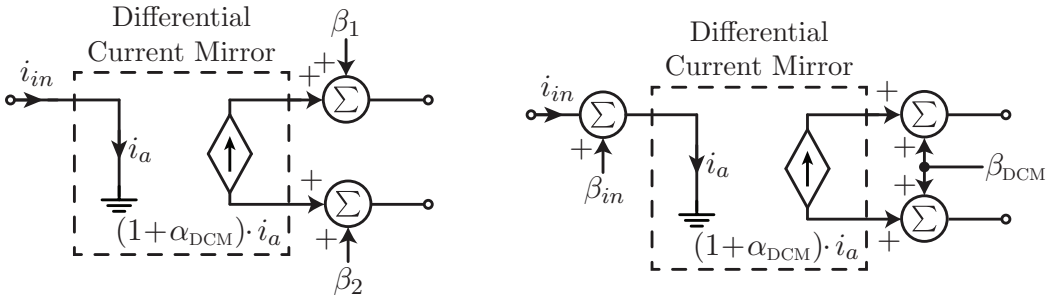


Figure C.4: Block representation of a differential current mirror with asymmetric offset errors (a) and with symmetric offset errors (b).

It is easy to see that

$$\beta_{\mathrm{DCM}} = \frac{\beta_1 + \beta_2}{2} \tag{C.11}$$

and

$$\beta_{in} = \frac{\beta_1 - \beta_2}{2(1 + \alpha_{\mathrm{DCM}})} \tag{C.12}$$

C.1.3 Output Copy Current Mirror

The output copy is performed by a basic current mirror. Similarly to the differential current mirror, a mismatch between the mirror's transistors introduces a gain error into the copy, which can be controlled to meet yield specifications. A mismatch

between the current sources, however, introduces an offset at the output. The block representation of the output copy with gain error and offset is presented in Fig. C.5.

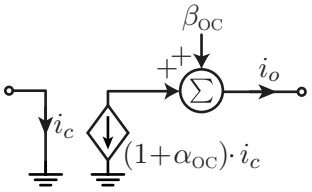


Figure C.5: Block representation of an output copy current mirror.

C.1.4 From Building Blocks to All-Pass Section

After modeling the errors on each building block, we can substitute them into the structurally all-pass section (SAPS), resulting in Fig. C.6. The subscript i represents the all-pass transfer function index and j the all-pass section index. Thus, the SAPS pictured in Fig. C.6 is the j'th all-pass section into the i'th all-pass transfer function.

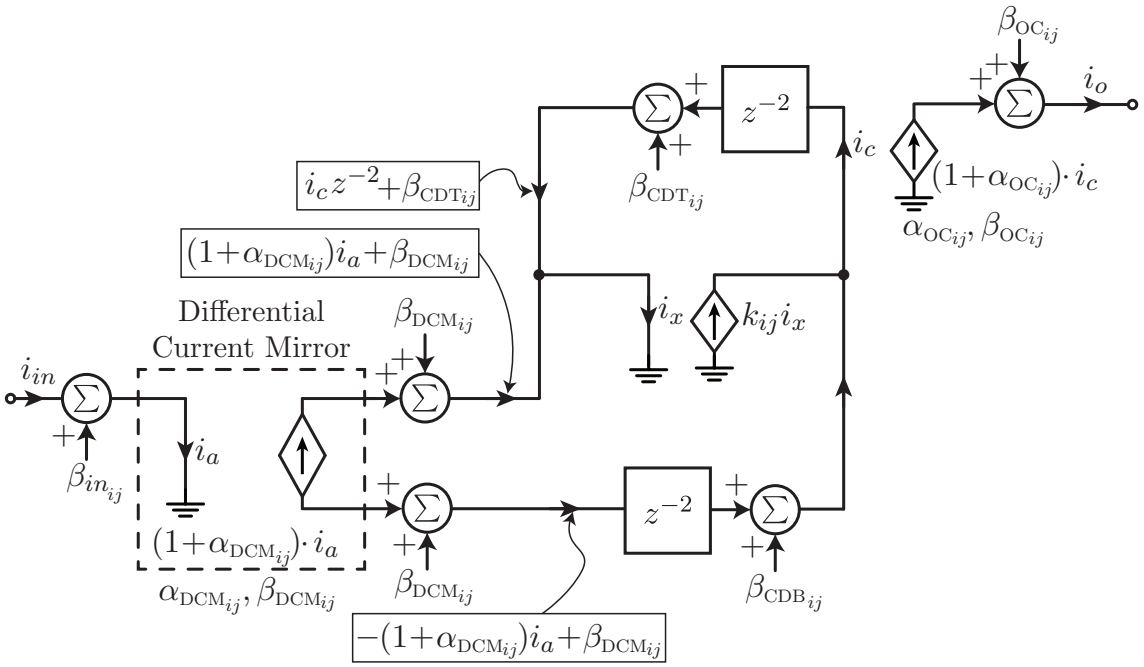


Figure C.6: Block diagram of a structurally all-pass section with gain error and offset from building blocks.

To obtain the total gain error, we use the superposition theorem and ground the offsets. From the block diagram, we obtain

$$i_o|_{\beta=0} = (1+\alpha_{\mathrm{OC}_{ij}})(1+\alpha_{\mathrm{DCM}_{ij}})A_{ij}(-z^2)i_{in} \tag{C.13}$$

where

$$A_{ij}(-z^2) = \frac{-z^{-2} + k_{ij}}{1 - k_{ij}z^{-2}}, \tag{C.14}$$

Since both gain errors $\alpha_{\mathrm{OC}_{ij}}$ and $\alpha_{\mathrm{DCM}_{ij}} \ll 1$, we can approximate (C.13) by

$$i_o|_{\beta=0} \approx (1 + \alpha_{ij})A_{ij}(-z^2)i_{in} \tag{C.15}$$

where α_{ij} is the total gain error of the j'th all-pass section into the i'th all-pass transfer function, whose value is given by

$$\alpha_{ij} = \alpha_{\mathrm{OC}_{ij}} + \alpha_{\mathrm{DCM}_{ij}} \tag{C.16}$$

The resulting gain error is a random variable with mean value given by

$$\overline{\alpha_{ij}} = \overline{\alpha_{\mathrm{OC}}} + \overline{\alpha_{\mathrm{DCM}}} = 0 \tag{C.17}$$

and variance given by

$$\sigma^2_{\alpha_{ij}} = \sigma^2_{\alpha_{\mathrm{OC}}} + \sigma^2_{\alpha_{\mathrm{DCM}}} \tag{C.18}$$

To obtain the total offset error of the all-pass section, we ground the input, and consider just the offsets. Thus, we have

$$i_o|_{i_{in}=0} = (1 + \alpha_{\mathrm{OC}_{ij}})i_c + \beta_{\mathrm{OC}_{ij}}U(z) \tag{C.19}$$

where

$$\begin{aligned} i_c|_{i_{in}=0} = \{&\beta_{\mathrm{CDB}_{ij}} + k_{ij}\left[\beta_{\mathrm{DCM}_{ij}} + \beta_{\mathrm{CDT}_{ij}} + (1 + \alpha_{\mathrm{DCM}_{ij}})\beta_{in_{ij}}\right] \\ &+ z^{-2}[\beta_{\mathrm{DCM}_{ij}} - (1 + \alpha_{\mathrm{DCM}_{ij}})\beta_{in_{ij}}]\,\}\,\frac{U(z)}{1 - k_{ij}z^{-2}} \end{aligned} \tag{C.20}$$

This offset has a transient, and we are interested into the constant value at the end. Therefore, we use the FVT and get

$$\beta_{ij} = \lim_{z\to 1}(z - 1)\; i_o(z)|_{i_{in}=0} \tag{C.21}$$

where after applying (C.20) into (C.19) leads to

$$\begin{aligned} \beta_{ij} = \lim_{z\to 1} \cancel{(z-1)}(1 + \alpha_{\mathrm{OC}})\,&\left[\beta_{\mathrm{CDB}_{ij}} + k_{ij}\left(\beta_{\mathrm{DCM}_{ij}} + \beta_{\mathrm{CDT}_{ij}} + (1 + \alpha_{\mathrm{DCM}_{ij}})\beta_{in_{ij}}\right)\right. \\ &\left. + z^{-2}(\beta_{\mathrm{DCM}_{ij}} - (1 + \alpha_{\mathrm{DCM}_{ij}})\beta_{in_{ij}})\,\right]\frac{z}{\cancel{(z-1)}(1 - k_{ij}z^{-2})} \end{aligned} \tag{C.22}$$

which simplifies to

$$\beta_{ij} = (1+\alpha_{\mathrm{OC}_{ij}}) \left[\frac{\beta_{\mathrm{CDB}_{ij}} + k_{ij}\beta_{\mathrm{CDT}_{ij}} + \beta_{\mathrm{DCM}_{ij}}(1+k_{ij})}{1-k_{ij}} - (1+\alpha_{\mathrm{DCM}_{ij}})\beta_{in_{ij}} \right] + \beta_{\mathrm{OC}_{ij}} \tag{C.23}$$

The resulting offset error is a random variable with mean value given by

$$\overline{\beta_{ij}} = (1+\overline{\alpha_{\mathrm{OC}}}) \left[(\overline{\beta_{\mathrm{CD}}} + \overline{\beta_{\mathrm{DCM}}}) \left(\frac{1+k_{ij}}{1-k_{ij}} \right) - (1+\overline{\alpha_{\mathrm{DCM}}})\overline{\beta_{\mathrm{in}}} \right] + \overline{\beta_{\mathrm{OC}}} = 0 \tag{C.24}$$

and variance given by

$$\sigma^2_{\beta_{ij}} \approx \left(\sigma^2_{\beta_{\mathrm{CD}}} + \sigma^2_{\beta_{\mathrm{DCM}}}\right) \left(\frac{1+k_{ij}}{1-k_{ij}} \right) + \sigma^2_{\beta_{\mathrm{in}}} + \sigma^2_{\beta_{\mathrm{OC}}} \tag{C.25}$$

The final relationship between input and output is given by

$$i_o = (1+\alpha_{ij})A_{ij}(-z^2)i_{in} + \beta_{ij} \tag{C.26}$$

and it is represented in Fig C.7. One can see that the gain and offset errors from building blocks do not affect the transfer function of the Hilbert transformer and by extension, its phase error. Thus, we can consider the phase error *independent* from the gain and offset errors of building blocks.

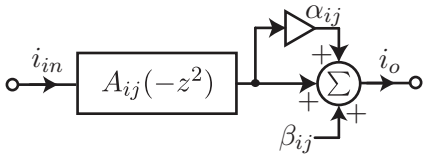


Figure C.7: Equivalent block representation of a structurally all-pass section.

C.1.5 From All-Pass Section to All-Pass Transfer function

To implement a Hilbert transformer, depending on its specifications, it is needed a cascade of all-pass section. Thus, we need to observe how the gain error and offset on each all-pass section affect the whole transfer function.

Remembering (2.25) from Chapter 2, the all-pass transfer functions to implement the Hilbert transformer can be represented by

$$A_i(-z^2) = \prod_{j=1}^{N_i} A_{ij}(-z^2) = \prod_{j=1}^{N_i} \frac{k_{ij} - z^{-2}}{1 - k_{ij}z^{-2}}, \text{ for i=1,2,} \tag{C.27}$$

when ideal all-pass sections are used. Considering the all-pass section representation

from Fig. C.7, the cascade of all-pass section which implements the all-pass transfer function can be represented by Fig. C.8.

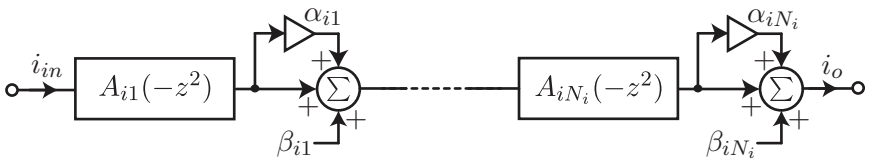


Figure C.8: Block diagram of a cascade of N_i structurally all-pass sections.

In a cascade of all-pass sections, the output of the previous section works as an input for the next section. To find the gain and offset errors, the superposition theorem is used once again. Each offset is set equal to zero, and the input current i_{in} path is observed at the output, resulting in

$$i_o|_{\beta=0} = \left[\prod_{j=1}^{N_i}(1+\alpha_{ij})A_{ij}(-z^2)\right] i_{in} \tag{C.28}$$

which after applying (C.27) leads to

$$i_o|_{\beta=0} = \left[\prod_{j=1}^{N_i}(1+\alpha_{ij})\right] A_i(-z^2) i_{in} \tag{C.29}$$

Since $\alpha_{ij} \ll 1$, the crossed terms are negligible and it result into

$$i_o|_{\beta=0} = (1+\alpha_i)\, A_i(-z^2) i_{in} \tag{C.30}$$

where

$$\alpha_i = \sum_{j=1}^{N_i} \alpha_{ij} = \sum_{j=1}^{N_i} \left(\alpha_{\mathrm{OC}_{ij}} + \alpha_{\mathrm{DCM}_{ij}}\right) \tag{C.31}$$

and it is a random variable with mean value given by

$$\overline{\alpha_i} = \sum_{j=1}^{N_i} \overline{\alpha_{ij}} = 0 \tag{C.32}$$

and its variance given by

$$\sigma^2_{\alpha_i} = \sum_{j=1}^{N_i} \sigma^2_{\alpha_{ij}} = (\sigma^2_{\alpha_{\mathrm{OC}}} + \sigma^2_{\alpha_{\mathrm{DCM}}}) \sum_{j=1}^{N_i} 1 = N_i(\sigma^2_{\alpha_{\mathrm{OC}}} + \sigma^2_{\alpha_{\mathrm{DCM}}}) \tag{C.33}$$

To obtain the total offset, the input current is set to zero and the output is observed. From Fig. C.8, we obtain

$$i_o(z)|_{i_{in}=0} = \sum_{j=1}^{N_i} \left\{ \beta_{ij} U(z) \left[\prod_{k=j+1}^{N_i} (1+\alpha_{ik}) A_{ik}(-z^2) \right] \right\} \tag{C.34}$$

To obtain the value after the transient, we use the FVT and get

$$\beta_i = \lim_{z\to 1}(z-1)\; i_o(z)|_{i_{in}=0} \tag{C.35}$$

$$\beta_i = \sum_{j=1}^{N_i} \left\{ \beta_{ij} \cdot 1 \left[\prod_{k=j+1}^{N_i} (1+\alpha_{ik}) \left(\frac{k_{ik}-1}{1-k_{ik}} \right) \right] \right\} \tag{C.36}$$

$$\beta_i = \sum_{j=1}^{N_i} \left\{ \beta_{ij} \left[\prod_{k=j+1}^{N_i} (1+\alpha_{ik})(-1) \right] \right\} = \sum_{j=1}^{N_i} \left[\beta_{ij} (-1)^{N_i-j} \prod_{k=j+1}^{N_i} (1+\alpha_{ik}) \right] \tag{C.37}$$

and since $\alpha_{ik} \ll 1$, the crossed terms are negligible and (C.37) can be simplified to

$$\beta_i \approx \sum_{j=1}^{N_i} (-1)^{N_i-j} \beta_{ij} \left(1 + \sum_{k=j+1}^{N_i} \alpha_{ik} \right). \tag{C.38}$$

β_i is a random variable with mean value given by

$$\overline{\beta_i} = \sum_{j=1}^{N_i} (-1)^{N_i-j} \overline{\beta_{ij}} \left(1 + \sum_{k=j+1}^{N_i} \overline{\alpha_{ik}} \right) = 0 \tag{C.39}$$

and since β_{ij} and α_{ik} are independent, the variance of β_i is given by

$$\sigma^2_{\beta_i} = \sum_{j=1}^{N_i} \sigma^2_{\beta_{ij}} \left(1 + \sum_{k=j+1}^{N_i} \sigma^2_{\alpha_{ik}} \right) \tag{C.40}$$

C.1.6 From All-Pass Transfer Functions to Reactive Power Measurement System

The method chosen for measuring reactive power in this dissertation was the 'two Hilbert transformer' method presented on Chapter 3.2.3. For clarity, the method's block diagram will be repeated here with offset and gain error added to the system, resulting on Fig C.9.

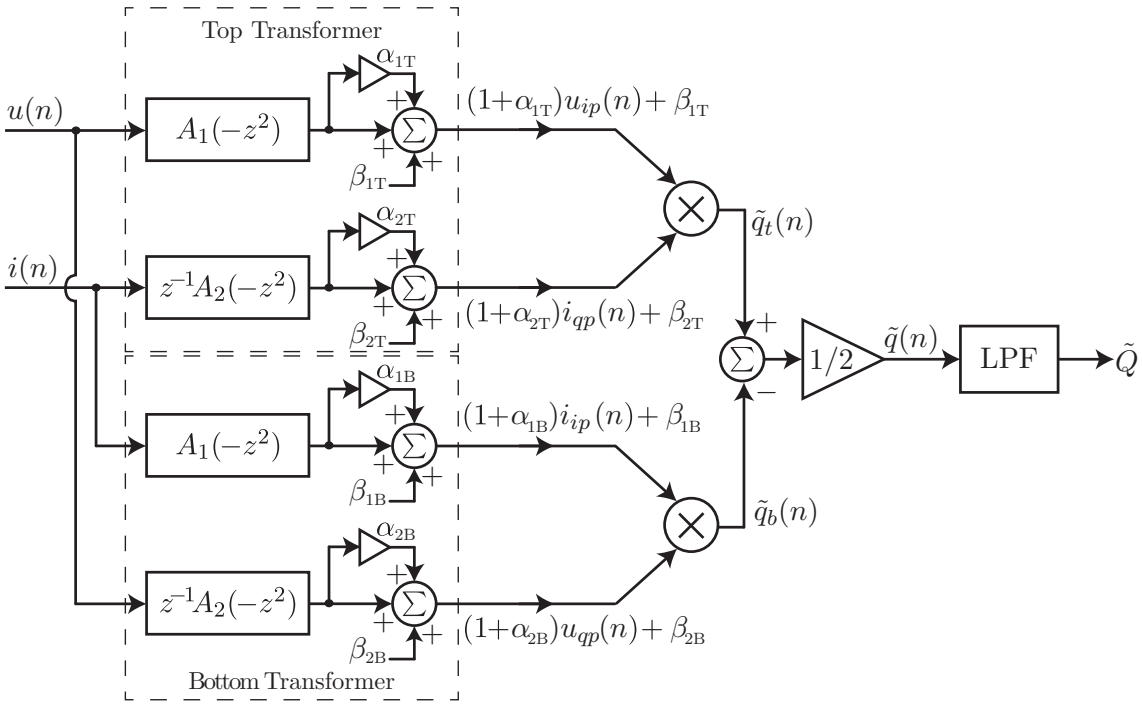


Figure C.9: Reactive power measurement system using two Hilbert transformers with all-pass transfer functions with gain and offset errors.

The voltage signals $u_{ip}(n)$ and $u_{qp}(n)$ were derived on equations (3.6) and (3.23), respectively. The current signals $i_{ip}(n)$ and $i_{qp}(n)$ are described on (3.22) and (3.13), respectively. After the multiplication, we obtain the top transformer component

$$\tilde{q}_t(n) = (1+\alpha_{1T})(1+\alpha_{2T})u_{ip}(n)i_{qp}(n)+\beta_{1T}(1+\alpha_{2T})i_{qp}(n)+\beta_{2T}(1+\alpha_{1T})u_{ip}(n)+\beta_{1T}\beta_{2T} \tag{C.41}$$

and the bottom component

$$\tilde{q}_b(n) = (1+\alpha_{1B})(1+\alpha_{2B})i_{ip}(n)u_{qp}(n)+\beta_{1B}(1+\alpha_{2B})u_{qp}(n)+\beta_{2B}(1+\alpha_{1B})i_{ip}(n)+\beta_{1B}\beta_{2B} \tag{C.42}$$

As explained before, each component will have $2N+1$ harmonics, and we are interested on the DC ones $\tilde{q}_{t0}$ and $\tilde{q}_{b0}$, given by

$$\tilde{q}_{t0} = (1+\alpha_{1T})(1+\alpha_{2T})\sum_{k=1}^{N} V_k I_k \sin(\varphi_k - \varepsilon_k) + \beta_{1T}\beta_{2T} \tag{C.43}$$

and

$$\tilde{q}_{b0} = (1+\alpha_{1B})(1+\alpha_{2B})\sum_{k=1}^{N} V_k I_k \sin(-\varphi_k - \varepsilon_k) + \beta_{1B}\beta_{2B} \tag{C.44}$$

After the low-pass filter with cutoff frequency below the fundamental, only the DC component passes, leading to

$$\tilde{Q} = \frac{1}{2}[\tilde{q}_{t0} - \tilde{q}_{b0}] \tag{C.45}$$

$$\begin{aligned}\tilde{Q} = \frac{1}{2}\sum_{k=1}^{N} V_k I_k \left[(1+\alpha_{1\mathrm{T}})(1+\alpha_{2\mathrm{T}})\sin(\varphi_k - \varepsilon_k)\right. \\ \left. - (1+\alpha_{1\mathrm{B}})(1+\alpha_{2\mathrm{B}})\sin\left(-\varphi_k - \varepsilon_k\right)\right] + \beta_Q\end{aligned} \tag{C.46}$$

where

$$\beta_Q = \frac{1}{2}(\beta_{1\mathrm{T}}\beta_{2\mathrm{T}} - \beta_{1\mathrm{B}}\beta_{2\mathrm{B}}) \tag{C.47}$$

Some simplifications can be made, since the coefficient sharing all-pass section will be used on our system. When using coefficient sharing all-pass sections, both top and bottom transfer functions have the same gain error, thus $\alpha_{1\mathrm{T}} = \alpha_{1\mathrm{B}} = \alpha_1$ and $\alpha_{2\mathrm{T}} = \alpha_{2\mathrm{B}} = \alpha_2$. Therefore (C.46) can be simplified to

$$\tilde{Q} = \frac{1}{2}(1+\alpha_1)(1+\alpha_2)\sum_{k=1}^{N} V_k I_k \left[\sin(\varphi_k - \varepsilon_k) - \sin(-\varphi_k - \varepsilon_k)\right] + \beta_Q \tag{C.48}$$

$$\tilde{Q} = (1+\alpha_1)(1+\alpha_2)\sum_{k=1}^{N} V_k I_k \sin(\varphi_k)\cos(\varepsilon_k) + \beta_Q \tag{C.49}$$

$$\tilde{Q} \approx (1+\alpha_1+\alpha_2)\sum_{k=1}^{N} Q_k \left(1 - \frac{1}{2}\varepsilon_k^2\right) + \beta_Q \tag{C.50}$$

where, after applying (C.31) leads to

$$\tilde{Q} \approx (1+\alpha_Q)\cdot\sum_{k=1}^{N} Q_k \left(1 - \frac{1}{2}\varepsilon_k^2\right) + \beta_Q \tag{C.51}$$

with

$$\alpha_Q = \sum_{j=1}^{N_1}\left(\alpha_{\mathrm{OC}_{1j}} + \alpha_{\mathrm{DCM}_{1j}}\right) + \sum_{j=1}^{N_2}\left(\alpha_{\mathrm{OC}_{2j}} + \alpha_{\mathrm{DCM}_{2j}}\right) \tag{C.52}$$

Some important points can be observed from the final result. Firstly, the gain error of the measurement is the sum of the gain errors from each differential current mirror and output copy current mirrors of the system. Also, the gain error is independent of the reactive power value. This allows a calibration routine to compensate for the gain errors of these blocks. Secondly, the offset error β_Q, expressed by (C.47),

consists in a product of two offsets. Since each offset is small, their product becomes insignificant when compared to the other terms of (C.51). Lastly, it can be seen that the effect of the phase error ε_k in the measurement result is signal-dependent. Therefore, it cannot be predicted beforehand.

Since α_Q and β_Q are random variables, their mean and variance can be obtained. For α_Q, the mean value is given by

$$\overline{\alpha_Q} = \sum_{j=1}^{N_1} (\overline{\alpha_{\mathrm{OC}}} + \overline{\alpha_{\mathrm{DCM}}}) + \sum_{j=1}^{N_2} (\overline{\alpha_{\mathrm{OC}}} + \overline{\alpha_{\mathrm{DCM}}}) = 0 \tag{C.53}$$

and variance given by

$$\sigma_{\alpha_Q} = (N_1 + N_2) \left(\sigma^2_{\alpha_{\mathrm{OC}}} + \sigma^2_{\alpha_{\mathrm{DCM}}}\right). \tag{C.54}$$

For β_Q, the mean value is given by

$$\overline{\beta_Q} = \frac{1}{2}(\overline{\beta_1} \cdot \overline{\beta_2} - \overline{\beta_1} \cdot \overline{\beta_2}) = 0 \tag{C.55}$$

and variance given by

$$\sigma_{\beta_Q} = \frac{1}{4}(\sigma^2_{\beta_1}\sigma^2_{\beta_2} + \sigma^2_{\beta_1}\sigma^2_{\beta_2}) = \frac{\sigma^2_{\beta_1}\sigma^2_{\beta_2}}{2} \tag{C.56}$$

Appendix D

Mismatch on Transistors

During the manufacturing process of an integrated circuits, the parameters that dictates circuit operation, such as gate oxide capacitance, mobility, and many other, are subject to random variations in their nominal values. In order to mitigate these errors and obtain a design yield, a mathematical model was developed by Pelgrom [47]. In this Appendix, his models are presented and a deep study of the effects of these random errors into the circuits implemented in this work is performed.

D.1 Propagation of Uncertainty

The propagation of uncertainty is the effect of variables' errors on a function of these variables. Consider a function of n variables f, where the variables are represented by a vector $\vec{x} = \langle x_1, x_2, ..., x_n \rangle$. $f(\vec{x})$ can be approximated using Taylor expansion and truncating on a first order term, leading to

$$f(\vec{x}) \approx f(\overline{x}) + \sum_{i}^{n} \left.\frac{\partial f}{\partial x_i}\right|_{\overline{x}} x_i \tag{D.1}$$

where $\overline{x} = \langle \overline{x_1}, \overline{x_2}, ..., \overline{x_n} \rangle$. The variance of function f is given by

$$\sigma^2(f) = \sum_{i}^{n} \sum_{j}^{n} \left.\frac{\partial f}{\partial x_i}\right|_{\overline{x}} \left.\frac{\partial f}{\partial x_j}\right|_{\overline{x}} \sigma(x_i)\sigma(x_j)R_{ij} \tag{D.2}$$

where R_{ij} is the correlation between random variables x_i and x_j. Since $R_{ij} = 1$ when $i = j$, (D.2) can be rewritten as

$$\sigma^2(f) = \sum_{i}^{n} \left(\left.\frac{\partial f}{\partial x_i}\right|_{\overline{x}} \right)^2 \sigma^2(x_i) + \sum_{i}^{n} \sum_{j \neq i}^{n} \left.\frac{\partial f}{\partial x_i}\right|_{\overline{x}} \left.\frac{\partial f}{\partial x_j}\right|_{\overline{x}} \sigma(x_i)\sigma(x_j)R_{ij} \tag{D.3}$$

When random variables x_i and x_j are independent, $R_{ij} = 0$. Thus, (D.3) can be

simplified to

$$\sigma^2(f) = \sum_i^n \left(\frac{\partial f}{\partial x_i}\bigg|_{\overline{x}} \right)^2 \sigma^2(x_i) \tag{D.4}$$

D.2 Pelgrom Models for Mismatch

In his work [47], Pelgrom derived the variance of a parameter P between two rectangular devices, which is expressed by

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2 \tag{D.5}$$

where ΔP is the difference between two devices with equal dimmensions (W and L), A_P is the area proportionality constant for parameter P, S_P is the spacing proportionality constant for parameter P and D is the distance between the two devices. From (D.5), it can be seen that the mismatch between two devices is inversely proportional to device area and proportional to their distance. However, for distances under $1mm$ [68], the term $S_P^2 D^2$ can be neglected.

The model derived by Pelgrom can be employed to observe matching properties between MOS transistors. Many process parameters can suffer from manufacturing imperfections, such as mobility (μ), oxide thickness (t_{ox}), and others. In this work it will be considered a variation on current gain k_p and threshold voltage V_{T0}, to simplify and allow analytic evaluation of mismatch effects on various circuits. However, mismatch is a far more complex problem, and higher precision models were already derived [69].

The Pelgrom equations considered in this work are given by

$$\sigma^2(V_{T0}) = \frac{A_{V_{T0}}^2}{WL} \tag{D.6}$$

$$\sigma^2(k_p) = \frac{A_{k_p}^2}{WL} \tag{D.7}$$

For simplicity, it will be used a relative variance, given by

$$\hat{\sigma}^2(V_{T0}) = \frac{\sigma^2(V_{T0})}{V_{T0}^2} = \frac{\hat{A}_{V_{T0}}^2}{WL} \tag{D.8}$$

$$\hat{\sigma}^2(k_p) = \frac{\sigma^2(k_p)}{k_p^2} = \frac{\hat{A}_{k_p}^2}{WL} \tag{D.9}$$

where the latter term can also appear implicit in $\beta = k_p W/L$. The relationship between them is given by

$$\hat{\sigma}^2(\beta) = \frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(k_p)\left(\frac{W}{L}\right)^2}{k_p^2\left(\frac{W}{L}\right)^2} = \frac{\sigma^2(k_p)}{k_p^2} = \hat{\sigma}^2(k_p) \tag{D.10}$$

Another important issue to address is that Pelgrom modeled the parameter variation between two devices. To find the area proportionality constant for a single transistor, the parameter must be divided by two. Through the next sections, the analysis are made considering a single transistor variation, so the value of A_P will already consider divided by 2.

D.3 Mismatch on a Current Mirror

Consider the simple current mirror presented in Fig. D.1. Both transistors M_a and M_b are implemented, respectively, by N_a and N_b unitary transistors with width W and length L in parallel, where N_a and N_b are integers.

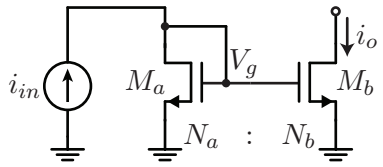


Figure D.1: Simple current mirror circuit.

From the circuit, we have

$$i_{in} = \frac{k_{pa}N_a\frac{W}{L}}{2\alpha}(V_g - V_{T0a})^2 \tag{D.11}$$

$$i_o = \frac{k_{pb}N_b\frac{W}{L}}{2\alpha}(V_g - V_{T0b})^2 \tag{D.12}$$

Applying the propagation of uncertainty on both current equation, we obtain

$$0 = \frac{N_a\frac{W}{L}}{2\alpha}(V_g - V_{T0})^2\Delta k_{pa} + \frac{2k_pN_a\frac{W}{L}}{2\alpha}(V_g - V_{T0})\Delta V_g - \frac{2k_pN_a\frac{W}{L}}{2\alpha}(V_g - V_{T0})\Delta V_{T0a} \tag{D.13}$$

$$\Delta i_o = \frac{N_b\frac{W}{L}}{2\alpha}(V_g - V_{T0})^2\Delta k_{pb} + \frac{2k_pN_b\frac{W}{L}}{2\alpha}(V_g - V_{T0})\Delta V_g - \frac{2k_pN_b\frac{W}{L}}{2\alpha}(V_g - V_{T0})\Delta V_{T0b} \tag{D.14}$$

The above system can be solved for the output current variation Δi_o, by isolating ΔV_g on top equation and applying it on bottom one, leading to

$$\Delta i_o = \frac{N_b\frac{W}{L}}{2\alpha}(V_g - V_{T0})^2\Delta k_{pb} - \frac{N_b\frac{W}{L}}{2\alpha}(V_g - V_{T0})^2\Delta k_{pa} + \frac{k_p N_b\frac{W}{L}}{\alpha}(V_g - V_{T0})\Delta V_{T0a} - \frac{k_p N_b\frac{W}{L}}{\alpha}(V_g - V_{T0})\Delta V_{T0a} \tag{D.15}$$

$$\Delta i_o = \frac{N_b\frac{W}{L}}{2\alpha}(V_g - V_{T0})^2(\Delta k_{pb} - \Delta k_{pa}) + \frac{k_p N_b\frac{W}{L}}{\alpha}(V_g - V_{T0})(\Delta V_{T0a} - \Delta V_{T0b}) \tag{D.16}$$

From the nominal current equation of M_a, we can obtain

$$V_g - V_{T0} = \sqrt{\frac{2\alpha i_{in} L}{k_p N_a W}} \tag{D.17}$$

which can be applied to (D.16), leading to

$$\Delta i_o = \frac{N_b\frac{W}{L}}{2\alpha}\frac{2\alpha i_{in} L}{k_p N_a W}(\Delta k_{pb} - \Delta k_{pa}) + \frac{k_p N_b\frac{W}{L}}{\alpha}\sqrt{\frac{2\alpha i_{in} L}{k_p N_a W}}(\Delta V_{T0a} - \Delta V_{T0b}) \tag{D.18}$$

$$\Delta i_o = \frac{N_b}{N_a}\frac{i_{in}}{k_p}(\Delta k_{pb} - \Delta k_{pa}) + \frac{N_b}{\sqrt{N_a}}\sqrt{\frac{k_p\frac{W}{L}}{\alpha}}\sqrt{2i_{in}}(\Delta V_{T0a} - \Delta V_{T0b}) \tag{D.19}$$

The variance of Δi_o is given by

$$\sigma^2(\Delta i_o) = \left(\frac{N_b}{N_a}\frac{i_{in}}{k_p}\right)^2(\sigma^2(k_{pb}) + \sigma^2(k_{pa})) + \frac{N_b^2}{N_a}\frac{2k_p W i_{in}}{\alpha L}(\sigma^2(V_{T0a}) + \sigma^2(\Delta V_{T0b})) \tag{D.20}$$

and considering $i_o = \frac{N_b}{N_a} i_{in}$, applying the relative variance in (D.20) leads to

$$\frac{N_b^2}{N_a^2} i_{in}^2\hat{\sigma}^2(\Delta i_o) = \left(\frac{N_b}{N_a}\frac{i_{in}}{k_p}\right)^2 k_p^2(\hat{\sigma}^2(k_{pb}) + \hat{\sigma}^2(k_{pa})) + \frac{N_b^2}{N_a}\frac{2k_p W i_{in}}{\alpha L}V_{T0}^2(\hat{\sigma}^2(V_{T0a}) + \hat{\sigma}^2(\Delta V_{T0b})) \tag{D.21}$$

which simplifies to

$$\hat{\sigma}^2(\Delta i_o) = \hat{\sigma}^2(k_{pb}) + \hat{\sigma}^2(k_{pa}) + \frac{2N_a k_p W V_{T0}^2}{i_{in}\alpha L}(\hat{\sigma}^2(V_{T0a}) + \hat{\sigma}^2(\Delta V_{T0b})) \tag{D.22}$$

Pelgrom equations can be applied in (D.22), leading to

$$\hat{\sigma}^2(\Delta i_o) = \frac{\hat{A}_{k_p}^2}{N_a WL} + \frac{\hat{A}_{k_p}^2}{N_b WL} + \frac{2N_a k_p W V_{T0}^2}{i_{in}\alpha L}\left(\frac{\hat{A}_{V_{T0}}^2}{N_a WL} + \frac{\hat{A}_{V_{T0}}^2}{N_a WL}\right) \tag{D.23}$$

$$\hat{\sigma}^2(\Delta i_o) = \frac{\hat{A}_{k_p}^2}{WL}\left(\frac{N_a + N_b}{N_a N_b}\right) + \frac{\hat{A}_{V_{T0}}^2}{WL}\frac{2N_a k_p W V_{T0}^2}{i_{in}\alpha L}\left(\frac{N_a + N_b}{N_a N_b}\right) \tag{D.24}$$

The ratio $R = W/L$ is a constraint for the current mirrors designed throughout this work, so it is applied to (D.24), leading to the final result, expressed by

$$\hat{\sigma}^2(\Delta i_o) = \frac{1}{L^2}\left(\frac{N_a + N_b}{N_b}\right)\left[\hat{A}_{k_p}^2\frac{1}{RN_a} + \hat{A}_{V_{T0}}^2\frac{2k_p V_{T0}^2}{i_{in}\alpha}\right] \tag{D.25}$$

D.4 Differential Pair Transconductance Variation

To obtain the transconductance variation for a differential pair, the transconductance of the pair must be derived. The differential pair is pictured in Fig. D.2.

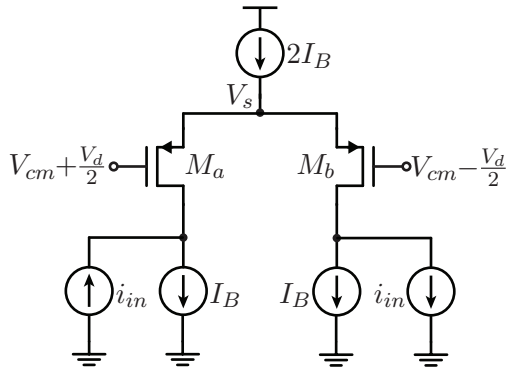


Figure D.2: Differential pair circuit.

The current equations, considering each transistor operating in the saturation region, are given by

$$\sqrt{\frac{2\alpha}{\beta_a}(I_B - i_{in})} = V_s - V_{cm} - \frac{V_d}{2} - V_{Ta} \tag{D.26}$$

$$\sqrt{\frac{2\alpha}{\beta_b}(I_B + i_{in})} = V_s - V_{cm} + \frac{V_d}{2} - V_{Tb} \tag{D.27}$$

and the subtraction of (D.26) from (D.27) leads to

$$\sqrt{\frac{2\alpha}{\beta_a}(I_B + i_{in})} - \sqrt{\frac{2\alpha}{\beta_a}(I_B - i_{in})} = V_d + V_{Ta} - V_{Tb} \tag{D.28}$$

The transconductance is obtained by an implicit differentiation on each side of (D.28) with respect to V_d, which is expressed by

$$\frac{\frac{2\alpha}{\beta_b}}{2\sqrt{\frac{2\alpha}{\beta_b}(I_B+i_{in})}}\frac{di_{in}}{dV_d}+\frac{\frac{2\alpha}{\beta_a}}{2\sqrt{\frac{2\alpha}{\beta_a}(I_B-i_{in})}}\frac{di_{in}}{dV_d}=1 \tag{D.29}$$

The modulation index m_i, defined as the ratio between input current and bias current, i.e. $m_i = i_{in}/I_B$, can be applied to (D.29), leading to

$$\left[\frac{\frac{2\alpha}{\beta_b}}{2\sqrt{\frac{2\alpha I_B}{\beta_b}(1+m_i)}}+\frac{\frac{2\alpha}{\beta_a}}{2\sqrt{\frac{2\alpha I_B}{\beta_a}(1-m_i)}}\right]\frac{di_{in}}{dV_d}=1 \tag{D.30}$$

which after some simplifications and using $gm = di_{in}/dV_d$, we obtain

$$\left[\frac{\sqrt{\frac{\alpha}{\beta_b}}}{\sqrt{2I_B(1+m_i)}}+\frac{\sqrt{\frac{\alpha}{\beta_a}}}{\sqrt{2I_B(1-m_i)}}\right]gm=1 \tag{D.31}$$

where gm can be isolated and expressed by

$$gm(m_i)=\sqrt{\frac{2I_B}{\alpha}}\left[\frac{\sqrt{\beta_a\beta_b}\sqrt{1-m_i^2}}{\sqrt{\beta_b}\sqrt{1+m_i}+\sqrt{\beta_a}\sqrt{1-m_i}}\right] \tag{D.32}$$

The nominal value of the transconductance is given when $\beta_a = \beta_b = \beta$, which leads to

$$gm(m_i)\Big|_{\beta_a=\beta_b=\beta}=\sqrt{\frac{2I_B\beta}{\alpha}}G(m_i) \tag{D.33}$$

where

$$G(m_i)=\frac{\sqrt{1-m_i^2}}{\sqrt{1+m_i}+\sqrt{1-m_i}} \tag{D.34}$$

Applying the propagation of uncertainty, the transconductance variation is expressed as

$$\Delta gm(m_i)=\frac{\partial gm}{\partial\beta_a}\Big|_{\beta_a=\beta_b=\beta}\Delta\beta_a+\frac{\partial gm}{\partial\beta_b}\Big|_{\beta_a=\beta_b=\beta}\Delta\beta_b \tag{D.35}$$

where the partial derivatives are expressed by

$$\frac{\partial gm}{\partial\beta_a}=\frac{\frac{1}{2}\sqrt{\frac{2I_B}{\alpha}}\sqrt{1-m_i^2}\sqrt{1+m_i}\frac{\beta_b}{\sqrt{\beta_a}}}{(\sqrt{\beta_b}\sqrt{1+m_i}+\sqrt{\beta_a}\sqrt{1-m_i})^2} \tag{D.36}$$

and

$$\frac{\partial gm}{\partial \beta_b} = \frac{\frac{1}{2}\sqrt{\frac{2I_B}{\alpha}}\sqrt{1-m_i^2}\sqrt{1-m_i}\frac{\beta_a}{\sqrt{\beta_b}}}{(\sqrt{\beta_b}\sqrt{1+m_i}+\sqrt{\beta_a}\sqrt{1-m_i})^2} \tag{D.37}$$

Applying (D.36) and (D.37) to (D.35) leads to

$$\Delta gm(m_i) = \left[\frac{\frac{1}{2}\sqrt{\frac{2I_B\beta}{\alpha}}\sqrt{1-m_i^2}\sqrt{1+m_i}}{\beta(\sqrt{1+m_i}+\sqrt{1-m_i})^2}\right]\Delta\beta_a + \left[\frac{\frac{1}{2}\sqrt{\frac{2I_B\beta}{\alpha}}\sqrt{1-m_i^2}\sqrt{1-m_i}}{\beta(\sqrt{1+m_i}+\sqrt{1-m_i})^2}\right]\Delta\beta_b \tag{D.38}$$

Assuming the errors are independent random variables, the variance of Δgm is the sum of each error variance. The variance of $\Delta\beta_a$ and $\Delta\beta_b$ are given by

$$\sigma^2(\beta_a) = \sigma^2(\beta_b) = \sigma^2(\beta) = \hat{\sigma}^2(\beta)\cdot\beta^2 \tag{D.39}$$

leading the variance of Δgm to

$$\sigma^2(\Delta gm) = \left[\frac{\frac{I_B\beta}{2\alpha}(1-m_i^2)(1+m_i)}{\beta^2(\sqrt{1+m_i}+\sqrt{1-m_i})^4}\right]\hat{\sigma}^2(\beta)\beta^2 + \left[\frac{\frac{I_B\beta}{2\alpha}(1-m_i^2)(1-m_i)}{\beta^2(\sqrt{1+m_i}+\sqrt{1-m_i})^2}\right]\hat{\sigma}^2(\beta)\beta^2 \tag{D.40}$$

$$\sigma^2(\Delta gm) = \left[\frac{\frac{I_B\beta}{2\alpha}(1-m_i^2)(1+m_i)}{(\sqrt{1+m_i}+\sqrt{1-m_i})^4}\right]\hat{\sigma}^2(\beta) + \left[\frac{\frac{I_B\beta}{2\alpha}(1-m_i^2)(1-m_i)}{(\sqrt{1+m_i}+\sqrt{1-m_i})^2}\right]\hat{\sigma}^2(\beta) \tag{D.41}$$

$$\sigma^2(\Delta gm) = \frac{I_B\beta}{\alpha}\left[\frac{1-m_i^2}{(\sqrt{1+m_i}+\sqrt{1-m_i})^4}\right]\hat{\sigma}^2(\beta) \tag{D.42}$$

The final transconductance variance is a function of m_i, so it depends on the input current value. It can be rewritten as

$$\sigma^2(\Delta gm) = \frac{I_B\beta}{\alpha}F(m_i)\cdot\hat{\sigma}^2(\beta) \tag{D.43}$$

where

$$F(m_i) = \left[\frac{1-m_i^2}{(\sqrt{1+m_i}+\sqrt{1-m_i})^4}\right] \tag{D.44}$$

Using MATLAB to evaluate $F(m_i)$, the curve in Fig. D.3 is obtained. The transconductance variation has its peak value when $m_i = 0$.

For simplicity, the maximum variation will be specified as the transconductance

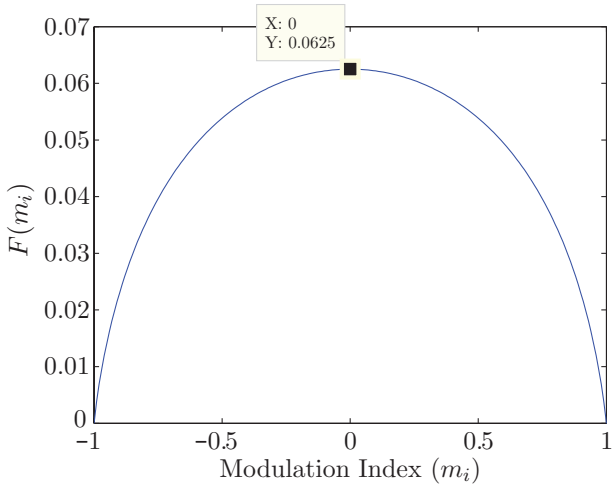


Figure D.3: Plot of $F(m_i)$ vs. modulation index m_i.

variation. Therefore, the final variance is given by

$$\sigma^2(\Delta gm) = \frac{I_B\beta}{16\alpha} \cdot \hat{\sigma}^2(\beta) \tag{D.45}$$

and after applying Pelgrom models is expressed by

$$\sigma^2(\Delta gm) = \frac{1}{L^2}\frac{I_B k_p}{16\alpha} \cdot \hat{A}_{k_p}^2 \tag{D.46}$$

D.5 Differential Pair Input Offset Voltage

For the differential pair pictured in Fig. D.2, when $V_d = 0$, the current i_{in} should be null. However, due to transistor mismatch, a small current offset is observed at the output. This current imbalance can be model by an input offset voltage V_{os} which cancels the current output. To simplify, an differential offset is considered, thus $V_d = V_{os}$. Applying these considerations into the current equations leads to

$$\sqrt{\frac{2\alpha I_B}{\beta_a}} = V_s - V_{cm} - \frac{V_{os}}{2} - V_{Ta} \tag{D.47}$$

$$\sqrt{\frac{2\alpha I_B}{\beta_b}} = V_s - V_{cm} + \frac{V_{os}}{2} - V_{Tb} \tag{D.48}$$

Subtracting (D.47) from (D.48) leads to

$$\sqrt{\frac{2\alpha I_B}{\beta_b}} - \sqrt{\frac{2\alpha I_B}{\beta_a}} = V_{os} - V_{Tb} + V_{Ta} \tag{D.49}$$

which is rearranged into

$$V_{os} = \sqrt{\frac{2\alpha I_B}{\beta_b}} - \sqrt{\frac{2\alpha I_B}{\beta_a}} + V_{Tb} - V_{Ta} \tag{D.50}$$

Applying the propagation of uncertainty, we obtain

$$\Delta V_{os} = \frac{1}{2\sqrt{\frac{2\alpha I_B}{\beta}}}\left(-\frac{2\alpha I_B}{\beta^2}\right)\Delta\beta_b - \frac{1}{2\sqrt{\frac{2\alpha I_B}{\beta}}}\left(-\frac{2\alpha I_B}{\beta^2}\right)\Delta\beta_a + \Delta V_{T0b} - \Delta V_{T0a} \tag{D.51}$$

which is rearranged into

$$\Delta V_{os} = \frac{1}{2\beta}\sqrt{\frac{2\alpha I_B}{\beta}}(\Delta\beta_a - \Delta\beta_b) + \Delta V_{T0b} - \Delta V_{T0a} \tag{D.52}$$

The variance of the offset voltage is given by

$$\sigma^2(\Delta V_{os}) = \frac{1}{4\beta^2}\frac{2\alpha I_B}{\beta}2\beta^2\hat{\sigma}^2(\beta) + 2V_{T0}^2\hat{\sigma}^2(V_{T0}) \tag{D.53}$$

which is simplified to

$$\sigma^2(\Delta V_{os}) = \frac{\alpha I_B}{\beta}\hat{\sigma}^2(\beta) + 2V_{T0}^2\hat{\sigma}^2(V_{T0}) \tag{D.54}$$

Applying Pelgrom rules, and using $R = W/L$, the final result is given by

$$\sigma^2(\Delta V_{os}) = \frac{1}{L^2}\left[\frac{\alpha I_B}{k_p R^2}\cdot\hat{A}_{k_p}^2 + \frac{2V_{T0}^2}{R}\cdot\hat{A}_{V_{T0}}^2\right] \tag{D.55}$$

D.6 Differential Current Mirror Gain Error

The differential current mirror (DCM) was introduced in Chapter 2.3.1, and it is responsible to create two copies of the structurally all-pass section (SAPS) input current. The circuit is composed by two identical differential amplifiers, M_{1a}-M_{1b} and M_{2a}-M_{2b}, with differential inputs connected together. The differential amplifier M_{1a}-M_{1b} have both transistors diode-connected. The input current i_{in} of M_{1a}-M_{1b} determines the input differential voltage, which is the same for M_{2a}-M_{2b}.

To simplify the analysis, the original configuration was slightly changed to a fully symmetric one, in order to reduce the amount of calculation. The resulting circuit is pictured in Fig. D.4.

Let $V_d = V_a - V_b$. For the circuit on Fig. D.4, we have

$$i_{in} = gm_1(m_i)V_d \tag{D.56}$$

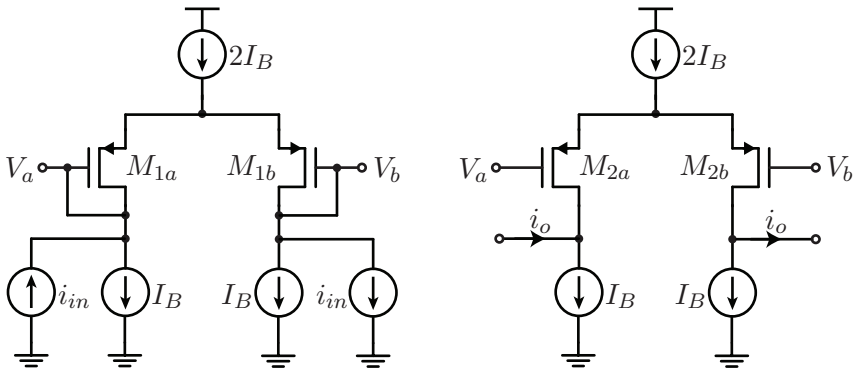


Figure D.4: Differential current mirror circuit.

$$i_o = gm_2(m_i)V_d \tag{D.57}$$

where $gm_1(m_i)$ and $gm_2(m_i)$ are large-signal transconductance and depend on the modulation index m_i, as derived in the last section. Applying (D.56) on (D.57) leads to

$$i_o = \frac{gm_2(m_i)}{gm_1(m_i)} i_{in} \tag{D.58}$$

The transconductance of each pair are different due to mismatch and process parameters variation. However, both large-signal transconductances can be represented by a nominal curve and a variation. Thus, they can be expressed as

$$gm_1(m_i) = gm(m_i) + \Delta gm_1 \tag{D.59}$$

$$gm_2(m_i) = gm(m_i) + \Delta gm_2 \tag{D.60}$$

and be applied to (D.58) to obtain

$$i_o = \frac{gm(m_i) + \Delta gm_2}{gm(m_i) + \Delta gm_1} i_{in} \tag{D.61}$$

Putting the average term in evidence, it leads to

$$i_o = \frac{1 + \dfrac{\Delta gm_2}{gm(m_i)}}{1 + \dfrac{\Delta gm_1}{gm(m_i)}} \cdot i_{in} = \frac{\left(1 + \dfrac{\Delta gm_2}{gm(m_i)}\right)\left(1 - \dfrac{\Delta gm_1}{gm(m_i)}\right)}{1 - \left(\dfrac{\Delta gm_1}{gm(m_i)}\right)^2} \cdot i_{in} \tag{D.62}$$

$$i_o = \frac{1 + \dfrac{\Delta gm_2}{gm(m_i)} - \dfrac{\Delta gm_1}{gm(m_i)} - \dfrac{\Delta gm_1 \Delta gm_2}{gm(m_i)^2}}{1 - \left(\dfrac{\Delta gm_1}{gm(m_i)}\right)^2} \cdot i_{in} \tag{D.63}$$

Since $|\Delta gm| \ll gm,\ \forall\ m_i$, (D.63) can be approximated by

$$A_c = \frac{i_o}{i_{in}} \approx 1 + \frac{\Delta gm_2}{gm(m_i)} - \frac{\Delta gm_1}{gm(m_i)} \tag{D.64}$$

The current gain (A_c) variance is given by

$$\sigma^2(A_c) = \frac{2\sigma^2(\Delta gm)}{(gm(m_i))^2} \tag{D.65}$$

$$\sigma^2(A_c) = \frac{2\frac{I_B\beta}{\alpha}F(m_i)\hat{\sigma}_\beta^2}{\frac{2I_B\beta}{\alpha}G(m_i)^2} = \frac{F(m_i)}{G(m_i)^2}\cdot\hat{\sigma}_\beta^2 \tag{D.66}$$

and the maximum value is given by

$$\sigma^2(A_c) = \frac{1}{2}\cdot\hat{\sigma}^2(\beta) \tag{D.67}$$

After applying Pelgrom models and $R = W/L$, the current gain variance is expressed as

$$\sigma^2(A_c) = \frac{1}{L^2}\frac{1}{2R}\cdot\hat{A}_{k_p}^2 \tag{D.68}$$

D.7 Differential Current Mirror Offset Current

The offset current is observed in the output when the input current is null. Due to mismatch on pair M_{1a}-M_{1b}, an offset voltage appears at the input of the differential pair M_{2a}-M_{2b}, which also contributes with its own offset voltage, leading to an output current given by

$$i_{os} = gm_2(m_i)V_{os1} + gm_2(m_i)V_{os2} \tag{D.69}$$

where gm_2 is the transconductance of pair M_{2a}-M_{2b}. The modulation index m_i is given by i_{os}/I_B, hence

$$i_{os} = gm_2\left(\frac{i_{os}}{I_B}\right)[V_{os1} + V_{os2}] \tag{D.70}$$

Considering a practical circuit, $|i_{os}| \ll I_B$, thus (D.70) can be approximated by

$$i_{os} \approx gm_2(0)[V_{os1} + V_{os2}] \tag{D.71}$$

Applying the propagation of errors, the output offset current variation is given by

$$\Delta i_{os} = \cancel{(V_{os1} + V_{os2})}\Delta gm_2 + gm(0)\Delta V_{os1} + gm(0)\Delta V_{os2} = \sqrt{\frac{I_B\beta}{2\alpha}}\,(\Delta V_{os1} + \Delta V_{os2}) \tag{D.72}$$

The variance of the offset current is given by

$$\sigma^2(\Delta i_{os}) = \frac{I_B\beta}{2\alpha} 2\sigma^2(\Delta V_{os}) \tag{D.73}$$

where $\sigma^2(\Delta V_{os})$ was derived in (D.54), hence

$$\sigma^2(\Delta i_{os}) = I_B^2\hat{\sigma}^2(\beta) + \frac{2I_B\beta V_{T0}^2}{\alpha}\hat{\sigma}^2(V_{T0}) \tag{D.74}$$

Applying Pelgrom models, the final result is expressed as

$$\sigma^2(\Delta i_{os}) = \frac{1}{L^2}\left[\frac{I_B^2}{R}\cdot\hat{A}_{k_p}^2 + \frac{2I_B k_p V_{T0}^2}{\alpha}\cdot\hat{A}_{V_{T0}}^2\right] \tag{D.75}$$