ANALOG INTEGRATED LOCK-IN AMPLIFIER FOR OPTICAL SENSORS

João Alberto de França Ferreira

Dissertação de Mestrado apresentada ao Programa de Pós-graduação em Engenharia Elétrica, COPPE, da Universidade Federal do Rio de Janeiro, como parte dos requisitos necessários à obtenção do título de Mestre em Engenharia Elétrica.

Orientador: Antonio Petraglia

Rio de Janeiro
Setembro de 2016

ANALOG INTEGRATED LOCK-IN AMPLIFIER FOR OPTICAL SENSORS

João Alberto de França Ferreira

DISSERTAÇÃO SUBMETIDA AO CORPO DOCENTE DO INSTITUTO ALBERTO LUIZ COIMBRA DE PÓS-GRADUAÇÃO E PESQUISA DE ENGENHARIA (COPPE) DA UNIVERSIDADE FEDERAL DO RIO DE JANEIRO COMO PARTE DOS REQUISITOS NECESSÁRIOS PARA A OBTENÇÃO DO GRAU DE MESTRE EM CIÊNCIAS EM ENGENHARIA ELÉTRICA.

Examinada por:

Prof. Antonio Petraglia, Ph.D.

Prof. Marcelo Martins Werneck, Ph.D.

Prof. João Carlos Machado, Ph.D.

RIO DE JANEIRO, RJ – BRASIL
SETEMBRO DE 2016

Ferreira, João Alberto de França

Analog Integrated Lock-In Amplifier for Optical Sensors/João Alberto de França Ferreira. – Rio de Janeiro: UFRJ/COPPE, 2016.

XVII, 86 p.: il.; 29, 7cm.

Orientador: Antonio Petraglia

Dissertação (mestrado) – UFRJ/COPPE/Programa de Engenharia Elétrica, 2016.

Referências Bibliográficas: p. 79 – 84.

1. Analog lock-in amplifier. 2. Fiber optic sensor. 3. CMOS analog integrated circuit. 4. Low-voltage low-power integrated sensor system. 5. Transimpedance amplifier (TIA). 6. Operational transconductance amplifier (OTA). I. Petraglia, Antonio. II. Universidade Federal do Rio de Janeiro, COPPE, Programa de Engenharia Elétrica. III. Título.

Acknowledgment

I would like to thank my advisor, professor Antonio Petraglia, for suggesting this work theme, that enabled me to gain expertise and practice in the design of analog integrated circuits, for his support and comprehension.

I would also like to thank all other professors of the PADS laboratory, professors Fernando Antônio Pinto Barúqui, José Gabriel Rodriguez Carneiro Gomes, Carlos Fernando Teodósio Soares and Mariane Petraglia, for the exchanges and support and professors Antonio Carneiro de Mesquita Filho e Antonio Carlos Moreirão de Queiroz, for the classes in interesting topics.

I express my gratitude with all the friends of the PADS laboratory for the friendship and help throughout this time, nominaly, Allan Bides and Luiza, Eduardo Anjos, Fernanda Duarte, Luis Fabián, Genildo Nonato, Odair, Juan Pablo Giron and Ana, Fabio de Lacerda, Thiago Brito, Mauro, Felipe Petraglia, Fellipe Falleiro, Thiago Valentim, Florian Wolf, Humberto Paz, Pedro Riascos, Edgard, Roberto, Francinei, Jorge de La Cruz, Oscar Palacios, Motta, Rafael and Manoel.

I shall mention the generous offer of the IEN (Instituto de Energia Nuclear) that enabled the PADS laboratory students to use its LPKF prototyping machine to manufacture their test boards. The visits to the IEN, the tasks develop there and all the exchanges with Fabio were very motivating.

Resumo da Dissertação apresentada à COPPE/UFRJ como parte dos requisitos necessários para a obtenção do grau de Mestre em Ciências (M.Sc.)

AMPLIFICADOR LOCK-IN ANALÓGICO INTEGRADO PARA SENSORES ÓPTICOS

João Alberto de França Ferreira

Setembro/2016

Orientador: Antonio Petraglia

Programa: Engenharia Elétrica

Este trabalho propõe uma topologia de amplificador lock-in analógico integrado para sensores ópticos. Um protótipo foi desenvolvido visando a sua utilização em um sensor a fibra óptica plástica para a medição do índice de refração de um meio aquoso. O projeto objetivou a integração em silício de todos os componentes do sistema e a geração de um circuito de baixa potência e baixa tensão, de maneira a viabilizar sua utilização em aplicações portáteis. A topologia do amplificador apresenta entradas e saídas diferenciais para mitigar problemas com ruído e interferências. O protótipo foi implementado em uma tecnologia CMOS 0,18 micrômetros. Foi utilizada uma tensão de alimentação unipolar de 1,8 volts. Simulações pós-layout indicam que o sistema pode operar com sinais num intervalo de frequências entre 100 Hz e 2 KHz, é capaz de rejeitar a componente DC da fotocorrente que tenha uma magnitude de até 10 μA e consegue processar com precisão sinais de até 14 μA de amplitude, com um consumo estático de potência de 275 μW.

Abstract of Dissertation presented to COPPE/UFRJ as a partial fulfillment of the requirements for the degree of Master of Science (M.Sc.)

ANALOG INTEGRATED LOCK-IN AMPLIFIER FOR OPTICAL SENSORS

João Alberto de França Ferreira

September/2016

Advisor: Antonio Petraglia

Department: Electrical Engineering

This work proposes a topology for an analog integrated lock-in amplifier for fiber optic sensors. A prototype has been developed for application in a plastic optical fiber sensor for measuring the refractive index in an aqueous medium. The design aimed at the integration of all system components in silicon and the generation of a low power and low voltage circuit, to allow its use in portable applications. The amplifier topology features differential inputs and outputs to mitigate problems with noise and interference. A prototype was implemented in a 0.18 microns CMOS technology. A unipolar power supply of 1.8 volts was used. Post-layout simulations indicate that the system can operate with signals in a frequency range between 100 Hz and 2 kHz, it is able to reject the DC photocurrent component with a magnitude of up to 10 μA and can accurately process signals up to 14 μA of amplitude, with a static power consumption of 275 μW.

Contents

List of Figures

List of Tables

List of symbols

A_c	carrier amplitude, p. 19
$A_m(t)$	amplitude of modulating signal, p. 19
A_r	reference signal amplitude, p. 21
BW_n	noise bandwidth, p. 18
C'_{ox}	gate-oxide capacitance per unit area, p. 17
K	flicker noise process-dependent constant, p. 17
L	transistor channel length, p. 17
R	resistance value, p. 14
R_L	resistive load, p. 12
$S_{i,sh}$	shot noise power spectral density, p. 16
$S_{v,th}$, $S_{i,th}$	thermal noise power spectral density, p. 14
$S_v(f)$, $S_i(f)$	noise power spectral density, p. 12
$S_v^{\frac{1}{2}}(f)$, $S_i^{\frac{1}{2}}(f)$	noise amplitude spectral density, p. 13
T	temperature (in Kelvins), p. 14
T_p	(time) period; suitable averaging time interval, p. 12
V_t	threshold voltage, p. 31
W	transistor channel width, p. 17
$*$	convolution operator, p. 21
$\delta(\omega)$	Dirac delta function, p. 20
γ	white noise parameter, p. 15

$\mathscr{F}\{\cdot\}$	Fourier transform, p. 20
ω_c	carrier frequency, p. 19
$\overline{v_n^2}$, $\overline{i_n^2}$	noise mean square value, p. 12
$\overline{v_x^2}$, $\overline{i_x^2}$	signal mean square value, p. 14
ϕ_c	carrier phase, p. 19
$\phi_m(t)$	phase of modulating signal, p. 19
f_c	noise corner frequency, p. 17
g_m	small-signal transconductance, p. 15
h_{lpf}	low-pass filter impulse response, p. 21
k_{lna}	low noise amplifier gain, p. 21
k_{lpf}	low-pass filter gain, p. 21
$m(t)$	modulating signal, p. 19
$n(t)$	noise signal, p. 21
q	elementary charge ($1.6021766208 \times 10^{-19}\,C$), p. 16
$v_{n,rms}$, $i_{n,rms}$	noise voltage/current root mean square (rms) value, p. 12
$v_n(t)$, $i_n(t)$	noise voltage/current (in the time domain), p. 12
$v_{x,rms}$, $i_{x,rms}$	signal voltage/current root mean square (rms) value, p. 14
k	Boltzmann constant ($1.38064852 \times 10^{-23}\,\frac{J}{K}$), p. 14

List of abbreviations

AC	Alternating current, p. 3
ADC	Analog-to-digital converter, p. 8
APS	Active pixel sensor, p. 2
CAS	Computer algebra system, p. 28
CCD	Charge-coupled device, p. 2
CMOS	Complementary metal-oxide semiconductor, p. 5
CMP	Chemical-mechanical polishing/planarization, p. 47
CMRR	Common-mode rejection ratio, p. 61
DC	Direct current, p. 4
DFT	Discrete Fourier transform, p. 68
DRC	Design rules check, p. 47
DSB-FC	Double side band-full carrier, p. 19
DSB-SC	Double side band-suppressed carrier, p. 19
DSP	Digital signal processor, p. 3
EDA	Electronic design automation, p. 47
EKV	Enz-Krummenacher-Vittoz model, p. 28
FAWG	Function/Arbitrary waveform generator, p. 26
FPGA	Field-programmable gate array, p. 3
I/O	Input/output, p. 55
IC	Integrated circuit, p. 29

LAPS	Light addressable potentiometric sensors, p. 5
LED	Light-emitting diode, p. 2
LIA	Lock-in amplifier, p. 26
LNA	Low noise amplifier, p. 3
LO	Local oscillator, p. 26
LPF	Low-pass filter, p. 27
LVS	Layout versus schematic, p. 47
MIM	Metal-Insulator-Metal capacitor, p. 31
MOSFET	Metal-oxide-semiconductor field-effect transistor, p. 6
MPW	Multi project wafer, p. 31
NMOS	n-channel metal-oxide-semiconductor field-effect transistor, p. 50
OTA	Operational transconductance amplifier, p. 9
PCB	Printed circuit board, p. 76
PDK	Process design kit, p. 58
PLL	Phase-locked loop, p. 6
PMMA	Polymethyl methacrylate, p. 1
PMOS	p-channel metal-oxide-semiconductor field-effect transistor, p. 50
POF	Plastic/polymer optical fiber, p. 4
PSD	Power spectral density, p. 12
PSP	Penn State Phillips MOSFET compact model, p. 58
PSRR	Power-supply rejection ratio, p. 61
RIE	Reactive ion etching, p. 47
SNR	Signal-to-noise ratio, p. 13
THD	Total harmonic distortion, p. 60
TIA	Transimpedance amplifier, p. 26

Chapter 1

Introduction

Fiber optic sensors comprise a technology that has recently emerged in the wake of development and increased use of optical fibers and optoelectronic components in communications and consumer goods. Based on their operation principle, or modulation and demodulation processes, one can distinguish different types of sensors, such as those based on the measurement of the amount of change in luminous intensity, polarization, phase and wavelength of the signal propagating in the fiber due to surrounding environment perturbations [1]. Different types of fibers may be used as sensor elements, such as the traditional glass fiber, and plastic fibers, which are made of polymers, such as the polymethyl methacrylate (PMMA) [2].

Due to the continuous and gradual development of the fibers and optoelectronic devices, reducing manufacturing costs and advantages over conventional electronic sensors, fiber optic sensors are being used more often every day. Among its advantages, stand out [1–3]:

- easy integration into a wide variety of structures;
- inability to conduct electric current;
- immunity to electromagnetic interference;
- reduced mass;
- robustness;
- high sensitivity;
- high bandwidth;
- multiplexing capability (to form sensor networks);
- fitness for remote sensing;

- the capacity of sensing several parameters such as refractive index, position, vibration, strain, displacement, velocity (linear and angular), temperature, humidity, viscosity, pressure, electric current, electric/magnetic field, acoustic signals, corrosion, among others.

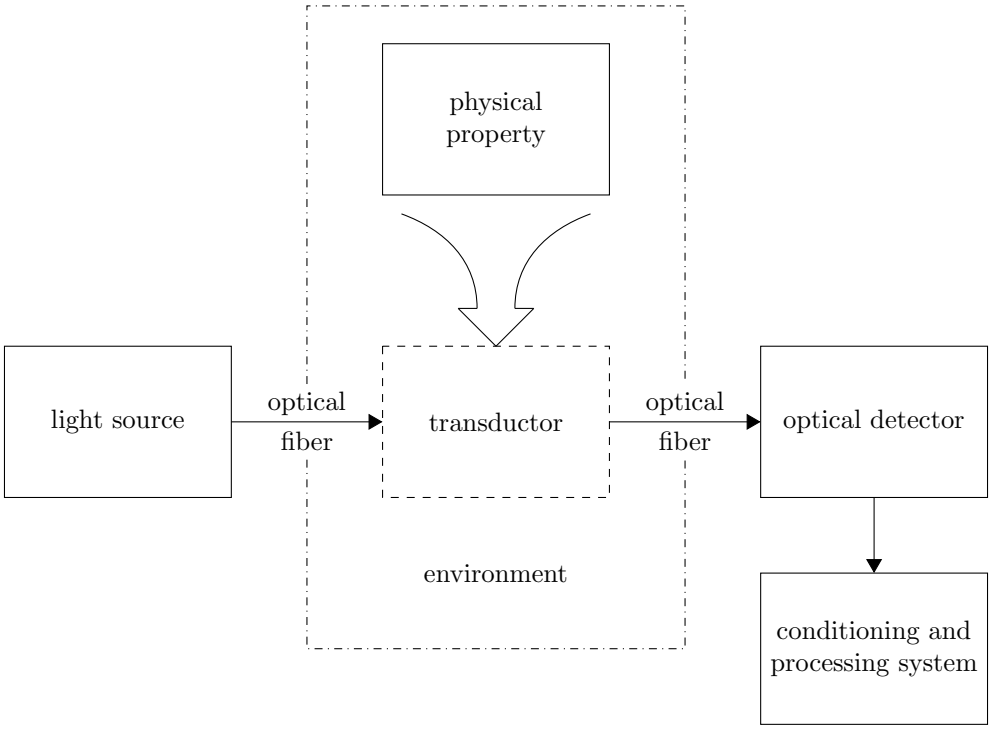


Figure 1.1: Structure of a fiber optic sensor, with a light source to generate an optical reference, an optical fiber and transductor, where the optical reference will be modulated accordingly to a physical property whose magnitude is desired, an optical detector to convert the optical signal to an electrical signal and a conditioning and processing circuit where the signal is demodulated.

The structure of a fiber optic sensor is shown in Figure 1.1. It consists of a light source (laser, LED, laser diode, etc.), optical fiber, optical detector (photodiode, APS, CCD etc.), electronic circuitry for conditioning and processing the signal generated by the detector, and in the case of an extrinsic sensor, a sensor or modulator element (the transducer), which converts a physical quantity (the measurand) into an optical signal.

In the extrinsic type of fiber optic sensor, fiber is simply used to guide the light to the sensor element and from there to the photodetector. In the case of an intrinsic fiber optic sensor, one or more physical properties of the fiber are changed. The external environment acts on the fiber disturbing the light signal that propagates inside it, thereby changing some characteristics of the signal.

1.1 Lock-in amplifier

A characteristic of sensors, in general, is the low amplitude of the generated signal. In certain applications, the signal amplitude gets to be of the same order of magnitude, or even lower, than the noise generated by external sources and by the own electronic circuit. Under these circumstances, the signal-to-noise ratio may display a much lower value than the unit, so that the use of traditional filtering techniques becomes impracticable.

In such situations, and when the sensor signal is an amplitude and/or phase modulated signal of known frequency, a lock-in amplifier can be used to retrieve and amplify it, improving the signal-to-noise ratio.

Commercial lock-in amplifiers are signal recovery instruments widely used in industry, especially in the measurement of chemical and physical variables. They are bulky, heavy and expensive equipment and, roughly speaking, can be seen as simple AC voltmeters. They can be analog or digital (implemented in DSP / FPGA).

Lock-in amplifiers are based on the synchronous detection principle, which is used to highlight the input signal component that has the same frequency and phase of a reference signal, and reject components at other frequencies. This technique reduces the noise bandwidth and extracts a known frequency signal, even if its amplitude is very small.

The block diagram of a two-phase analog lock-in amplifier is shown in Figure 1.2. A lock-in is said two-phase when it has two demodulators, one generating an in-phase component, and the other, a quadrature component. This scheme allows for the estimation of amplitude and phase of the input signal without the need for adjusting the reference signal phase. A single-phase lock-in, on the other hand, has only one demodulator and, therefore, requires a phase adjustment circuit to recover only the amplitude of the input signal.

In the topology shown in Figure 1.2, the low noise amplifier (LNA) amplifies the modulated signal generated by the sensor element. Then, as the frequency of the modulated signal is known, a band-pass filter with a cut-off frequency equal to the signal frequency is used to conduct a "pre-filtering", to reduce the noise bandwidth and weaken external interferences. From there, the synchronous demodulation is developed. The modulated signal is multiplied by a reference signal with the same frequency and phase through the mixer, generating a rectified signal which includes a constant term proportional to the input signal level. Then, this signal is filtered to separate the constant term from the generated high order components. In this demodulation process, all noise and interferences that are not correlated with the reference, that is the common case, average to zero in the final output.

The preceding paragraph describes the working principle of an analog single-

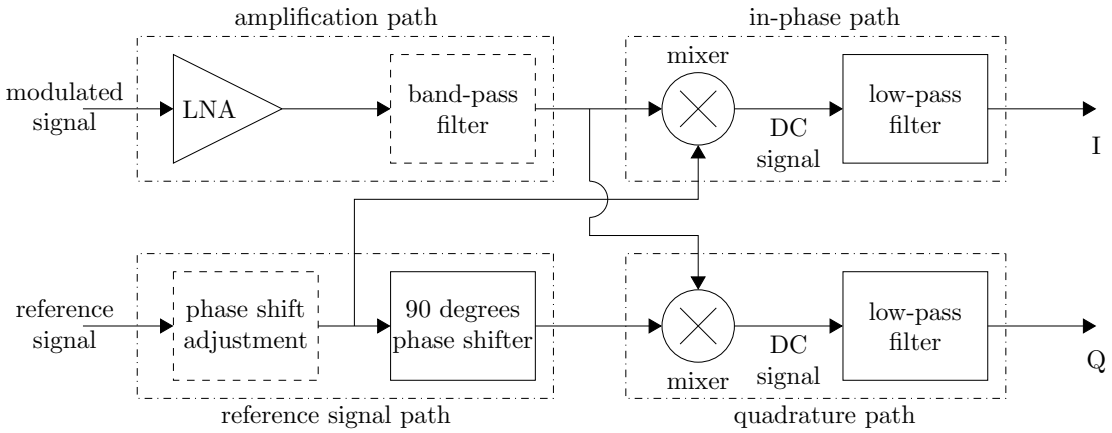


Figure 1.2: Block diagram of an analog two-phase lock-in amplifier (optional components are enclosed in a dashed box) comprising an amplification path, two synchronous demodulators, each one consisting of the in-phase and quadrature channels, and a reference signal path that generates an appropriate reference for the demodulators.

phase lock-in amplifier. In a two-phase lock-in amplifier, a second mixer is used to demodulate the amplified signal by means of a quadrature reference signal. This procedure produces a DC signal whose average value is proportional to the phase difference between the input signal and the reference signal.

Although commercial lock-in amplifiers are widely used in instrumentation laboratories, integrated versions are not easily found for sale. One can read about them only in scientific publications, thereby hampering other applications, especially those requiring portability and low power.

1.2 Motivation and objectives

Taking as starting point the work published in [4], where plastic optical fiber sensors based on amplitude modulation were developed for determining the refraction index of an aqueous medium, the present work strives to propose and develop an analog lock-in amplifier for conditioning the signal generated by the photodetector (photodiode) at the end of the plastic optical fiber (POF).

The relevance of the proposed work can be atested when it is understood as a second step, aggregator and driver, in the transfer of the knowledge gained in academia to society. The first step is the initial research itself ([4]), and the proposed work encourages the transfer of academic knowledge to society by adding other insights and requirements directed to create a commercial product.

The creation of a commercial product is possible if the conditioning and signal processing systems implemented by the data acquisition board and the Matlab/Simulink software in [4], are integrated on silicon. This integration provides,

among other items:

- product customization capabilities
- portability
- mass production capacity
- cost reduction of the final product

The proposed lock-in amplifier topology applies to all sensors based on amplitude modulation and having a photodiode as optical detector. This type of sensor produces a very low signal amplitude. If this signal is in an environment with many interference sources, obtaining the signal by a linear filtering operation may be infeasible. The lock-in amplifier is critical in scenarios such as this, to amplify the signal and improve the signal-to-noise ratio. Obviously, the lock-in amplifier is not limited to fiber optic sensor applications, it can be adapted to any situation where there is a need to recover a signal immersed in noise (even if the noise is much greater than the signal), or simply improve the signal-to-noise ratio.

1.3 Literature review

Several works on the design of analog integrated lock-in amplifiers for use in sensors exist in the literature. Amplifiers have been designed for specific purposes, such as lock-ins for Light Addressable Potentiometric Sensors (LAPS) [5]; for detecting small quantities of gas through a resistive sensor [6–10]; for optical coherence tomography signal detection [11]; for the detection of small amplitude signals in magnetically stimulated mechanical resonators [12, 13]; for hydrogen detection by a sensor based on palladium nanowire [14]; for optical sensors and spectroscopy [15, 16] and for detectors in terahertz imagers [17]. General-purpose lock-in amplifiers have also been developed [18–22]. Among these, single-phase [5–7, 15, 16, 18–21] and two-phase [8–14, 17, 22] systems were designed.

All works have chosen to design their systems in a CMOS technology due to the fact that a large range of element sensor types can be integrated in this kind of technology. This opens up the possibility to create a monolithic sensor system, which consists of the sensing element and conditioning and signal processing circuits, all integrated on a single die. Furthermore, the CMOS manufacturing process of components is well known and already established in the industry. Compared with other technologies, this provides the manufacture of reliable components at a low cost.

Some researches persist for long periods and present, in several articles, the results obtained during different moments. One of these researches began with [5], which had shown a lock-in amplifier manufactured in a 0.6 μm technology, and has evolved by adapting the initial topology and changing certain characteristics such as gain and operating frequency. Thus, discrete prototypes were presented in [6, 8, 9] and integrated ones in [7, 10] to validate the various proposed changes. Other studies published in early articles present just the simulation results and later, in other articles, the experimental results, as in [12, 13] and [19–21]. The work presented in [16] was based on the system topology presented in [15] and was limited to modify the topology of certain blocks, only presenting simulation results.

Most of the studies present systems whose purpose is to condition voltage signals, and just a few are designed to condition current signals [11, 14–16].

In [18], an analog lock-in amplifier with a topology similar to the one in Figure 1.2 was fabricated in a 0.7 μm CMOS technology. An instrumentation amplifier receives the sensor signal that is again amplified and filtered by a MOSFET-C bandpass amplifier with adjustable gain. The bandpass characteristic of the amplifier reduces the noise bandwidth and the influence of external interferences. The mixer, also implemented in a MOSFET-C technique, receives the sinusoidal reference signal generated by a PLL, as in commercial equipment, which generates the reference signal locally from an external clock. To eliminate the high frequency components of the rectified signal generated by the mixer, a low-pass switched-capacitor filter is used, with a variable cutoff frequency through the adjustment of the switching frequency and three control bits. All blocks have differential inputs and outputs. To convert the differential signal output in a single-ended signal, a DC amplifier with offset adjustment is used.

The lock-in amplifier presented in [5] bears similarities with the previous work. Its gain stage also has an instrumentation amplifier at the input, followed by a band-pass G_m-C filter with a selection bit for selecting the filter cut-off frequency (1 or 10 KHz), and by a programmable gain amplifier. The demodulator is implemented by a switched unitary gain amplifier, that alters the gain from positive to negative when the amplitude of the input sine wave turns to be negative. The reference channel receives an external clock and has a circuit for phase adjustment and another that generates a ninety degree phase shift in the clock, to allow the adjustment of the output of the lock-in amplifier (the output must provide zero volts). After adjustment, the phase shift circuit is inhibited and the reference signal has now the same phase as the signal in the gain path. A low-pass second order G_m-C filter follows the mixer.

The work presented in [6] is a continuation of [5]. Regarding the system topology, the amplifier at the output of the gain stage was eliminated. Moreover, the internal

topology of the differential amplifiers, that serve as basic building blocks for the instrumentation amplifier and the mixer, has changed. The operating frequency range of the lock-in amplifier has also changed. Now, the system can work with frequency values of 11 Hz, 17 Hz, and 77 Hz. Three second-order active band-pass filters, each one with a cutoff frequency set for each one of the three frequencies, have been implemented. To cope with such low frequencies for the input signal, the low-pass filter was changed to a fourth-order cascade Gm-C filter with 1.3 mHz cutoff frequency. A discrete prototype that operates at a frequency of 77 Hz was developed and validated.

The above system is again modified in [7]. In this work, the band-pass filter was eliminated from the system and the topology of the amplifiers was changed one more time. The phase adjustment circuit was also modified. In this, as well as in the two previous works, the resistor of the instrumentation amplifier that allows the adjustment of the gain is implemented as a discrete component, external to the integrated circuit, just to allow the adjustment of the gain by changing the resistor. The low-pass filter was changed again. Now, it is implemented by a discrete cascade of four RC cells, with a cutoff frequency of 100 mHz.

In [8, 9] the topology of the previous work changed significantly. The lock-in amplifier has now a topology with several blocks to implement an automatic phase adjustment. The band-pass filter returns to the input path, and the system starts now to feed back the phase adjustment circuit and the ninety degree phase lag block with the system output signals, representing the error in the detection of the amplitude of the input signal and the error in the detection of phase, respectively. The system was again implemented with discrete elements and validated, showing excellent results.

The previous work is complemented by [10], which adds the automatic adjustment capacity of the frequency of the reference signal. An integrated version of the system is presented and the excellent results shown by the discrete prototype are ratified.

In [11], a two-phase lock-in amplifier is designed and manufactured for signal detection in optical coherence tomography systems, with an interferogram signal that has a carrier frequency of 100 kHz and a bandwidth of 5 kHz. The designed system consists of a transimpedance amplifier with differential output, for converting the current signal from the optical detector into a voltage signal. This block is not considered by the authors as pertaining to the lock-in amplifier architecture. The transimpedance amplifier has adjustable gain and rejection capability. A differential gain stage, with differential input and output, amplifies the signal generated by the transimpedance amplifier and feeds the demodulators. These are based on the Gilbert cell and have a differential input and a single-terminated output. Finally,

each demodulator is followed by a third-order Butterworth switched-capacitor filter with a designed cutoff frequency of 5 kHz and adjustable by means of the clock. The clock is generated by a voltage controlled oscillator based on Schmitt triggers. The reference signal is generated externally. The fabricated circuit was validated in the application for which it was designed and demonstrated efficiency.

A lock-in amplifier is developed aiming at magnetically stimulated mechanical resonator applications. Simulation results are presented in [12], while their experimental results are provided in [13]. The system has, in its input signal amplification path, an instrumentation amplifier, followed by a differential second-order G_m-C high-pass filter with external capacitors to allow its adjustment, and a programmable gain stage. The demodulators are implemented through passive N-MOS bridges, and the low-pass filters through second-order passive networks with discrete capacitors, as in the high-pass filter. In this project, the lock-in amplifier is accompanied by a fixed gain amplifier with offset adjustment, a programmable gain amplifier and a $\Delta\Sigma$ analog-to-digital converter (ADC). The reference signal (square) is generated externally. This signal also serves as a reference for a PLL, external to the designed system, that will generate the necessary signal to stimulate the sensor.

In [14] a two-phase lock-in amplifier is designed to detect the signal of the current flowing through a palladium nanowire when stimulated by a sinusoidal signal voltage. To this end, it presents in its amplification path a current-voltage converter at its entrance, followed by a second-order switched-capacitor band-pass filter. The demodulators have a particular topology, consisting of a thermometric code generator, followed by control switches and an analog adder. The second-order switched-capacitor low-pass filters provide a DC signal at the output of the in-phase and quadrature signal paths which represent, respectively, a value proportional to the amplitude of the current signal (or voltage) generated by the nanowire and a value proportional to the amount of phase error between the reference signal and the input signal voltage.

In [15], the authors developed a lock-in amplifier for optic applications and spectroscopy with operating frequency range from 13 to 25 kHz. The system topology is similar to the one presented in [14] and the differences are in the fact that the amplifier developed in [14] has a two-phase topology, while the one developed in [15] has a single-phase topology. Moreover, high-pass filters follow the transimpedance amplifier and the band-pass filter in order to eliminate the DC component of the signal generated by both blocks. In this paper, also, the signal of the amplifying path, after being amplified, is used as a reference for a PLL, which will generate the local reference signal having the same phase and frequency of the signal generated by the sensor. The filters are all second-order G_m-C and the mixer is based on a Gilbert cell. In the PLL, the voltage controlled oscillator is based on a ring oscillator

and the second-order loop filter is composed of discrete components, external to the integrated circuit.

The same authors developed in [22] an integrated lock-in amplifier for operating frequencies ranging between 15 and 20 MHz. The introduced topology is quite different from the traditional one, becoming a mixed-signal system with analog and digital blocks. The designed system was able to track the input signal amplitude and phase.

In [19–21] an analog integrated single-phase lock-in amplifier, for applications that require portability, was developed using an unconventional strategy. The voltage signal from the sensor element is converted into a current signal by means of a transcondutor, and synchronous demodulation is performed by a mixer that operates in current mode. A current splitter block provides gain adjustment capability through three bits. Finally, the current signal is converted into a voltage one by a transimpedance amplifier and the converted signal is filtered by a passive discrete RC filter (external to the integrated circuit), with a 5 Hz cutoff frequency.

The manufactured system was characterized and used in a practical test where the objective was to detect a small concentration of carbon monoxide mixed with a mass of nitrogen. Compared to other studies, the lock-in amplifier showed excellent electrical characteristics, despite not having integrated the output low-pass filter, nor the OTA bandwidth adjustment capacitors. There was no circuit for generating an internal reference signal to the demodulator. The reference signals were generated externally, by bench function generators. In the practical experiment, the designed lock-in amplifier was able to detect carbon monoxide concentrations in the order of units of ppms.

A lock-in amplifier was designed and presented in [17] to condition signals from terahertz detectors. The long-term goal of the project is to integrate the circuit along with terahertz imagers. The system comprises a low noise amplifier followed by four mixers, each one receiving the amplified signal and the reference signal lagged by, respectively, 0°, 90°, 180° and 270°. The delayed signals are generated by a specific circuit, driven by an external clock. The DC signal at the output of demodulators that receive the reference signals lagged 0° and 180°, feed a differential amplifier, whose goal is to eliminate the offset of the previous blocks. The signal generated by this differential amplifier is said in-phase and passes through a low-pass filter to eliminate high-frequency signal components and obtain a DC value proportional to the amplitude of the input signal. For the generation of the quadrature signal, proportional to the phase difference between the input signal and the reference signal, the same scheme is applied, using for this purpose the DC signal at the output of the other two demodulators.

Chapter 2

System Level Analysis

Lock-in systems are signal recovery instruments that are generally used to carry out measurements in situations where signals of interest are overshadowed by noise and interferences.

There are several techniques for signal recovery, such as the ones based on linear filtering operations, waveform averaging and signal correlation. But, the one that proved most successful was that based on the synchronous detection principle, the lock-in amplifier.

A synchronous detector measures variations in a signal of interest by using a synchronous reference, that can be derived from the input modulator. It shall be find that detection with respect to a synchronous reference enables the use of very long averaging times for the purpose of signal-to-noise ratio (SNR) improvement and that practical systems are capable of operating with signals well below the background noise level.

Synchronous detectors offer a significant advance over alternative amplitude-demodulation schemes employing non-linear devices such as envelope detectors. The latter make no fundamental distinction between signal and noise components, whereas a synchronous detector is engineered to respond specifically to the information-bearing signal.

A synchronous detector is responsive to the amplitude of a signal but is also sensitive to the phase difference between a signal and the reference. Therefore, it can be devised to measure variations in both the amplitude and phase of periodic signals in the presence of noise and interference.

A lock-in system is that one operating on the synchronous detector principle and a lock-in amplifier is a lock-in system that encompasses a synchronous detector, preamplifiers and a reference processing circuit.

In general, applications can be divided into two main categories: the one where lock-in systems are used in their long-established role as signal-recovery tools for the measurement of modulated signal in noise; and the other, where lock-in systems are

used for the precision measurement of signals, in situations where signal-recovery capability does not appear to be a prime consideration. The application aimed by this work is better classified in the second category. Appendix 1 of [23] presents an almost exhaustive list of areas where lock-in amplifiers can be employed.

In the case of an optic fiber sensor, considering that the process is essentially linear, that is, no new frequencies are generated between input and output, the signal of interest appears in the output of the transducer with the same frequency as the fundamental excitation frequency.

The measurement of the phase-shift introduced by the experiment might be of interest, but, very often, it is sufficient to only monitor changes in the magnitude of the output signal.

In the envisaged application, the objective is to determine the concentration of bacteria in water through the measurement of refractive index of the liquid by a plastic optical fiber (POF) sensor. The modulated signal output by the transducer (photodiode) conveys a modulating signal that is slowly varying, not just with respect to the excitation frequency, but also with respect to observation interval. Indeed, in many circumstances the signal may have fixed characteristics throughout the time available for measurement.

In this chapter, some important concepts on signals and noise in the time and frequency domains are briefly revised, the basic theory that underlies the lock-in amplifier operation is introduced, the proposed lock-in amplifier system level architecture is presented and, finally, comments about the employed circuit sizing methodology are made.

2.1 Considerations on signals and noise

A distinction between interference sources of external origin and noise, which is inherent to the measurement system, is usually made. Interference occurs if the received energy transferred through an unintended coupling path causes the circuit to behave in an undesired manner, provided the received energy is of sufficient magnitude and/or spectral content. The means to mitigate external interferences are: (1) suppress the emission at its source; (2) make the coupling path as inefficient as possible; and (3) make the circuit less susceptible to coupled energy [24]. In its turn, the intrinsic circuit noise is analyzed and worked during design.

2.1.1 Noise

Time domain

As noise is a random process, the instantaneous value of noise in the time domain cannot be predicted at any time even if the past values are known. So, to take into account noise on system modeling, it is usual to use the noise mean square value, sometimes referred as average normalized noise power, according to Equations 2.1 and 2.2, or its root mean square value, according to Equations 2.3 and 2.4, as a statistical model for the noise [25, 26],

$$\overline{v_n^2} = \lim_{T_p \to +\infty} \frac{1}{T_p} \int_0^{T_p} v_n^2(t)\, dt \qquad \left[V^2\right] \tag{2.1}$$

$$\overline{i_n^2} = \lim_{T_p \to +\infty} \frac{1}{T_p} \int_0^{T_p} i_n^2(t)\, dt \qquad \left[A^2\right] \tag{2.2}$$

$$v_{n,rms} = \sqrt{\lim_{T_p \to +\infty} \frac{1}{T_p} \int_0^{T_p} v_n^2(t)\, dt} \qquad [V] \tag{2.3}$$

$$i_{n,rms} = \sqrt{\lim_{T_p \to +\infty} \frac{1}{T_p} \int_0^{T_p} i_n^2(t)\, dt} \qquad [A] \tag{2.4}$$

where v_n is a noise voltage and i_n a noise current.

Knowing the noise mean square value, one can readily calculate the actual power delivered to a load R_L as $\frac{\overline{v_n^2}}{R_L}$ or $\overline{i_n^2} R_L$.

Frequency domain

In practice, noise power measurements are used in systems with well-defined impedance levels. Elsewhere, it is generally more convenient to use the concept of power spectral density (PSD) of the noise signal. The PSD shows the power the signal carries at each frequency. More specifically, it is defined as the average power carried by a noise signal in a 1 Hertz bandwidth around a frequency f. The PSD is expressed in units of $\frac{V^2}{Hz}$ and $\frac{A^2}{Hz}$. An example of the typical characteristic of the PSD of a signal is shown in Figure 2.1.

The noise corner frequency f_c delimits two regions in the plot. At low frequencies, the noise is dominated by flicker noise, whereas at higher frequencies, broadband noise dominates.

It is also common to work with the square root of the noise power spectral density.

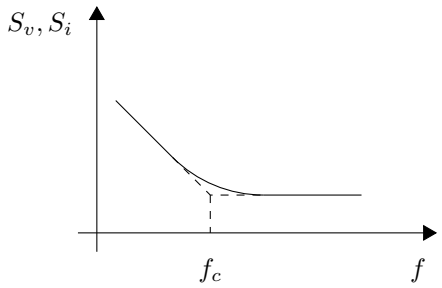


Figure 2.1: Example of the PSD of a voltage ($S_v(f)$) and current ($S_i(f)$) signals, showing the dominance of flicker noise at frequencies below the corner frequency f_c, and the dominance of thermal noise at frequencies above f_c.

This value is termed the amplitude spectral density, or root spectral density, and is expressed in units of $\frac{V}{\sqrt{Hz}}$ and $\frac{A}{\sqrt{Hz}}$, as shown in Figure 2.2.

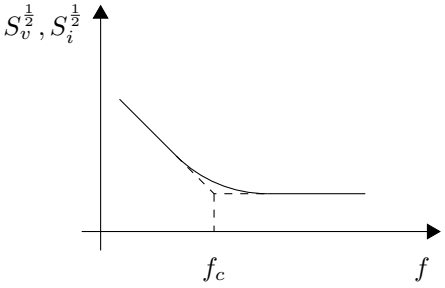


Figure 2.2: Example of the amplitude spectral density of a voltage ($S_v^{\frac{1}{2}}(f)$) and current ($S_i^{\frac{1}{2}}(f)$) signals demonstrating the dominance of flicker noise at frequencies below the corner frequency f_c, and the dominance of thermal noise at frequencies above f_c.

The root mean square value of the noise signal can also be obtained in the frequency domain by

$$v_{n,rms} = \sqrt{\int_0^{+\infty} S_v(f)\ df} \qquad [V] \tag{2.5}$$

$$i_{n,rms} = \sqrt{\int_0^{+\infty} S_i(f)\ df} \qquad [A] \tag{2.6}$$

In practice, the root mean square noise within a specified frequency range can be computed by taking the extremes of the frequency interval as integration limits.

2.1.2 Signal-to-noise ratio

Knowing how to obtain the mean square value of noise, the signal-to-noise ratio (SNR) of a node in a system can be now defined as [26]

$$SNR = \frac{\text{signal power}}{\text{noise power}} \tag{2.7}$$

or in decibels (dB) as

$$SNR = 10\log\left(\frac{\overline{v_x^2}}{\overline{v_n^2}}\right) = 20\log\left(\frac{v_{x,rms}}{v_{n,rms}}\right) \qquad [dB] \tag{2.8}$$

$$SNR = 10\log\left(\frac{\overline{i_x^2}}{\overline{i_n^2}}\right) = 20\log\left(\frac{i_{x,rms}}{i_{n,rms}}\right) \qquad [dB] \tag{2.9}$$

where $\overline{v_x^2}$ and $\overline{i_x^2}$ are the signal mean square values and $v_{x,rms}$ and $i_{x,rms}$ the root mean square values.

2.1.3 Broadband noise

Broadband noise (or white noise) is known to have a constant power spectral density over all the frequency spectrum or, in practice, over the frequency range of interest.

Thermal noise

In semiconductors, a major source of noise is thermal noise (also known as Johnson noise or Nyquist noise). It is generated by the random motion of electrons in a resistive material and in a temperature other than the absolute zero.

For a resistor, the thermal noise can be modelled by a voltage source $S_{v,th}$ with a convenient arbitrated polarity in series with the noiseless resistor, or by a current source $S_{i,th}$ in parallel with the noiseless resistor, as shown in Figure 2.3. The one-sided power spectral density[1] is found to be given by

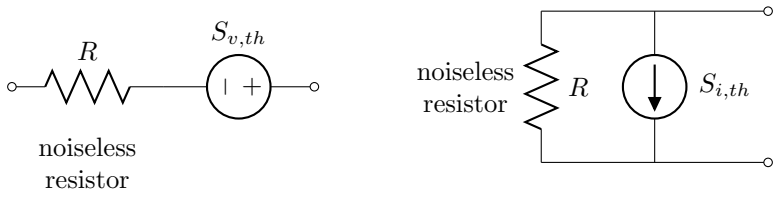
$$S_{v,th} = 4kTR \qquad \left[\frac{V^2}{Hz}\right] \tag{2.10}$$

$$S_{i,th} = \frac{4kT}{R} \qquad \left[\frac{A^2}{Hz}\right] \tag{2.11}$$

where $k = 1.38064852 \times 10^{-23}$ J/K is the Boltzmann constant, T the temperature in Kelvins and R the resistance value. For the models to hold equivalence, $\frac{S_{v,th}}{R^2} = S_{i,th}$.

For a MOSFET, the modeling of thermal noise is a tough matter as the noise varies with the operating region of the transistor, and an all-region equation invari-

[1] In the one-sided spectral density, f is constrained to the interval $[0; +\infty[$, while in the two-sided spectral density, f is constrained to the interval $]-\infty; +\infty[$.



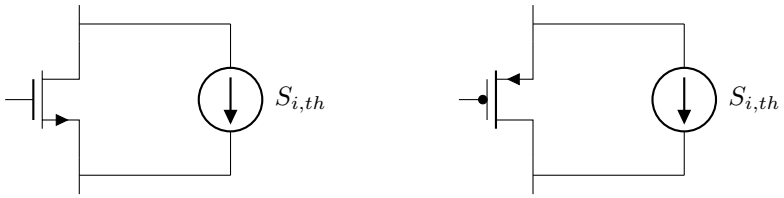
(a) (b)

Figure 2.3: Models for a noisy resistor.

ably results in a complex expression. But, for the common case of a long-channel device operating in strong inversion and in saturation, it is generally accepted to model the noise generated in the channel of the MOSFET by a current source connected between the drain and source terminals (shown in Figure 2.4) with a power spectral density [26]

$$S_{i,th} = 4kT\gamma g_m \qquad \left[\frac{A^2}{Hz}\right] \tag{2.12}$$

where g_m is the device small-signal transconductance, and the white noise parameter γ is assumed to be equal to $\frac{2}{3}$ for a long-channel transistor and may need to be replaced by a larger value for submicron devices.



(a) (b)

Figure 2.4: Model of a noisy (a) nmos transistor; (b) pmos transistor.

Shot noise

Shot noise is associated with a DC flow produced by carriers crossing a potential barrier and is attributed to the passage of discrete charge carriers. Carriers can cross the barrier provided they have sufficient energy to do so; some carriers cross, and some do not. The large numbers of carriers that do cross, each carrying a charge of magnitude q, generates an average current I_{DC}. On top of this is superimposed a minute fluctuation due to the randomness in the flow of individual charge carriers over the barrier. For this reason, shot noise have a power spectral density [27]

$$S_{i,sh} = 2qI_{DC} \qquad \left[\frac{A^2}{Hz}\right] \tag{2.13}$$

where q is the elementary charge ($1.6021766208 \times 10^{-19}\,C$) and I_{DC}, as mentioned before, is the average current.

Shot noise will be present in all semiconductor devices operating with finite bias current, and is usually the dominant source of broadband noise in optical detectors [23]. Here, a periodic current variation due to a variable intensity light beam must often be measured against a more or less steady bias current which flows in response to a much greater "background" illumination due to light leakage. Many such detectors conform closely to an ideal current source, and the output can be measured by connecting the detector to an external load resistor R_L. Figure 2.5 gives the noise equivalent circuit of this arrangement, which shows that the signal current i_s appears in competition with the shot noise current i_{sh} of the bias current I_{DC} and the thermal noise current i_{th} of the load resistor.

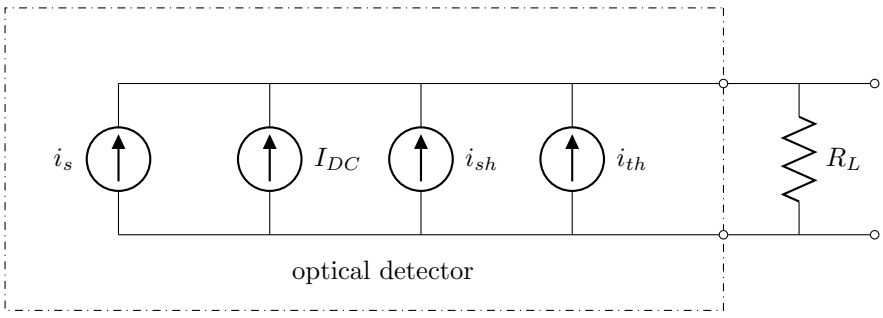


Figure 2.5: Noise equivalent circuit of an optical detector and its various components: i_s - signal current, I_{DC} - bias current, i_{sh} - shot noise current and i_{th} - thermal noise current.

To ensure that the signal-to-noise ratio inherent to the detector is not degraded further by the thermal noise in R_L, the following condition can be investigated:

$$2qI_{DC} \geqslant \frac{4kT}{R_L} \tag{2.14}$$

which gives

$$R_L \geqslant \frac{2kT}{qI_{DC}} \tag{2.15}$$

2.1.4 Low-frequency noise

Flicker noise

A significant type of low-frequency noise is flicker noise, also known as $\frac{1}{f}$ noise or pink noise, that with thermal noise constitute the two types of dominant noise in MOSFETs. Flicker noise is attributed primarily to: (1) the trapping and releasing of charge carriers that move near the gate oxide and silicon substrate interface, due

to extra energy states that exist in this interface; (2) to mobility fluctuations, due to lattice scattering [27].

The flicker noise is usually modelled by a voltage source in series with the gate with power spectral density given by

$$S_{v,fl} = \frac{K}{C'_{ox}WLf} \qquad \left[\frac{V^2}{Hz}\right] \tag{2.16}$$

where K is a process-dependent constant, C_{ox} is the gate-oxide capacitance per unit area, W and L are, respectively, the transistor channel width and length, and f is the operating frequency.

When both, flicker noise and thermal noise are ploted in the same graph, the flicker noise corner (f_c) can be perceived in the intersection between the curves (refer to Figures 2.1 and 2.2). This point can be roughly determined by equaling the noises after transforming the gate noise source in an equivalent channel current source, as [25]

$$4kT\left(\frac{2}{3}\right)g_m = \frac{K}{C'_{ox}WLf_c}g_m^2 \tag{2.17}$$

that is,

$$f_c = \frac{3Kg_m}{8kTC'_{ox}WL} \qquad [Hz] \tag{2.18}$$

2.2 Filtered noise and noise bandwidth

The bandwidth of the noise that appears together with the signal at the output of the transducer, is always fixed at a well defined value due to the low-pass filter effect caused by the capacitance of the transducer and the input resistance of the circuit that follows, generally a high input impedance LNA.

If the low-pass characteristic of the transducer/LNA combination can be expressed by a transfer function $H(j\omega)$, the output spectral density of the noise is expressed by

$$S_{v,out} = S_{v,in}|H(j\omega)|^2 \qquad \left[\frac{V^2}{Hz}\right] \tag{2.19}$$

$$S_{i,out} = S_{i,in}|H(j\omega)|^2 \qquad \left[\frac{A^2}{Hz}\right] \tag{2.20}$$

The root spectral densities can be obtained by taking the square root of both sides in 2.19 and 2.20.

$$S_{v,out}^{\frac{1}{2}} = S_{v,in}^{\frac{1}{2}}|H(j\omega)| \qquad \left[\frac{V}{\sqrt{Hz}}\right] \tag{2.21}$$

$$S_{i,out}^{\frac{1}{2}} = S_{i,in}^{\frac{1}{2}} |H(j\omega)| \qquad \left[\frac{A}{\sqrt{Hz}}\right] \tag{2.22}$$

To calculate the total output mean square value, Equations 2.19 and 2.20 are integrated over the entire spectrum, that is,

$$\overline{v_n^2} = \int_0^{+\infty} S_{v,in} |H(j\omega)|^2 \, df \qquad \left[V^2\right] \tag{2.23}$$

$$\overline{i_n^2} = \int_0^{+\infty} S_{i,in} |H(j\omega)|^2 \, df \qquad \left[A^2\right] \tag{2.24}$$

As previously mentioned, the average power spectral density is determined by the noise power within a 1-Hz bandwidth. This 1-Hz bandwidth is thought of as an ideal band-pass filter with a gain of 1 and a steep characteristic. However, practical filters have a more smooth characteristic. To account for this fact, the noise equivalent bandwidth BW_n (or, simply, noise bandwidth) of a given filter is defined as the bandwidth of an ideal filter that has the same RMS output noise as that of the given filter when white noise is applied to both filters, assuming the same gain for both filters. In other words, given a filter frequency response with peak gain A_0, the noise bandwidth is the width of the ideal filter that has the same area and gain, A_0, as that of the original filter (Figure 2.6).

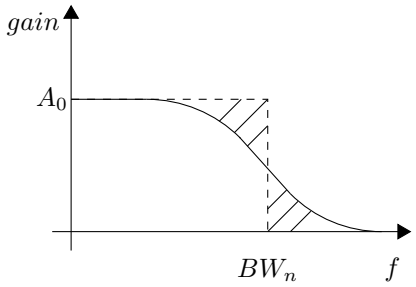


Figure 2.6: Noise bandwidth BW_n and its comparison to the bandwidth of a practical filter.

The advantage of knowing the noise bandwidth of a filter is that when white noise is applied to the filter input, the total output noise mean square value is easily calculated by multiplying the average power spectral density by the noise bandwidth as

$$\overline{v_n^2} = S_{v,out} BW_n \, df \qquad \left[V^2\right] \tag{2.25}$$

$$\overline{i_n^2} = S_{i,out} BW_n \, df \qquad \left[A^2\right] \tag{2.26}$$

2.3 Signal spectrum and modulation

In lock-in measurements, the signal is usually amplitude- and/or phase-modulated, and therefore a previous knowledge of at least the sketch of the signal is necessary.

Considering a carrier wave

$$c(t) = A_c \cos(\omega_c t + \phi_c) \tag{2.27}$$

where A_c is the carrier amplitude, ω_c the carrier frequency and ϕ_c the carrier phase with respect to an arbitrated reference, an amplitude-modulated signal is described by:

$$\begin{aligned} s_{am}(t) &= [1 + m(t)]\, c(t) \\ &= A_c [1 + m(t)] \cos(\omega_c t + \phi_c) \\ &= A_c \cos(\omega_c t + \phi_c) + A_c m(t) \cos(\omega_c t + \phi_c) \end{aligned} \tag{2.28}$$

while a phase-modulated signal is given by:

$$\begin{aligned} s_{pm}(t) &= A_c \cos[\omega_c t + m(t)] \\ &= A_c [\cos(\omega_c t) \cos(m(t)) - \sin(\omega_c t) \sin(m(t))] \end{aligned} \tag{2.29}$$

where $m(t)$ is the modulating signal that should be retrieved.

More precisely, Equation 2.28 represents the double side band-full carrier (DSB-FC) method, where the pure carrier signal is summed to the modulated signal. This is in contrast with the double side band-suppressed carrier (DSB-SC) method, where the carrier is suppressed from the modulated signal.

It is assumed that $m(t)$ has a smaller changing rate than $\cos(\omega_c t)$. Indeed, the modulating signal can be very slowly varying, often having a bandwidth in the order of a few Hertz, that is, an extremely narrowband signal.

Yet, a signal modulated both in amplitude and phase (mixed modulation) is represented by:

$$s_{mm}(t) = A_c [1 + A_m(t)] \cos[\omega_c t + \phi_m(t)] \tag{2.30}$$

where $A_m(t)$ and $\phi_m(t)$ are, respectively, the amplitude and phase of modulating signal.

It is generally easier to study the signals in the frequency domain. For such end one can resort to Fourier series and transforms as well to trigonometric identities to operate with the well-defined sinusoidal carriers.

To obtain the signal spectrum of the amplitude modulated signal (e.g. Fig-

ure 2.7), the Fourier transform is applied:

$$\begin{aligned}\mathscr{F}\{s(t)\} &= S(j\omega) \\ &= \frac{A_c}{2}\delta(\omega-\omega_c)+\frac{A_c}{2}\delta(\omega+\omega_c)+\frac{A_c}{2}M(j\omega+j\omega_c)+\frac{A_c}{2}M(j\omega-j\omega_c)\end{aligned} \tag{2.31}$$

The spectrum generally provides sufficient knowledge about the bandwidth of the

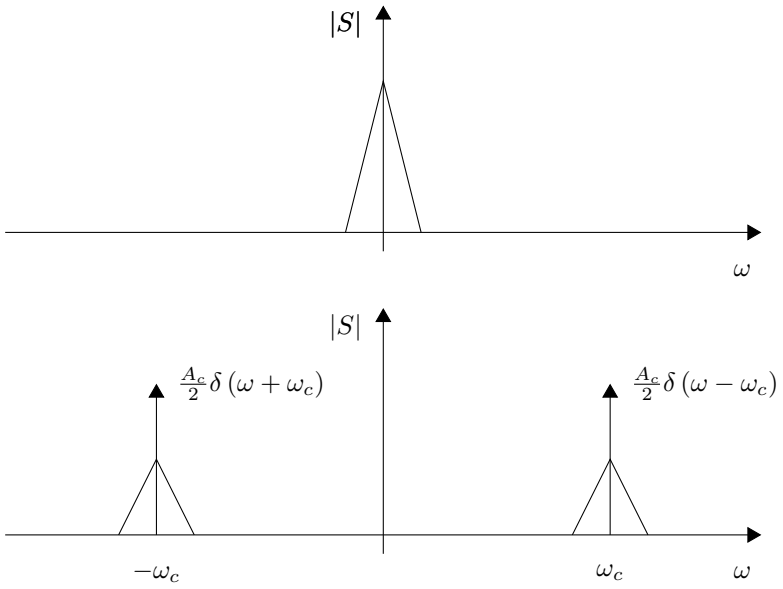


Figure 2.7: Spectrum magnitude of signal $m(t)$ (above) and the the spectrum of the same signal modulated by a sinusoidal carrier of frequency ω_0 and amplitude A_c (below).

modulating signal and its location along all the frequency spectrum.

In regard to phase modulation, for low-index modulation, that is, when the phase shift is very small ($|\sin(t)| \ll 1$), the phase modulated signal can be approximated by:

$$\begin{aligned}s_{pm}(t) &\cong A_c[\cos(\omega_c t)-m(t)\sin(\omega_c t)] \\ &\cong A_c\cos(\omega_c t)-A_c m(t)\sin(\omega_c t)\end{aligned} \tag{2.32}$$

The above expression indicates that for small values of phase shift, the resulting phase modulation amplitude spectrum is identical to that of amplitude modulation.

2.4 Fundamentals of lock-in systems

For the lock-in system depicted in Figure 1.2, its operation can be modeled by considering an amplitude modulated signal with added noise at its input,

$$s_{am}(t) = A_c[1 + m(t)]\cos(\omega_c t + \phi_c) + n(t). \tag{2.33}$$

At the output of the LNA, the signal finds itself amplified by a gain factor k_{lna}, as shown in

$$s'_{am}(t) = k_{lna}\{A_c[1 + m(t)]\cos(\omega_c t + \phi_c) + n(t)\}. \tag{2.34}$$

The synchronous demodulation starts by multiplying the amplified signal by a reference, that can be the own excitation signal. The mixer response in the in-phase channel is given by

$$\begin{aligned} s''_{am,i}(t) &= s'_{am}(t)\, r_i(t) \\ &= k_{lna}\{A_c[1 + m(t)]\cos(\omega_c t + \phi_c) + n(t)\} A_r \cos(\omega_r t + \phi_r) \\ &= A_c A_r k_{lna}[1 + m(t)]\cos(\omega_c t + \phi_c)\cos(\omega_r t + \phi_r) + A_r k_{lna} n(t)\cos(\omega_r t + \phi_r) \\ &= \frac{1}{2} A_c A_r k_{lna}[1 + m(t)]\{\cos[(\omega_c - \omega_r)t + \phi_c - \phi_r] + \cos[(\omega_c + \omega_r)t + \phi_c + \phi_r]\} \\ &+ A_r k_{lna} n(t)\cos(\omega_r t + \phi_r). \end{aligned} \tag{2.35}$$

When $r_i(t)$ is synchronized with s'_{am}, that is, $\omega_c = \omega_r$ and $\phi_c = \phi_r = 0$, the output of the mixer results in

$$\begin{aligned} s''_{am,i}(t) &= \frac{1}{2} A_c A_r k_{lna}[1 + m(t)][1 + \cos(2\omega_r t)] + A_r k_{lna} n(t)\cos(\omega_r t) \\ &= \frac{1}{2} A_c A_r k_{lna}[1 + m(t)] + \frac{1}{2} A_c A_r k_{lna}[1 + m(t)]\cos(2\omega_r t) \\ &+ A_r k_{lna} n(t)\cos(\omega_r t). \end{aligned} \tag{2.36}$$

To complete demodulation, and obtain a constant component that is proportional to the input signal amplitude, the resulting signal is filtered to eliminate the high order components

$$\begin{aligned} out_i &= s''_{am,i}(t) * h_{lpf}(t) \\ &\cong \frac{1}{2} A_c A_r k_{lna} k_{lpf}[1 + m(t)] \\ &\cong \frac{1}{2} A_c A_r k_{lna} k_{lpf} + \frac{1}{2} A_c A_r k_{lna} k_{lpf} m(t). \end{aligned} \tag{2.37}$$

Where h_{lpf} is the low-pass filter impulse response, k_{lpf} the filter gain and "$*$" the convolution operator.

It is assumed that the cut-off frequency of the low-pass filter is much lower than $\omega_c = \omega_r$, so it can significantly attenuate the high-order components.

In equation 2.37, the first term is due to the carrier present in the modulated signal. The second, is the desired response proportional to the input signal. The response of the in-phase demodulator for an amplitude modulated signal without an added carrier will only have the second term.

The quadrature channel receives the reference signal delayed by 90°, so the multiplier response will be

$$\begin{aligned} s''_{am,q}(t) &= s'_{am}(t)\, r_q(t) \\ &= k_{lna}\left\{A_c\left[1+m(t)\right]\cos\left(\omega_c t+\phi_c\right)+n(t)\right\} A_r \sin\left(\omega_r t+\phi_r\right) \\ &= A_c A_r k_{lna}\left[1+m(t)\right]\cos\left(\omega_c t+\phi_c\right)\sin\left(\omega_r t+\phi_r\right)+A_r k_{lna} n(t)\sin\left(\omega_r t+\phi_r\right) \\ &= \frac{1}{2}A_c A_r k_{lna}\left[1+m(t)\right]\left\{\sin\left[\left(\omega_c+\omega_r\right)t+\phi_c+\phi_r\right]+\sin\left[\left(\omega_c-\omega_r\right)t+\phi_c-\phi_r\right]\right\} \\ &+ A_r k_{lna} n(t)\sin\left(\omega_r t+\phi_r\right). \end{aligned} \tag{2.38}$$

When $r_q(t)$ is in quadrature with $s'_{am}(t)$, the mixer in the quadrature channel presents the following response:

$$s''_{am,q}(t) = \frac{1}{2}A_c A_r k_{lna}\left[1+m(t)\right]\sin\left(2\omega_r t\right)+A_r k_{lna} n(t)\sin\left(\omega_r t\right). \tag{2.39}$$

The filter, then, outputs

$$out_q = s''_{am,q}(t) * h_{lpf}(t) \cong 0 \tag{2.40}$$

The result illustrates a method used to sync the demodulator input waveforms, called the "null-shift" procedure. Considering a single-phase lock-in amplifier, and starting from an arbitrary initial phase condition, the reference phase is adjusted so that the demodulator presents a null value at its output. In this condition, equation 2.40 indicates that the demodulator inputs are in quadrature. Then, shifting the input reference phase by 90° leads to the desired in-phase condition, given by equation 2.37. This procedure can be carried out even under noisy conditions, and maximizes the output D.C. response for symmetric periodic signals, and almost maximizes the response for asymmetrical periodic signals [23].

Obviously, when considering two-phase lock-in amplifiers, the "null-shift" procedure is not necessary, as the in-phase and quadrature paths outputs correspond to the components of a phasor. Starting from Equations 2.35 and 2.38, and considering $\omega_c = \omega_r$ and $\phi = \phi_c - \phi_r$, the in-phase and quadrature channel outputs will be, respectively,

$$out_i = \frac{1}{2}A_c A_r k_{lna} k_{lpf} + \frac{1}{2}A_c A_r k_{lna} k_{lpf} m(t)\cos(\phi) \tag{2.41}$$

$$out_q = \frac{1}{2}A_c A_r k_{lna} k_{lpf} + \frac{1}{2}A_c A_r k_{lna} k_{lpf} m(t)\sin(\phi) \tag{2.42}$$

From equations 2.41 and 2.42, the phasor magnitude and phase can be calculated by:

$$|s(t)| = \sqrt{out_i^2 + out_q^2} \tag{2.43}$$

$$\phi_s(t) = \tan^{-1}\left(\frac{out_q}{out_i}\right) \tag{2.44}$$

In the same manner done for an amplitude modulated input, the demonstrations can be repeated for a phase modulated signal given by

$$s_{pm}(t) = A_c \cos[\omega_c t + m(t)] + n(t) \tag{2.45}$$

for this signal, the LNA output is

$$s'_{pm}(t) = k_{lna}\{A_c \cos[\omega_c t + m(t)] + n(t)\}, \tag{2.46}$$

and the mixer output in the in-phase path will be

$$\begin{aligned} s''_{pm,i}(t) &= s'_{pm}(t)\, r_i(t) \\ &= k_{lna}\{A_c \cos[\omega_c t + m(t)] + n(t)\} A_r \cos(\omega_r t + \phi_r) \\ &= A_c A_r k_{lna} \cos[\omega_c t + m(t)] \cos(\omega_r t + \phi_r) + A_r k_{lna} n(t) \cos(\omega_r t + \phi_r) \\ &= \frac{1}{2}A_c A_r k_{lna}\{\cos[(\omega_c - \omega_r)t + m(t) - \phi_r] + \cos[(\omega_c + \omega_r)t + m(t) + \phi_r]\} \\ &+ A_r k_{lna} n(t) \cos(\omega_r t + \phi_r). \end{aligned} \tag{2.47}$$

When $r_i(t)$ is synchronized with s'_{pm}, the output of the mixer of the in-phase path results in

$$\begin{aligned} s''_{pm,i}(t) &= \frac{1}{2}A_c A_r k_{lna}\{\cos[m(t)] + \cos[2\omega_r t + m(t)]\} + A_r k_{lna} n(t)\cos(\omega_r t) \\ &= \frac{1}{2}A_c A_r k_{lna}\cos[m(t)] + \frac{1}{2}A_c A_r k_{lna}\cos[2\omega_r t + m(t)] \\ &+ A_r k_{lna} n(t)\cos(\omega_r t). \end{aligned} \tag{2.48}$$

The in-phase path output is then

$$\begin{aligned} out_i &= s''_{pm,i}(t) * h_{lpf}(t) \\ &\cong \frac{1}{2} A_c A_r k_{lna} k_{lpf} \cos[m(t)] \\ &\cong \frac{1}{2} A_c A_r k_{lna} k_{lpf}, |m(t)| \ll 1. \end{aligned} \tag{2.49}$$

Consequently, the mixer response at the quadrature channel is

$$\begin{aligned} s''_{pm,q}(t) &= s'_{pm}(t) r_q(t) \\ &= k_{lna} \{A_c \cos(\omega_c t + m(t)) + n(t)\} A_r \sin(\omega_r t + \phi_r) \\ &= A_c A_r k_{lna} \cos[\omega_c t + m(t)] \sin(\omega_r t + \phi_r) + A_r k_{lna} n(t) \sin(\omega_r t + \phi_r) \\ &= \frac{1}{2} A_c A_r k_{lna} \{\sin[(\omega_c + \omega_r) t + m(t) + \phi_r] - \sin[(\omega_c - \omega_r) t + m(t) - \phi_r]\} \\ &+ A_r k_{lna} n(t) \sin(\omega_r t + \phi_r) \end{aligned} \tag{2.50}$$

and when $r_i(t)$ enters in quadrature with $s'_{pm}(t)$, the mixer output simplifies to

$$\begin{aligned} s''_{pm,q}(t) &= \frac{1}{2} A_c A_r k_{lna} \{\sin[2\omega_r t + m(t)] - \sin[m(t)]\} + A_r k_{lna} n(t) \sin(\omega_r t) \\ &= \frac{1}{2} A_c A_r k_{lna} \sin[2\omega_r t + m(t)] - \frac{1}{2} A_c A_r k_{lna} \sin[m(t)] + A_r k_{lna} n(t) \sin(\omega_r t). \end{aligned} \tag{2.51}$$

The quadrature path output becomes

$$\begin{aligned} out_q &= s''_{pm,q}(t) * h_{lpf}(t) \\ &\cong -\frac{1}{2} A_c A_r k_{lna} \sin[m(t)] \\ &\cong -\frac{1}{2} A_c A_r k_{lna} m(t), |m(t)| \ll 1 \end{aligned} \tag{2.52}$$

According to Equation 2.52, for a phase modulated signal, the demodulator works as a linear phase detector for small phase variations.

In general, it is expected that the sensor signal appears modulated both in phase and amplitude. Thus, considering a mixed modulation given by

$$s_{mm}(t) = A_m(t) \cos[\omega_c t + \phi_m(t)] + n(t) \tag{2.53}$$

the LNA output turns out to be

$$s'_{mm}(t) = k_{lna} \{A_m(t) \cos[\omega_c t + \phi_m(t)] + n(t)\} \tag{2.54}$$

and the output of the mixer in the in-phase path can be expressed as

$$\begin{aligned} s''_{mm,i}(t) &= s'_{mm}(t)\, r_i(t) \\ &= k_{lna}\left\{A_m(t)\cos\left[\omega_c t+\phi_m(t)\right]+n(t)\right\} A_r\cos\left(\omega_r t+\phi_r\right) \\ &= A_m(t)\, A_r k_{lna}\cos\left[\omega_c t+\phi_m(t)\right]\cos\left(\omega_r t+\phi_r\right)+A_r k_{lna} n(t)\cos\left(\omega_r t+\phi_r\right) \\ &= \frac{1}{2}A_m(t)\, A_r k_{lna}\left\{\cos\left[\left(\omega_c-\omega_r\right)t+\phi_m(t)-\phi_r\right]+\cos\left[\left(\omega_c+\omega_r\right)t+\phi_m(t)+\phi_r\right]\right\} \\ &+ A_r k_{lna} n(t)\cos\left(\omega_r t+\phi_r\right). \end{aligned} \tag{2.55}$$

When $r_i(t)$ is synchronized with s'_{mm}, the output of the mixer results in

$$\begin{aligned} s''_{mm,i}(t) &= \frac{1}{2}A_m(t)\, A_r k_{lna}\left\{\cos\left[\phi_m(t)\right]+\cos\left[2\omega_r t+\phi_m(t)\right]\right\}+A_r k_{lna} n(t)\cos\left(\omega_r t\right) \\ &= \frac{1}{2}A_m(t)\, A_r k_{lna}\cos\left[\phi_m(t)\right]+\frac{1}{2}A_m(t)\, A_r k_{lna}\cos\left[2\omega_r t+\phi_m(t)\right] \\ &+ A_r k_{lna} n(t)\cos\left(\omega_r t\right). \end{aligned} \tag{2.56}$$

The in-phase path output is

$$\begin{aligned} out_i &= s''_{mm,i}(t) * h_{lpf}(t) \\ &\cong \frac{1}{2}A_m(t)\, A_r k_{lna} k_{lpf}\cos\left[\phi_m(t)\right] \\ &\cong \frac{1}{2}A_m(t)\, A_r k_{lna} k_{lpf}, \left|\phi_m(t)\right| \ll 1. \end{aligned} \tag{2.57}$$

The mixer response at the quadrature channel is

$$\begin{aligned} s''_{mm,q}(t) &= s'_{mm}(t)\, r_q(t) \\ &= k_{lna}\left\{A_m(t)\cos\left(\omega_c t+\phi_m(t)\right)+n(t)\right\} A_r\sin\left(\omega_r t+\phi_r\right) \\ &= A_m(t)\, A_r k_{lna}\cos\left[\omega_c t+\phi_m m(t)\right]\sin\left(\omega_r t+\phi_r\right)+A_r k_{lna} n(t)\sin\left(\omega_r t+\phi_r\right) \\ &= \frac{1}{2}A_m(t)\, A_r k_{lna}\left\{\sin\left[\left(\omega_c+\omega_r\right)t+\phi_m(t)+\phi_r\right]-\sin\left[\left(\omega_c-\omega_r\right)t+\phi_m(t)-\phi_r\right]\right\} \\ &+ A_r k_{lna} n(t)\sin\left(\omega_r t+\phi_r\right). \end{aligned} \tag{2.58}$$

When $r_q(t)$ is in quadrature with $s'_{mm}(t)$,

$$\begin{aligned} s''_{mm,q}(t) &= \frac{1}{2}A_m(t)\,A_r k_{lna}\left\{\sin\left[2\omega_r t+\phi_m(t)\right]-\sin\left[\phi_m(t)\right]\right\}+A_r k_{lna}n(t)\sin(\omega_r t) \\ &= \frac{1}{2}A_m(t)\,A_r k_{lna}\sin\left[2\omega_r t+\phi_m(t)\right]-\frac{1}{2}A_m(t)\,A_r k_{lna}\sin\left[\phi_m(t)\right] \\ &+ A_r k_{lna}n(t)\sin(\omega_r t)\,. \end{aligned} \tag{2.59}$$

The quadrature path output turns out to be

$$\begin{aligned} out_q &= s''_{mm,q}(t) * h_{lpf}(t) \\ &\cong -\frac{1}{2}A_m(t)\,A_r k_{lna}\sin\left[\phi_m(t)\right] \\ &\cong 0, |\phi_m(t)| \ll 1 \end{aligned} \tag{2.60}$$

Equations 2.57 and 2.60 show that, for small phase variations, the input signal amplitude can be tracked without incurring in serious errors. Nevertheless, the single-phase lock-in amplifier is unsuited to track phase variations in general (as can also be verified through Equations 2.49 and 2.52). However, the two-phase lock-in amplifier is not subjected to such constraints.

2.5 Lock-in amplifier architecture

The overall proposed system architecture is illustrated in Figure 2.8, where, for completeness, the discrete photodiode is also represented.

An externally generated reference signal could be used to stimulate the LED at the input of the fiber optic sensor, as well as a reference to the lock-in amplifier (LIA), provided this one has a phase adjustment circuit to allow the syncing of the mixer input signals. As the developed prototype has no such circuit, an externally generated reference signal is used to stimulate the LED, and another externally generated differential signal is supplied to the local oscillator (LO) port of the LIA. Both signals can be generated by bench function/arbitrary waveform generators (FAWGs).

It should be noticed that all blocks that constitutes the LIA have a fully-differential topology. This increases circuit complexity and power consumption, but, at the other hand, it mitigates the noise coupling problem, improve supply noise immunity and dynamic range and, consequently, the SNR [28].

The amplification path of the LIA is constituted by the Transimpedance amplifier (TIA) with its associated DC photocurrent rejection circuit, constituted by transistors M_0 through M_4 and the low-pass filter formed by the OTA and C_1. The

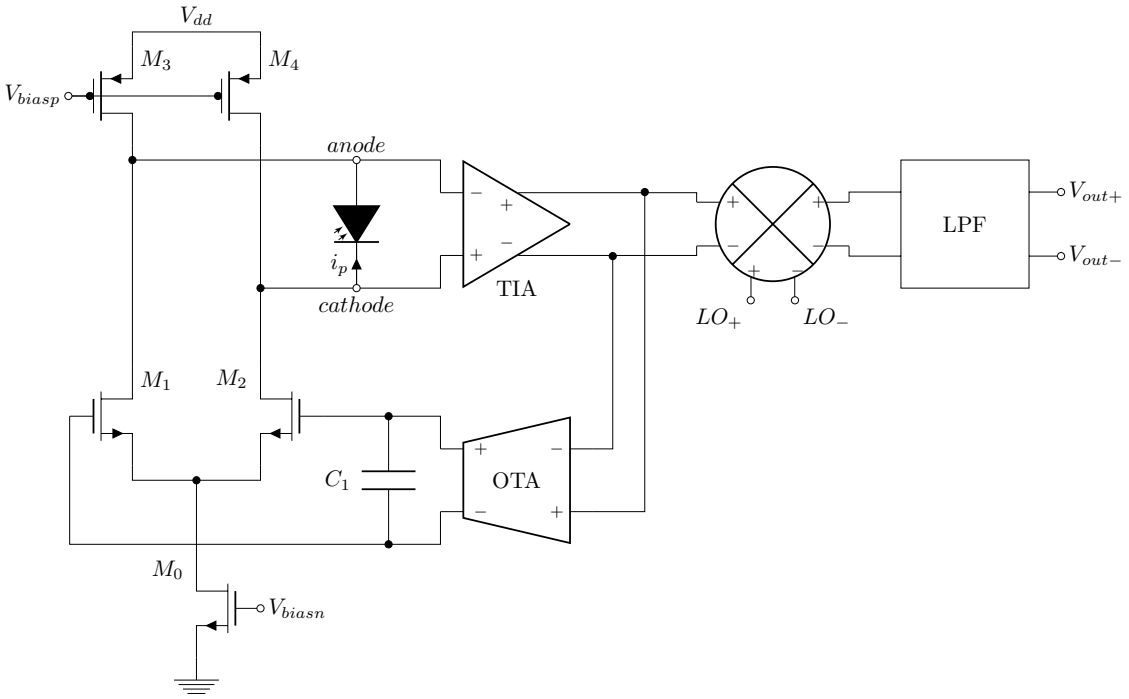


Figure 2.8: Proposed topology for a single-phase lock-in amplifier.

circuits were designed to sustain an external discrete photodiode in zero-bias mode (more details on photodiode operation are given in Section 3.2), to reject DC currents up to 10 μA and to amplify the weak modulated signal generated by the fiber optic sensor. To simplify the work for a first prototype, the TIA was developed with a fixed gain equal to 20 kΩ. Adjustable or programmable gain could be implemented by substituting the gain setting resistors by transistors or R-2R or M-2M networks.

The mixer and low-pass filter constitute the synchronous demodulator, responsible for the task of signal recovering. As demonstrated in the previous section, provided that the signals are in sync, the mixer rectifies the signal coming from the amplification path, generating a component at DC and another one at the double of the signal frequency. The low-pass filter attenuates the high frequency component to obtain a signal without ripple in its output, proportional to the amplitude of the input modulating signal.

Mixer gain is a function of input signals amplitude and can be adjusted by changing the amplitude of the LO signal. The low-pass filter (LPF) gain can be adjusted by setting the voltage at the V_{tun} port of the LIA.

The LPF has a huge influence in some important LIA performances. It determines the equivalent noise bandwidth, as well as its settling time [18].

2.6 Sizing methodology

Sizing of integrated circuits is a hard problem. The designer should find component parameters that satisfies conflicting circuit and system performances. Because of that, there are various methodologies to ease and/or optimize circuit sizing. Some of these works were revised in order to find a suitable methodology to be used in the design of the various circuits of this project.

Traditional books on analog integrated circuit design [25, 26] teach sizing circuit through the solution of analytical equations derived from simplified small-signal and large-signal models of devices. The required equation constants (e.g. oxide capacitance per unit area, carrier mobility) are obtained from the technology manuals or extracted through a suitable method from simulations or from physical devices, and are valid for a specific bias point.

The problem with this methodology is that the handled models are kept simple so as to not complicate the manipulation of the analytical equations but, when the sized circuit is simulated considering high-order effects, the results deviates drastically from the expected outcome. Unless the circuit does not suffer a significant influence of second order effects (e.g. velocity saturation, mobility degradation due to vertical field, drain induced barrier lowering, etc), it will not work. In modern technologies, as the one used in this work, this is not generally the case, as several high order effects are modeled.

In practice, the general procedure to carry out transistor sizing in an integrated circuit design is to simulate the transistor with fixed bias voltages and channel length and sweep channel width so as to find the width corresponding to the desired drain current [29]. This procedure is repeated for all transistors in the design. In fact, you can sweep any design variable, while keeping the others fixed.

The above procedure is generally tedious and painful as it requires a large number of simulation runs, which are expensive operations to be constantly executed. On the other hand, the transistors can be precisely biased and circuit behavior can be verified directly from simulations and fine tuned.

Concerned with such difficulties, two methods are presented in [30] based on the g_m/I_D methodology, associated with a computer algebra system (CAS). The first method, termed "the semi-empirical approach", consists of creating a lookup table with values of small-signal model parameters (G_m, G_{mb}, G_{DS}), drain currents and capacitances for various bias and channel lengths, but at a fixed channel width. In the second method, termed "the compact model approach", a lookup table with the extracted values of the Enz-Krummenacher-Vittoz (EKV) model is created for various values of bias (terminal voltages), channel lengths and a fixed channel width. In [30], the values where obtained from measures over the physical devices, but they

can also be obtained from simulations (of high level models). A methodical sizing procedure, using one of the approaches, are then developed and the derived analytic equations are entered in the computer algebra system so as to create a function that can be used for sizing. The function makes heavy use of the CAS interpolation functions and can use all its other capabilities like plot utilities.

This methodology improves the accuracy of that described in the traditional books on analog integrated circuit design, and can be easily used to resize the circuit by just changing the specifications. However, it is difficult to set up everything and create the sizing script. Also, the procedure is inflexible. If another performance is needed to be considered, the script must be adapted, or a new one has to be created.

Another book [31] analyses the tradeoffs that usually occur in analog IC design and explains the methodology employed by the author to size IC devices. The method is also based on the EKV MOSFET model and many of the model parameters are extracted from the considered technology and listed in a spreadsheet. All circuit devices are also listed in the spreadsheet with its intended channel length, drain current and inversion coefficient. Based on these three parameters, the channel width and several other MOSFET performances are calculated. These MOSFET performances are used to calculate overall circuit performances.

Despite using approximated model equations, as the equations used consider various second-order effects, the results are relatively accurate. The method is more flexible, as it enables the easy exploration of design choices over circuit performances, providing a better insight.

In this work, an approach similar to the one presented in [31] is used.

As the model used in the adopted PDK (process development kit) was the PSP [32], a Verilog-AMS[2] description of the model, with all equations, exactly as implemented in simulators, was adapted to MATLAB. With the model parameters taken directly from the PDK, and passing the design parameters listed in Table 2.1, the adapted code enabled to run an operation point analysis and obtain several MOSFET performances. Based on the MOSFET performances, circuit performances can be accurately determined and design tradeoffs can be explored by changing the choices for the design parameters of Table 2.1.

The following advantages can be highlighted: (1) the code runs very fast because it is optimized for numerical simulation; (2) the accuracy is the same as the model used in the simulator tool; (3) it enables easy exploration of design choices.

[2]Verilog-AMS is a description language used for modelling digital, analog, mixed-signal and multiphysics systems. It is considered a good practice to describe MOSFET models in Verilog-AMS and have a third program translate the description to an optimized code that can be implemented in simulators. The objective is to ensure that the model implemented in simulators is equal to that provided by the model developer.

Table 2.1: Sizing function parameters

device id
drain voltage (V_d)
gate voltage (V_g)
source voltage (V_s)
substrate/bulk voltage (V_b)
channel length (L)
channel width (W)
drain current (I_d)
inversion coefficient (IC)
number of parallel transistors (multipliers - Mult)
number of fingers (NF)
ambient temperature

Chapter 3

Circuit Design and Analysis

In this chapter, initially, some comments about the adopted CMOS process technology are made. Next, the chosen topologies for the various blocks that constitute the lock-in amplifier are presented and functioning principles explained.

3.1 Initial considerations about the technology

The technology employed in this work design presents several transistor options, e.g. low voltage, RF, isolated, high V_t, high voltage. The low voltage *nfet* and *pfet* transistors were used throughout the project due to the fact that they have the smallest number of masks. Overall, this enables reduction of the project cost, because the use of the other MOSFET models would, necessarily, imply in an increase in the number of manufacturing steps.

Even employing great care and effort in the design of the low-pass filter so as to keep the capacitance values as small as possible, as the signal to be conditioned by the lock-in amplifier has extremely low frequency, the values found for these capacitances are two orders of magnitude above what is generally seen in typical integrated circuits. However, the technology used has the capability of manufacturing metal-insulator-metal (MIM) capacitors with capacitance values within the desired order of magnitude.

To produce capacitance values as high as the desired ones without taking up a large silicon area, the technology offers a dual MIM capacitor device, one in which one plate lies between two other plates connected in parallel, as shown in Figure 3.1. There is also the option, for both the standard and dual MIM capacitors, to employ a high density insulating material, to obtain even higher capacitance values.

The high density dielectric option was not used in the project because it is unavailable in the prototyping service (MPW) used. So, the dual MIM capacitor ($DUALCMIM$) that has twice the capacitance per unit area of the MIM capacitor ($4.10\,\frac{fF}{\mu m^2}$ against $2.05\,\frac{fF}{\mu m^2}$) was used.

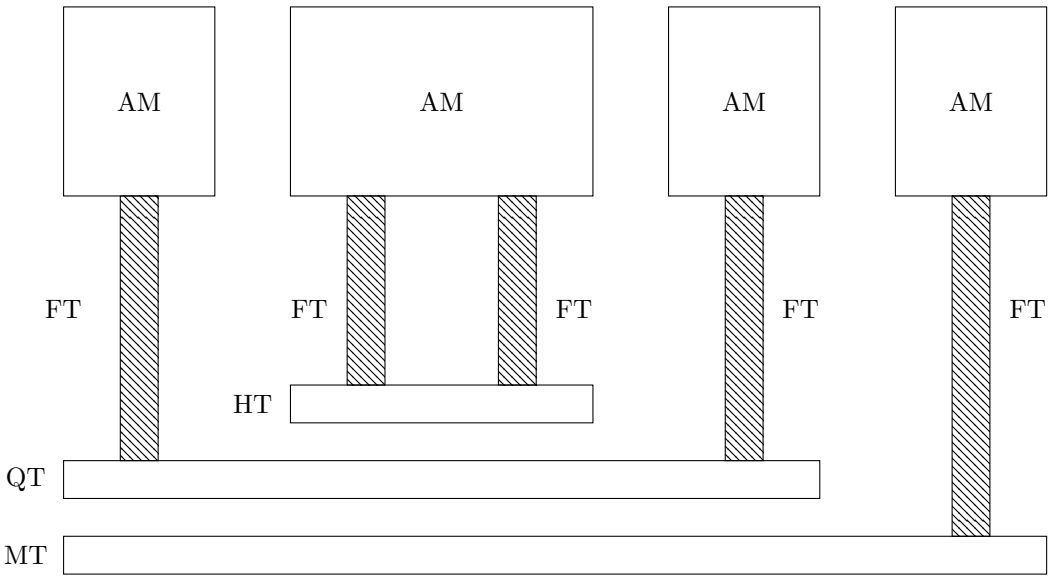


Figure 3.1: Sectional view of a dual MIM capacitor. AM is the thick aluminum metal, FT is a square via that connects AM to MT and the capacitor plates, HT and QT are capacitor plates in copper and MT is the bottom capacitor plate in copper.

In filters with differential topology, instead of using a capacitor suspended between the differential nodes, it is typical to use two capacitors with double the capacitance value, each one connected from one of the differential nodes to ground node. This is done to mitigate the imbalance among the differential nodes caused by differences between the magnitude of the parasitic component that appears between the substrate and the bottom plate of the capacitor, and that associated with the interaction between the substrate and the top plate [29]. As the MIM capacitors in the technology used are set far from the substrate (the MIM capacitors seat between the penultimate and top metal layers), the magnitude of the parasitic components is therefore alleviated. Moreover, as it is not affordable to multiply the already high capacitances obtained for the low-pass filter at the risk of getting impracticable values, it was defined to use suspended capacitors between differential nodes so as to reduce the area of silicon and, consequently, reduce the overall IC cost.

The technology also allows placing the capacitors above circuit areas that use up to the antepenultimate metal layer (in our case, M4), increasing the density and reducing the total area of the circuit. This option, obviously, would create parasitic elements that could interfere in the operation of the circuit and thus was avoided when conducting the prototype layout. However, if a project has serious area or cost constraints, it is an option to be considered.

It is worth mentioning that according to the technology manual [33], the devices have been characterized and are assured to support operating conditions that do not exceed 10% of their nominal values. The models are valid for junction temperatures

in the range $[-40°C; 150°C]$.

All circuits were designed to operate with a single power supply of 1.8 V.

3.2 DC photocurrent rejection circuit

In the literature, it is easy to find works related to optical receivers were the photodetector, almost always a photodiode, is biased with a reverse voltage, so as to increase junction depletion region, reduce photodiode capacitance and increase receiver speed. The increase in speed comes with an increase in leakage current (or dark current), I_{DC} in Figure 2.5, that causes a rise in shot noise, as predicted by Equation 2.13. This mode of operation is known as the photoconductive mode.

In this work, the photodiode was chosen to be kept with zero bias. This option was adopted because, in this mode of operation, the value of the photodetector shunt resistor (see Figure 3.2) is fixed, thereby generating an output current that is linearly dependent on the incident radiation level, and the leakage current is greatly reduced, consequently reducing shot noise. The envisaged application does not require a high speed photodetector, but one that can implement a highly accurate conversion between the received light signal and the generated output electrical signal (current). Fixing the photodiode between the transimpedance amplifier input terminals, force the photodiode to remain in zero-bias mode.

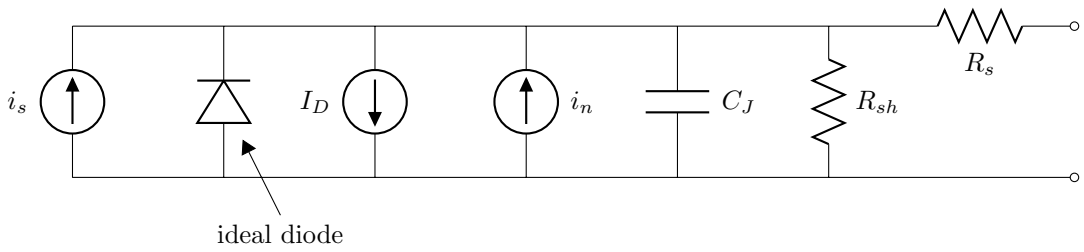


Figure 3.2: Photodiode model. i_s is the signal current, I_D the dark current, i_n a noise current, C_j the junction capacitance, R_{sh} the shunt resistance, R_s the series resistance, and the ideal diode models the diode characteristic of the photodiode when this is direct biased.

Since the sensitivity of the photodiode varies with its voltage, the photodiode voltage has a nonlinear relationship with incident light energy. On the other hand, photodiode current has a linear relationship with the incident light energy when the voltage across the photodiode is maintained constant, so as to stabilize its sensitivity. Therefore, photodiode current monitoring with a zero bias voltage is the preferred option when accuracy is the most desired feature.

To keep the photodiode with zero bias, it was connected between the fully-differential transconductance amplifier inputs (see Figure 3.3). This way, the voltage across the photodiode is virtually zero.

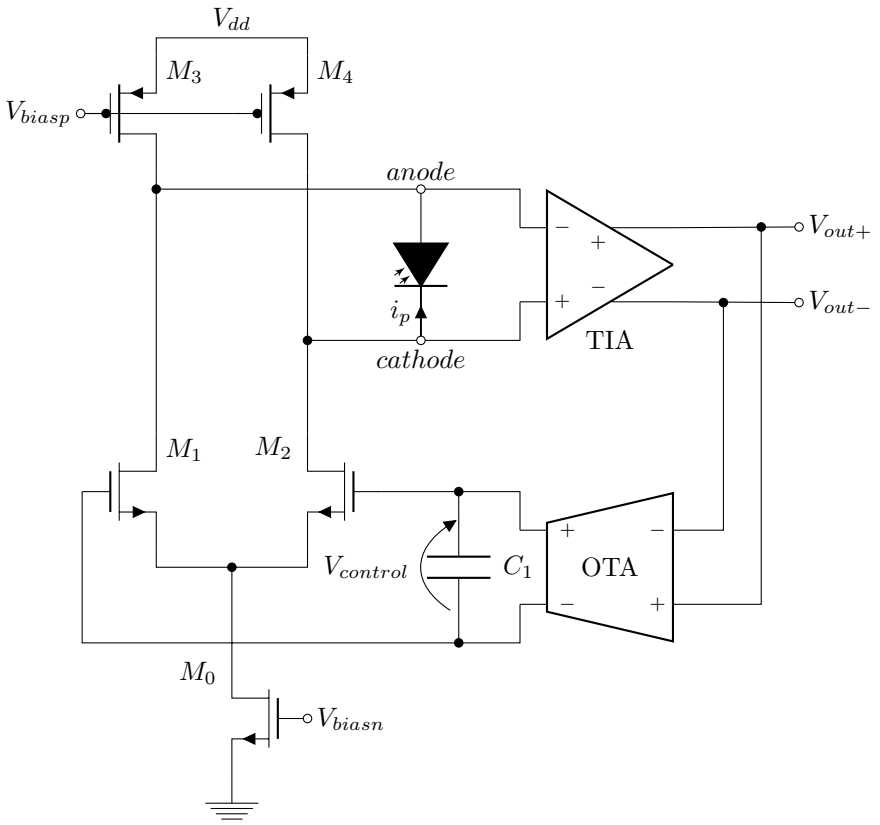


Figure 3.3: DC photocurrent rejection circuit solution. The TIA amplifies the photocurrent i_p and the loop formed by the low-pass filter (OTA + C_1) and $M_0 - M_4$ transistors act to reject the DC component of the photocurrent.

Beyond assuring a linear conversion of the optical signal to an electrical signal, another concern that exists is the rejection of the DC current generated by the photodiode so as to avoid saturation of the output of the transimpedance amplifier. With the objective of rejecting the DC component, that can be much higher than the modulated optical signal, the scheme shown in Figure 3.3 is employed. It was adapted from the works presented in [34–36]. The properties of transistors $M_0 - M_4$ and capacitor C_1 of the designed circuit are presented, respectively, in Tables 3.1 and 3.2. The OTA is presented in Subsection 3.2.1 and the TIA in Section 3.3.

Table 3.1: Transistors dimensions of the DC photocurrent rejection circuit

Component	Type	L	W	Multiplicity	Intended operating region
M_0	*nmos*	5 μm	840 nm	10 (parallel)	saturation
M_1; M_2	*nmos*	5 μm	39 μm	4 (parallel)	triode; saturation
M_3; M_4	*pmos*	5 μm	840 nm	5 (parallel)	saturation

The circuit works as follows, the DC photocurrent generated by the photodiode causes an offset at the output of the TIA. The low-pass filter formed by the OTA and capacitor C_1 senses this offset and generates a proportional signal that is injected

Table 3.2: Capacitor dimensions of the DC photocurrent rejection circuit

Component	Type	L	W	Multiplicity	Total capacitance
C_1	dual CMIM	120.55 μm	120.55 μm	2	126.47464 pF

in the gates of M_1 and M_2 that will act to regulate this offset by sinking more or less current, so as to drain the constant component of the photocurrent towards M_0, thereby eliminating the influence of the DC photocurrent over the TIA output.

Transistors M_0, M_3 and M_4, since they will always be in saturation region, work as current sources, as well as the photodiode. Considering that the cathode of the photodiode is connected to the drain of M_4, and the anode to the drain of M_3, the photodiode will drain part of the steady current generated by M_3. The other part will follow through M_1 so as to be drained by M_0. The DC photocurrent generated by the photodiode will sum with the steady current generated by M_4 and will follow through M_2 so as to be drained by M_0 as well. The transistors M_1 and M_2 work as valves, and can operate in the triode or saturation regions, because the sum of the currents passing through these transistors will be forced by M_0 and by the combination of M_3, M_4 and the photodiode.

Considering that $V_{control}$ is the output of the OTA-C filter and G_m the OTA transconductance, we can write

$$\frac{V_{control}}{V_{out}} = \frac{G_m}{sC_1} \therefore V_{control} = \frac{G_m}{sC_1} V_{out} \tag{3.1}$$

The current drained by the differential pair is thus

$$i = -g_m \frac{G_m}{sC_1} V_{out} \tag{3.2}$$

where g_m is the transconductance of transistors $M_{1,2}$ of the differential pair. It could also be verified that

$$V_{out} = (i_p + I_{DC})\, G_\Omega \therefore I_{DC} = \frac{V_{out}}{G_\Omega} - i_p \tag{3.3}$$

where I_{DC} is the DC component of the current generated by the photodiode and i_p the AC component. G_Ω is the gain of the transimpedance amplifier.

The transfer fucntion for the DC photocurrent rejection circuit can be obtained from Equations 3.2 and 3.3 as

$$-g_m \frac{G_m}{sC_1} V_{out} = \frac{V_{out}}{G_\Omega} - i_p \therefore \frac{V_{out}}{i_p} = \frac{G_\Omega s}{s + \frac{g_m G_m G_\Omega}{C_1}} \tag{3.4}$$

The circuit was designed to be capable of rejecting DC currents up to 10 μA,

the maximum value that transistors $M_{3,4}$ can source.

3.2.1 Operational transconductance amplifier (OTA)

Preliminarily, during design, the OTA used in the low-pass filter at the output of the LIA (presented in Section 3.5.1) was also applied to the filter of the DC photocurrent rejection circuit. It worked in nominal conditions, but failed when considering mismatch and process variations due to its high input offset, so, a topology with smaller offset and small transconductance was then seek. A satisfactory solution was found in [37]. The technique employed in the cited work to reduce, simultaneously, transconductance and offset, is thoroughly explained in [38, 39].

The topology used in this work is shown in Figure 3.4. The attenuator used in the OTA of Section 3.5.1 was associated with the OTA presented in [37] to improve linearity. In order to further improve linearity and reduce transconductance, the differential pair current source was split in two and a degeneration transistor M_{tun} is connected between the sources of the differential pair transistors.

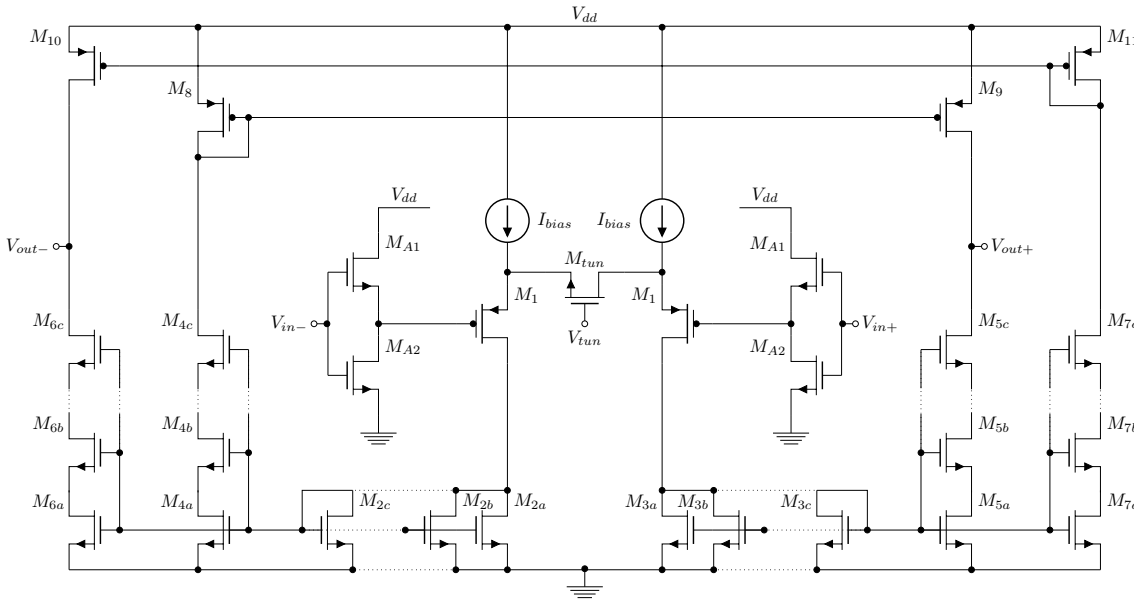


Figure 3.4: Topology for the OTA of the DC photocurrent rejection circuit.

Also, a differential output amplifier was needed, so, an extra pair of series-parallel current mirrors was added. The current division factor from the input to the output was chosen to be 25. This factor was implemented by five transistors in parallel at the input and five transistors in series at the output.

In nominal conditions, the OTA presented a transconductance of $7nS$, which enabled to attain a filter cutoff frequency of $25mHz$, enough to let the signal of interest pass without attenuation and reject the DC component.

To bias the output with a common-mode voltage of $1.35V$, transistors $M_8 - M_{10}$

were implemented with an association of eight transistors in series, so as to not have an uncommon device with channel length much bigger than channel width, which would complicate the circuit layout.

Table 3.3: Transistors dimensions for the OTA of Figure 3.4

Component	Type	L	W	Multiplicity	Intended operating region
M_{A1}	*nmos*	5 μm	1 μm	1	saturation
M_{A2}	*nmos*	5 μm	1 μm	2 (parallel)	triode
M_1	*pmos*	5 μm	6.31 μm	2 (parallel)	saturation
M_2; M_3	*nmos*	5 μm	1.69 μm	5 (parallel)	saturation
M_4; M_5; M_6; M_7	*nmos*	5 μm	1.69 μm	5 (series)	saturation
M_8; M_9; M_{10}; M_{11}	*pmos*	5 μm	650 nm	8 (series)	saturation
M_{tun}	*nmos*	450 nm	500 nm	1	saturation

3.3 Transimpedance amplifier (TIA)

The fully-differential transimpedance amplifier used in this work, shown in Figure 3.5, was derived from the differential output instrumentation amplifier presented in [40], where the input buffers where changed by current-to-voltage converters.

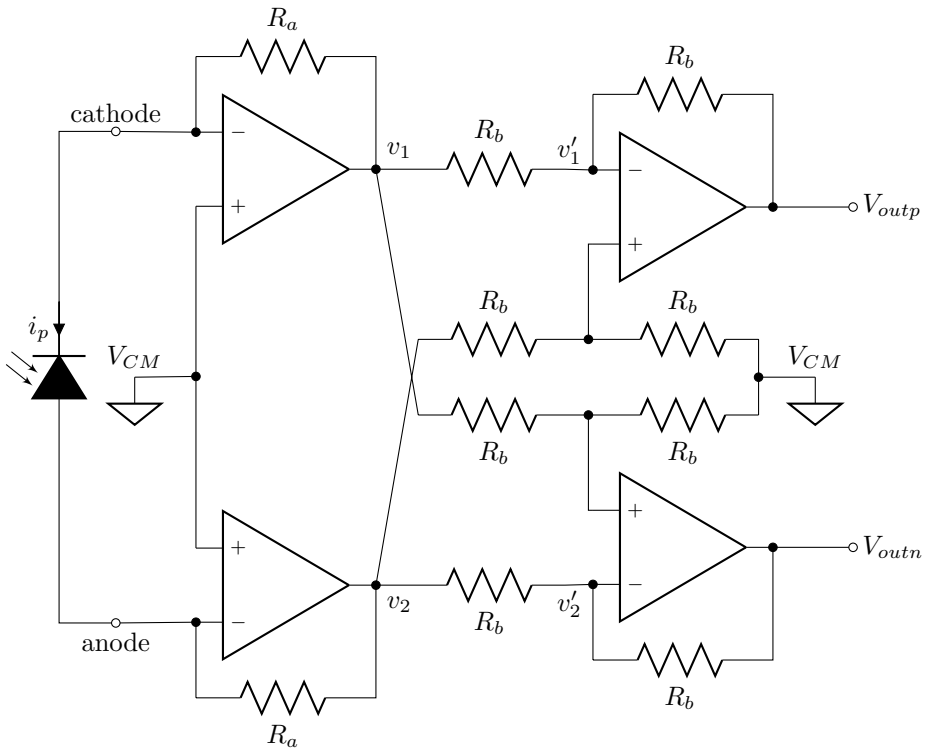


Figure 3.5: Trasimpedance amplifier (TIA) topology.

Initially, it was considered the use of the fully differential current-to-voltage converter presented in [41], but it was verified that, due to the voltage subtractor at the output of the amplifier, the converter actually had a single-ended output.

The replacement of the voltage subtractor by a differential amplifier, as in [18], was then tried. But it was later realized that this change affected the characteristic of the converter.

The differential gain of the TIA can be easily found to be (see Appendix A)

$$\frac{V_{outp} - V_{outn}}{i_p} = -4R_a \tag{3.5}$$

The resistance values and dimensions of the resistors that compose the transimpedance amplifier are presented in Table 3.4. The value of R_a was made to be 5 kΩ so as to produce a gain of 20 kΩ. The value chosen for R_a is small enough so as to avoid large thermal noise power. The same observation applies to R_b.

The resistor type *opppcres* [33] was selected based on its mismatch performance. It presented the smaller mismatch compared to the other options available.

Table 3.4: Transimpedance amplifier (TIA) resistors dimensions

Component	Type	L	W	Series bars	Total resistance
R_a	opppcres	6.69 μm	3 μm	8	5003.76 Ω
R_b	opppcres	4 μm	3 μm	8	3113.52 Ω

The topology of Figure 3.5, based on the traditional instrumentation amplifier, inherit its performance characteristic, as excellent common-mode and power supply rejection. The fully-differential transimpedance amplifier employs four identical traditional Miller operational amplifiers, as shown next.

3.3.1 Operational amplifier

The operational amplifier employed in the transimpedance amplifier needs a very low output impedance, as the impedance seen by its output is very small, due to the relatively small values used for the resistors R_a and R_b shown in Figure 3.5. The topology of the operational amplifier is shown in Figure 3.6. A traditional two-stage Miller operational amplifier was used, and to reduce the output impedance, a push-pull stage was added.

With the push-pull stage, the output impedance was reduced to a value near that seen at its output, which enabled a correct operation of the transimpedance amplifier. However, a tradeoff does exist, to accomplish its task, the push-pull stage requires a significant quiescent current. The quiescent current of the push-pull stage amounts to $12\mu A$, while the total quiescent current of the amplifier is $14.5\mu A$.

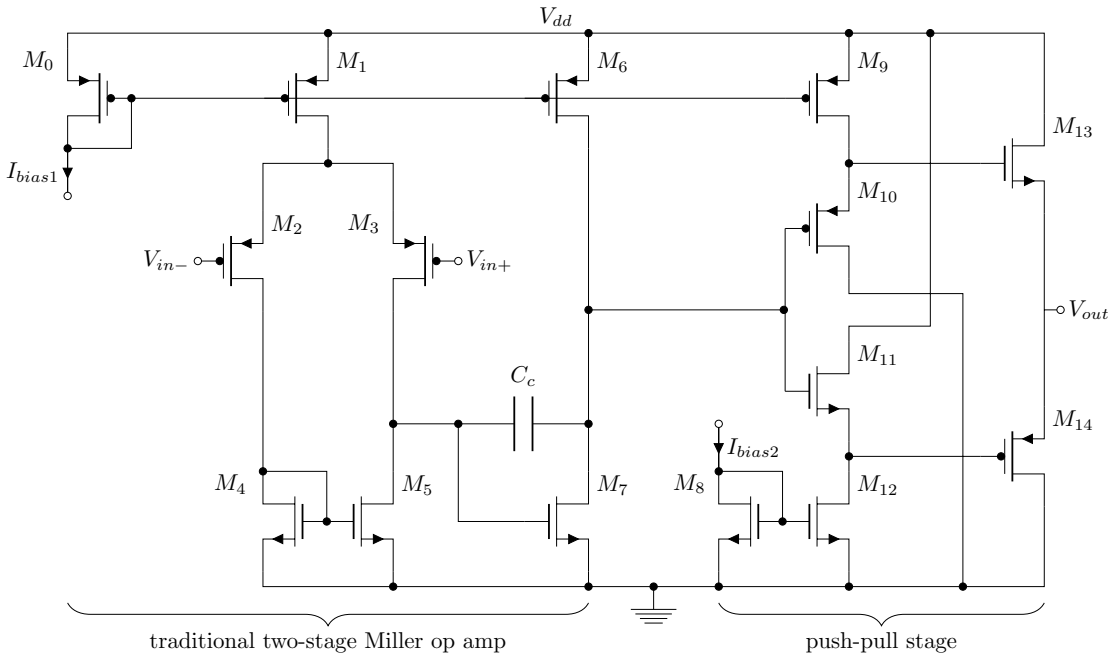


Figure 3.6: Operational Amplifier topology.

The devices and component dimensions are presented in Tables 3.5 and 3.6. With the output push-pull stage, the operational amplifier output impedance was made as small as 2.649 kΩ.

3.4 Mixer

The mixer (or analog four-quadrant multiplier) of the synchronous demodulator was implemented by means of a double balanced Gilbert-cell mixer (Figure 3.7). The double balanced characteristic concerns the property of avoiding RF and LO signals to pass through and appear at the output.

To lower the output common-mode voltage and buffer the mixer output, a level-shifter was implemented through the use of a common-drain stage, as suggested in [42]. Devices dimensions are presented in Table 3.7.

The mixer transfer function is given by [11]

$$V_{out} = k \cdot V_{RF} \cdot V_{LO} \tag{3.6}$$

where V_{RF} is the TIA output signal, V_{LO} the externally provided reference signal, and k the mixer gain, that is a function of bias current I_{DS} of transistor M_1. The common-drain stage does not contribute to mixer gain, as it has an unitary voltage gain.

Table 3.5: Transistors dimensions for the operational amplifier block

Component	Type	L	W	Multiplicity	Intended operating region
M_0	*pmos*	5 μm	6.36 μm	4 (parallel)	saturation
M_1	*pmos*	5 μm	6.36 μm	2 (parallel)	saturation
M_2; M_3	*pmos*	5 μm	20.04 μm	4 (parallel)	saturation
M_4; M_5	*nmos*	5 μm	1.54 μm	1	saturation
M_6	*pmos*	5 μm	6.36 μm	4 (parallel)	saturation
M_7	*nmos*	5 μm	1.54 μm	4 (parallel)	saturation
M_8	*nmos*	5 μm	1.52 μm	2 (parallel)	saturation
M_9	*pmos*	5 μm	6.36 μm	8 (parallel)	saturation
M_{10}	*pmos*	5 μm	6.36 μm	2 (parallel)	saturation
M_{11}	*nmos*	5 μm	1.52 μm	2 (parallel)	saturation
M_{12}	*nmos*	5 μm	1.52 μm	4 (parallel)	saturation
M_{13}	*nmos*	180 nm	7.82 μm	1	saturation
M_{14}	*pmos*	180 nm	8.4 μm	1	saturation

Table 3.6: Capacitor dimensions for the operational amplifier block

Component	Type	L	W	Multiplicity	Total capacitance
C_c	dual CMIM	15 μm	15 μm	1	1.457533 pF

3.5 Low-pass filter

Integrated filters can be classified in two basic types: continuous-time and discrete-time (switched-capacitor filters). Continuous-time filters are preferred in medium dynamic range applications (roughly between 40 and 100 dB) and where high speed and/or low power dissipation are needed [28]. On the other hand, switched-capacitor filters are less sensitive to temperature changes and have the ability of adjusting the cutoff frequency by changing the clock frequency.

Switched-capacitor filters, as any discrete-time systems, are subject to aliasing. To avoid this effect, a continuous-time signal needs to be conditioned, by a continuous-time low-pass filter, to limit its bandwidth, before being sampled [29].

Considering that, switched-capacitor filters require a continuous-time low-pass filter to precede them, that discrete-time systems are more difficult to simulate, and that the filter switching could be a potential noise source, a continuous-time low-pass filter was chosen to be used at the LIA output.

There are several techniques to implement continuous-time filters, among which the MOSFET-C and the G_m-C stand out. The MOSFET-C filters are constructed similarly as RC-active filters, using capacitors and the operational amplifiers and the resistors are replaced by MOSFETs operating in the triode region. This technique has two main disadvantages: (i) operational amplifiers with small output impedance

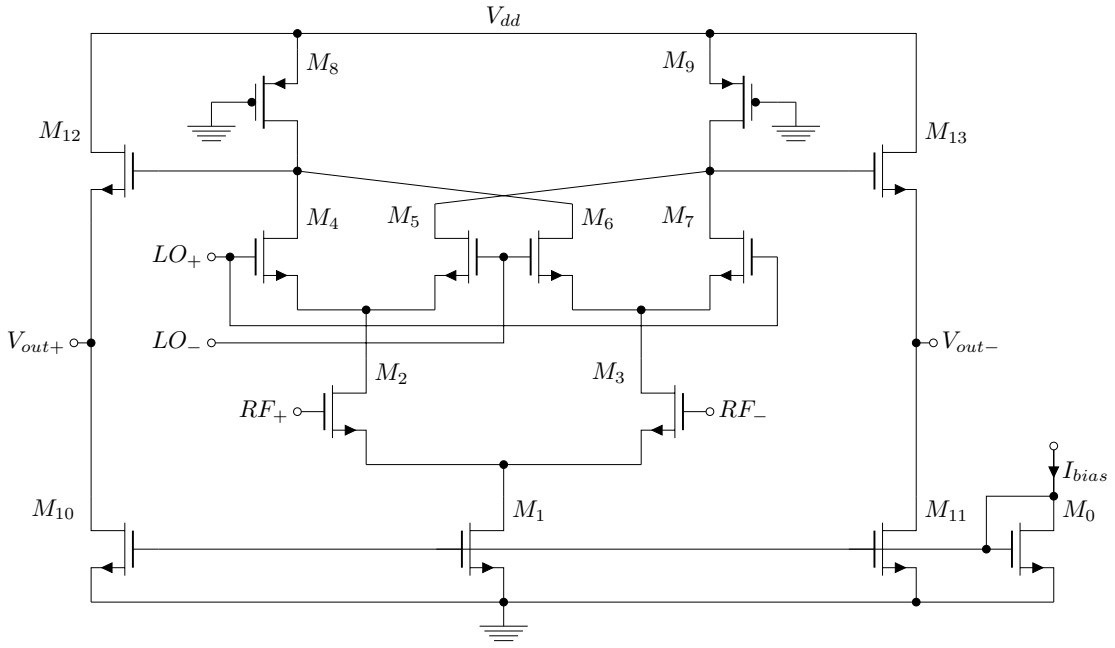


Figure 3.7: Mixer topology, consisting of a Gilbert cell and an common-drain amplifier working as a buffer and level-shifter.

Table 3.7: Transistors dimensions for the mixer block.

Component	Type	L	W	Multiplicity	Intended operating region
M_0	*nmos*	5 μm	1.52 μm	2 (parallel)	saturation
M_1	*nmos*	5 μm	1.52 μm	8 (parallel)	saturation
M_2; M_3	*nmos*	5 μm	1.26 μm	2 (parallel)	saturation
M_4; M_5; M_6; M_7	*nmos*	5 μm	2.24 μm	2 (parallel)	saturation
M_8; M_9	*pmos*	5 μm	250 nm	2 (parallel)	saturation
M_{10}; M_{11}	*nmos*	5 μm	1.52 μm	2 (parallel)	saturation
M_{12}; M_{13}	*nmos*	5 μm	5.46 μm	2 (parallel)	saturation

can't be easily designed in CMOS technology without incurring in huge quiescent currents, and (ii) the distortion due to the MOSFETs increases the distortion of the filter, which reduces its dynamic range.

G_m-C filters, on the other hand, are composed of OTAs and capacitors. Unlike operational amplifiers, OTAs, require high output impedances, that are relatively easy to be obtained in CMOS technologies. A number of transconductance linearization techniques can be applied to improve the dynamic range of G_m-C filters[29].

In this work, a third-order Chebyshev G_m-C low-pass filter was designed to integrate the mixer output an obtain a voltage value proportional to the magnitude of the input modulating signal. The filter cutoff frequency was chosen as 50 Hz. At 200 Hz the filter would provide 40 dB of attenuation and 60 dB at 400 Hz.

Continuous-time filters with poles in this frequency range would require large ca-

pacitance values, which are impractical in IC realization. In the case of G_m-C filters, to reduce the capacitance values, transconductors with very small transconductance values (at the order of a few nano-siemens) can be employed. An OTA with such characteristic is presented in Section 3.5.1. It is based on the one developed in [29] and is employed in the implementation of the LIA's output low-pass filter.

Continuous-time filters are known to be highly susceptible to element value variations due to manufacturing tolerances, temperature variations, aging, etc. To tackle this problem, automatic tuning techniques are employed in which elements are tuned by varying their bias voltage or current [28].

To keep system complexity to a reasonably level, and as an automatic tunning circuit for the low-pass filter is not absolutely indispensable, it was chosen to not implement an automatic tunning circuit for this prototype, even knowing that the mismatch and the manufacturing process variations can displace the cutoff frequency to a value that could significantly impact the LIA operation.

There are two common approaches for topology synthesis in continuous-time filters. The simplest approach constitutes in cascade second-order sections (biquads), each section implementing a pole pair of the transfer function. The second approach, the one used in this work, starts by finding the appropriate passive LC ladder prototype, and replacing each inductor by a gyrator and a capacitor with an appropriate value, so as to emulate the replaced inductor.

Considering the already mentioned filter specifications, and using the *ELETSIM* software[1], the LC ladder prototype shown in Figure 3.8 was obtained. The component values, denormalized in frequency are listed in Table 3.8.

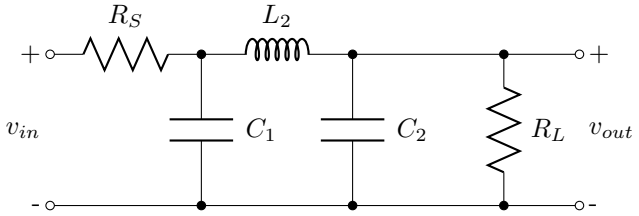


Figure 3.8: LC doubly terminated ladder prototype for the low-pass filter.

As the first step to derive the G_m-C filter topology, the v_{in} voltage source and the series resistor R_S are replaced by its Norton equivalent. Then, the resistors are replaced by equivalent circuits made with transconductors (see Figure 3.9) and the suspended inductor by two gyrators and a capacitor. The current source is implemented by a simple OTA with transconductance $G_m = \frac{1}{R_s} = \frac{1}{R_L} = 1$. This way, the same transconductance value is used in the OTAs that implement the resistors [29, 43].

[1]Available at http://www.coe.ufrj.br/∼acmq

Table 3.8: LC ladder prototype component values

Component	Value
R_s	1
C_1	$6.44129543522535 \times 10^{-3}$
L_2	$3.16432635907662 \times 10^{-3}$
C_3	$6.44129543522535 \times 10^{-3}$
R_L	1

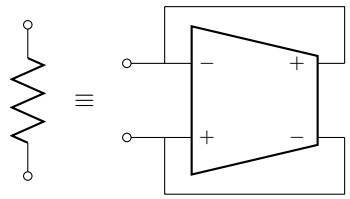


Figure 3.9: Transconductor equivalent circuit for a resistor.

A gyrator can be implemented by two transconductors connected as illustrated in Figure 3.10. To emulate a suspended inductor, two gyrators are needed such that the association gyrator/capacitor can be perceived as a suspended inductor by all the network.

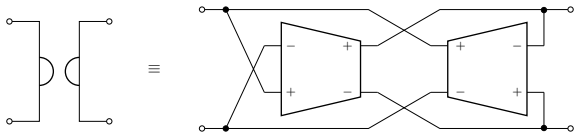


Figure 3.10: A gyrator implemented by two transconductors.

After all the substitutions, the differential G_m-C filter topology shown in Figure 3.11 is obtained. In the design, all transconductors have been chosen to present the same transconductance. This facilitates filter tuning through simultaneous adjustment of all OTA transconductances.

The transconductance and capacitance values given in Table 3.8 still need to be scaled in impedance. To do this, a transconductance value of $G_m = 40nS$ was chosen for the OTAs. With this value, the capacitances were scaled as shown in Table 3.9.

3.5.1 Operational transconductance amplifier (OTA)

The operational transconductance amplifier topology employed at the LIA output low-pass filter was the one presented in [29]. The only difference lies in the fact that current divider transistors were discarded, as it was possible to attain the desired transconductance without the current division technique. The employed topology is shown in Figure 3.12 and its biasing circuit in Figure 3.13.

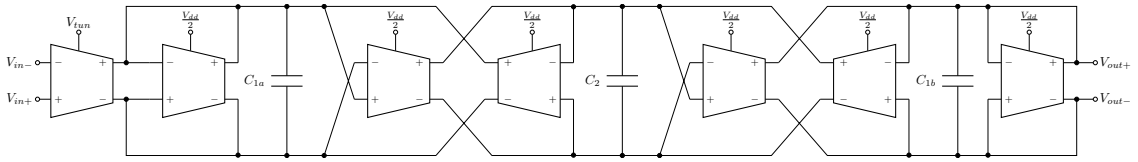


Figure 3.11: Third-order fully differential G_m-C low-pass filter. The filter gain can be adjusted by setting the first OTA transconductance through the V_{tun} voltage. The other OTA transconductances are fixed by setting the V_{tun} voltage to $\frac{V_{dd}}{2}$.

Table 3.9: Low-pass filter capacitors dimensions

Component	Type	L	W	Multiplicity	Total capacitance
C_1	dual CMIM	84.16 μm	84.16 μm	8	252.95344 pF
C_2	dual CMIM	84.16 μm	84.16 μm	4	126.47672 pF

The topology is constituted by a folded cascode amplifier with a degeneration transistor between the sources of the input differential pair transistors, to reduce transconductance and improve linearity. With the same objective, an attenuator, with a scaling factor of $1/5$, precedes each input. The common-mode rejection circuit is implemented by transistors $M_{C1} - M_{C8}$.

The filter transconductor must present an output impedance much higher than the filter time constant [29]. Otherwise, the filter quality factor would be severely degraded. To accomplish this requirement, a first attempt was to use lengthy transistors. A gate length of $5\mu m$ was adopted here and used throughout the block designs for homogeneity and, consequently, ease layout, while a quiescent current of $2\mu A$ for all branches was arbitrated. The attained output impedance was near $80M\Omega$, which was too small. The quiescent current of each amplifier branch was then reduced to $100nA$. This also has the property of increasing the output resistance, as $r_o = \frac{1}{g_{ds}} = \frac{1+\lambda V_{ds}}{\lambda I_D}$. After this, the output resistance was increased to over $10G\Omega$, which led the characteristic of the transfer function to the expected form.

Another technique used in the OTA design was to connect the bulk of the input differential pair to its source, to improve CMRR and obtain a viable transistor size, that otherwise, with current transistors bias and bulks connected to ground, would result in transistor widths larger than 1mm. Table 3.10 presents the devices dimensions of the designed OTA.

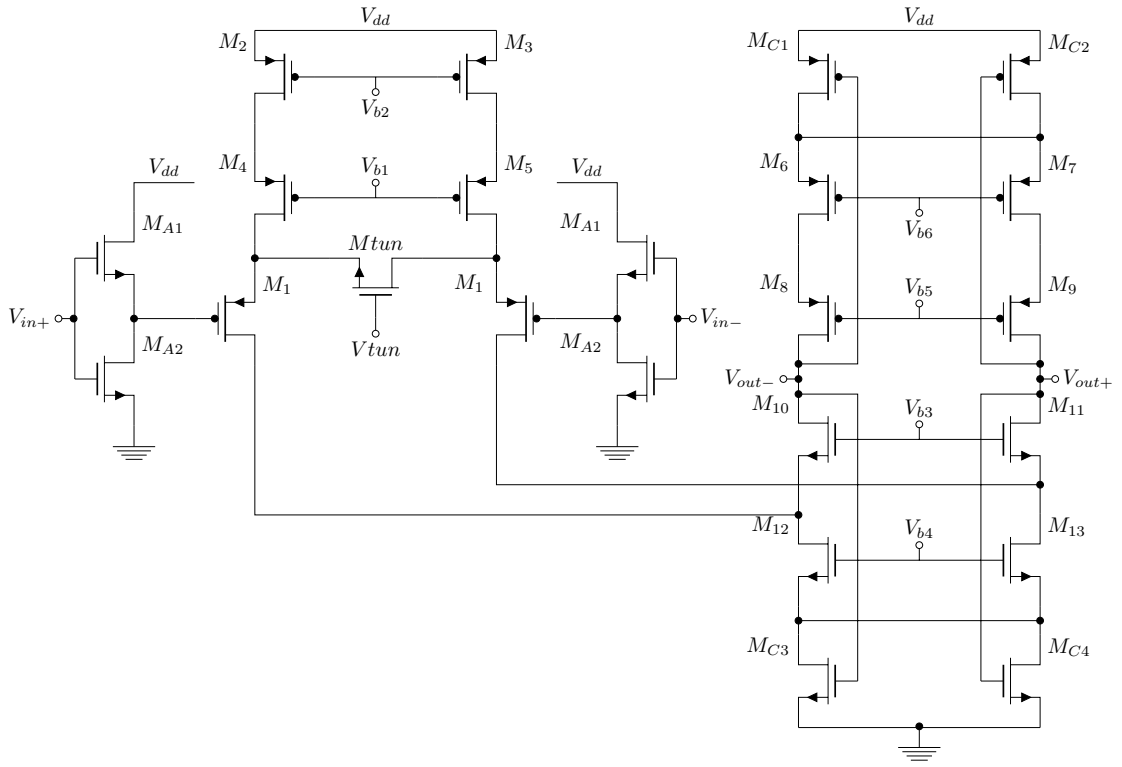


Figure 3.12: Low-pass filter OTA topology, consisting of a folded-cascode with a degeneration transistor and input attenuators.

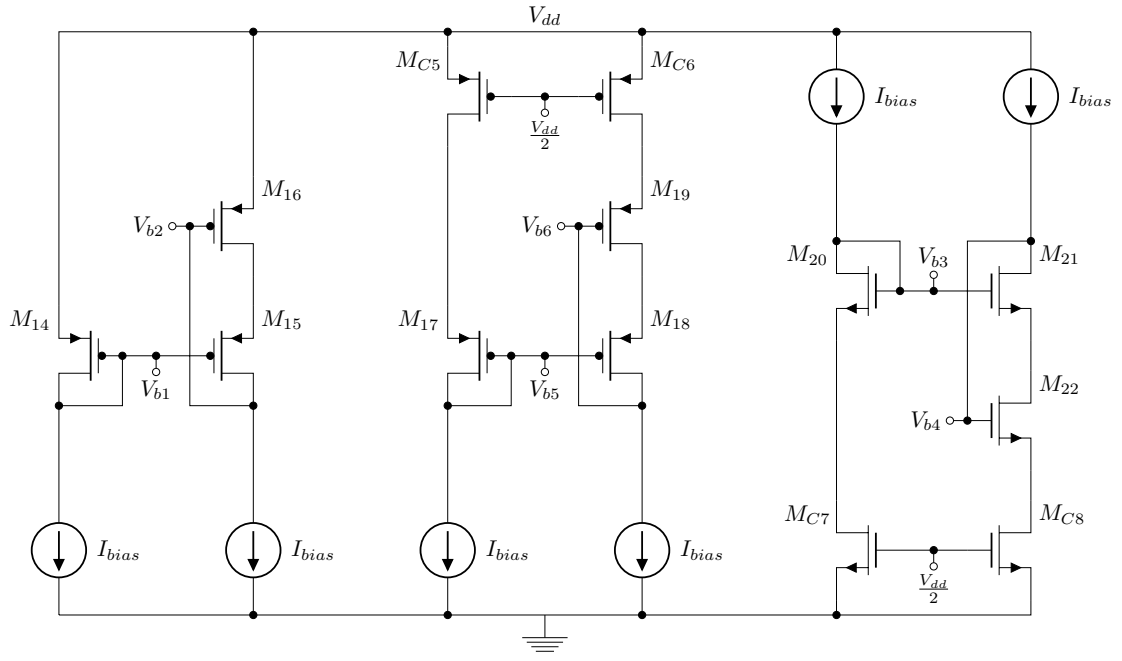


Figure 3.13: OTA bias voltages.

Table 3.10: Devices dimensions of the low-pass filter OTA

Component	Type	L	W	Multiplicity	Intended operating region
M_{A1}	*nmos*	5 μm	1 μm	1	saturation
M_{A2}	*nmos*	5 μm	1 μm	2 (parallel)	triode
M_1	*pmos*	5 μm	3.48 μm	2 (parallel)	saturation
M_2; M_3; M_4; M_5	*pmos*	5 μm	14.07 μm	1	saturation
M_6; M_7; M_8; M_9	*pmos*	5 μm	13.9 μm	1	saturation
M_{10}; M_{11}; M_{12}; M_{13}	*nmos*	5 μm	5.35 μm	2 (parallel)	saturation
M_{C1}; M_{C2}	*pmos*	5 μm	1.33 μm	1	triode
M_{C3}; M_{C4}	*nmos*	5 μm	470 nm	2 (parallel)	triode
M_{tun}	*nmos*	2.29 μm	220 nm	1	triode
M_{14}	*pmos*	5 μm	5.68 μm	8 (series)	saturation
M_{15}; M_{16}	*pmos*	5 μm	14.07 μm	1	saturation
M_{17}	*pmos*	5 μm	3.98 μm	8 (series)	saturation
M_{18}; M_{19}	*pmos*	5 μm	13.9 μm	1	saturation
M_{C5}; M_{C6}	*pmos*	5 μm	1.33 μm	1	triode
M_{20}	*nmos*	5 μm	2.72 μm	8 (series)	saturation
M_{21}	*nmos*	5 μm	5.35 μm	2 (parallel)	saturation
M_{22}	*nmos*	5 μm	5.35 μm	1	saturation
M_{C7}; M_{C8}	*nmos*	5 μm	470 nm	1	triode

Chapter 4

Layout

The layout is the lowest level of abstraction in the design of an integrated circuit. Based on the layout the electronic design automation (EDA) software generates the masks that are used by the foundry in the photolithography step of the manufacturing process. It is at this stage that the circuit geometric pattern is recorded on the wafer. One or more masks are used for recording, for example, the *nwell*, gate oxide, diffusion areas, polysilicon, capacitor dielectric, etc.

The manufacturing process of an IC is a complex task, and despite the fact that this process is well controlled so as to assure the quality of the fabricated components, various effects, classified as process variations and systematic and random variations, cause the effective sizes and electrical properties of components to differ from the intended ones and to fluctuate from component to component. These fluctuations can cause the circuit performance to deviate drastically from its intended nominal performance.

To evaluate the impact of such effects on circuit performances, a Monte Carlo analysis should be performed. This analysis gives us an estimation of the yield of the design.

In parallel with yield performance, there is still a concern with the reliability of the fabricated circuit. To assure a good reliability, the foundry defines design rules that should be followed. For illustration, these rules comprise, among many others, the minimum metal to metal distance, so as to avoid short circuits during wafer processing; minimum and maximum metal and polysilicon area coverage, that impact the performance of the chemical-mechanical polishing (CMP); reactive ion etching (RIE); and lithographic processing steps.

The EDA software tools used in the design enables to check if all design rules defined by the foundry were followed (DRC, antenna and pattern desinty verifications) and to check if the layout completely matches the respective circuit schematic (LVS verification). After successfully completing all checks, the designer can extract the components and interconnection parasitics based on the finished layout, and incor-

porates these parasitics in simulations to obtain a more accurate analysis of circuit operation and performance.

The employed layout techniques are briefly explained in Section 4.1. The physical layout of the various blocks that constitute the lock-in amplifier system are presented in the sections that follow. All layouts have its parasitics extracted (calculated) in order to obtain a more realistic simulation of the behavior of the system (see Chapter 5). The developed layout is sent for fabrication in an MPW prototyping service. For debugging purposes, the layout of some system building blocks is sent along with the system complete layout. These debugging blocks share the same power and ground rails, but the LIA system does not share any rail or port with any other block.

4.1 Layout techniques

The performance of certain circuits as current sources and differential pairs are extremely dependent on the matching of its devices. While the mismatch due to random variations can be statistically modeled and considered in circuit sizing, the mismatch due to systematic variations can be mitigated through some layout techniques.

In this work, the following techniques were considered in the layout of system blocks:

- matched components were drawn as close as possible one another, so as to reduce the influence of process and temperature gradients;
- matched elements were arranged with an aspect ratio as close as possible to 1, for the same reason as above;
- matched components were positioned with the same orientation, so as both were subjected to the same systematic errors;
- components were divided into smaller parts (called unitary elements) with equal dimensions that could be associated in series and/or parallel so as to reduce random variations and gate resistance;
- unitary elements of matched components were arranged in an interdigitated and/or common-centroid geometry, so as to mitigate process and temperature problems, and possibly, systematic errors due to wafer processing;
- parasitic effects over matched components interconnects were equalized, so as to no give rise to signal propagation problems, such as phase mismatch of differential signals (this is more critical in RF circuits);

- a large number of contacts were used whenever possible to improve reliability and reduce interconnection parasitics;
- source/drain diffusion areas of matched devices were shared to reduce junction capacitance.

Another common technique is the placement of dummy components at the outside borders of matched devices, so as to replicate the environment at the inner borders. This technique intends to reduce systematic errors that can arise due to the idiosyncrasies of the manufacturing process. However, the dummy component should be tied to a node to avoid charge build up during the ion etching manufacturing step and, as source/drain diffusion areas were shared, this ended to force the dummy to be tied to a circuit node, instead of to the ground or to the power supply. This procedure would result in adding parasitics to circuit nodes, that could cause a circuit misbehavior. Hence, dummy devices were not used.

The current density at all nodes in the system is small enough to always allows the use of minimum width metal paths. However, when relevant, the paths were enlarged to ensue the insertion of a greater number of *vias* or contacts.

4.2 Transimpedance amplifier

The transimpedance amplifier (Figure 4.1) is composed by four instances of the op amp cell (Figure 4.2), disposed as in schematic diagram (Figure 3.5).

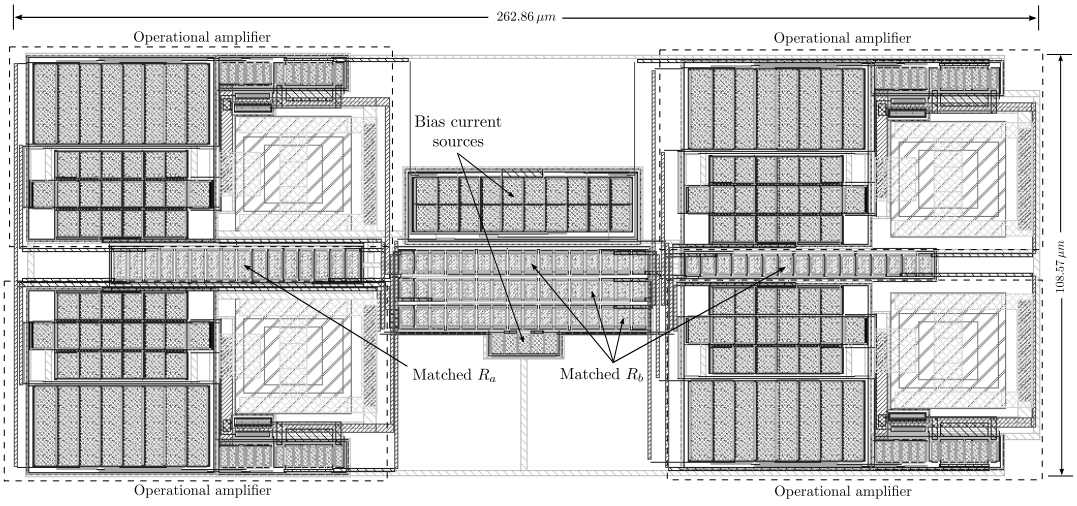


Figure 4.1: Transimpedance amplifier layout.

Five resistance pairs should be matched so as to ensure the advantages brought by the differential topology. To match each pair, they were divided into eight smaller parts (see Table 3.4) and laid out in an interdigitated pattern such as AABBAABBBAABBAABB. The placement of matched resistances is shown in Figure 4.1.

The NMOS and PMOS bias current sources are placed between the op amps, so as to reduce the distance the bias current should travel to reach each op amp.

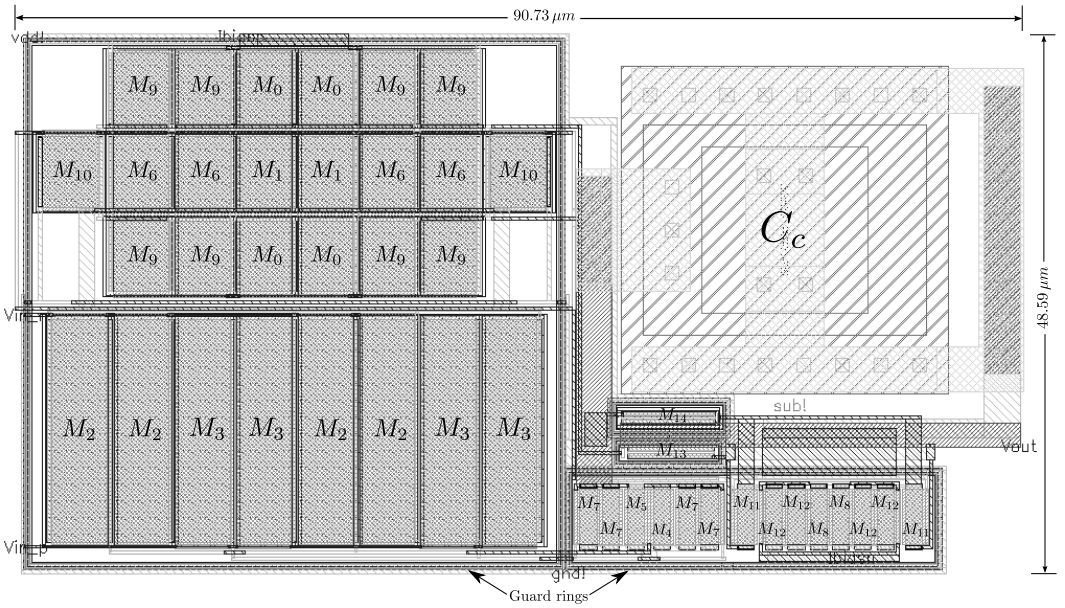


Figure 4.2: Operational amplifier layout.

The operational amplifier that constitutes the transimpedance amplifier is shown in Figure 4.2. It can be perceived that the PMOS differential pair transistors, $M_{2,3}$, occupies a large area and are arranged in an interdigitation pattern, sharing source and drain diffusions. They lie below PMOS current mirrors transistors $M_{0,1}$ that sources currents to the differential pair, to transistor M_6, that works as an active load to the op amp second stage NMOS transistor M_7, and to the $M_{9,10}$ push-pull transistors. As all these transistor gates, except for M_{10}, are connected together, they were laid out in a common-centroid configuration to improve threshold voltage (V_t) matching and, consequently, the current copying accuracy. They share source and drain areas, except for the M_{10} transistor. Yet, it was positioned so as to form a regular geometry, despite not being to be matched with the other transistors. All these PMOS transistors were wrapped by a sole guard ring connected to the power supply. The guard ring protects against latch-up and substrate noise.

The NMOS current mirror, $M_{4,5}$, was placed beside the differential pair transistors, matched with the second stage NMOS transistor M_7 in common-centroid. The transistors were rotated by ninety degrees so that its gate length was vertically oriented to obtain a better aspect ratio.

The NMOS push-pull transistors, $M_{8,11,12}$, were placed beside the other NMOS transistors and arranged in the same manner. All the above mentioned NMOS transistors are surrounded by a sole guard ring.

The compensation capacitor C_C was placed above the NMOS transistors so as to obtain a regular geometry for the whole amplifier layout. The output transistors

$M_{13,14}$ were wrapped, each one, in a guard ring and placed in the space between the compensation capacitor and the NMOS transistors. The capacitor lying on the upper metal layers was not placed over the other circuit elements to avoid parasitics that could affect circuit performance.

4.3 Mixer

The mixer layout is displayed in Figure 4.3. It can be seen that the Gilbert Cell differential pairs $M_{2,3}$, $M_{4,5}$ and $M_{6,7}$ were disposed in a common-centroid configuration. They share the source diffusion area, as their sources are connected to the same node. The current mirrors composed by FETs M_0, M_1, M_{10} and M_{11} are also disposed in a common-centroid configuration, but transistors orientation were rotated by 90 degrees, so as to produce a better aspect ratio, and make the sources oriented downwards, so as to ease the interconnection with the ground rail. This way, all gates are connected together with a single poly strip, and the contacts are made at the extremities.

The PMOS, $M_{8,9}$, are laid out following the same principles, but its sources are oriented upwards, to enable the interconnection with the power rail.

Transistors $M_{12,13}$ from the level-shifter, were divided into two parts, each one placed at one of the sides of the Gilbert cell RF input differential pair, so as to generate a compact cell layout. Despite being apart, the transistors have a common-centroid configuration and share the same drain diffusion areas.

4.4 Low-pass filter

The third-order Chebyshev low-pass filter layout is presented in Figure 4.4. It is composed by seven transconductor cells, seen in the figure positioned in a row above the filter capacitances, that occupies the majority of the area. Bias generating circuits were placed near the center of the row to reduce the parasitic effects on the value of bias voltages distributed to all OTAs, due to the distance between each OTA and the bias generating circuit. The layout of a transconductor cell is shown in Figure 4.5.

The filter capacitors were divided into smaller instances to enable a common-centroid arrangement. The number and size of instances were chosen to obtain a regular geometry and a good aspect ratio for the module layout.

A difficulty in this layout was to place and connect the PMOS transistors of the differential pair ($M_{1a,1b}$), that have its bulk connected to its source. Each transistor was divided into two smaller ones, so as to enable a common-centroid placement. Each device was then enclosed by a guard ring and the source and bulk (*nwell*) was

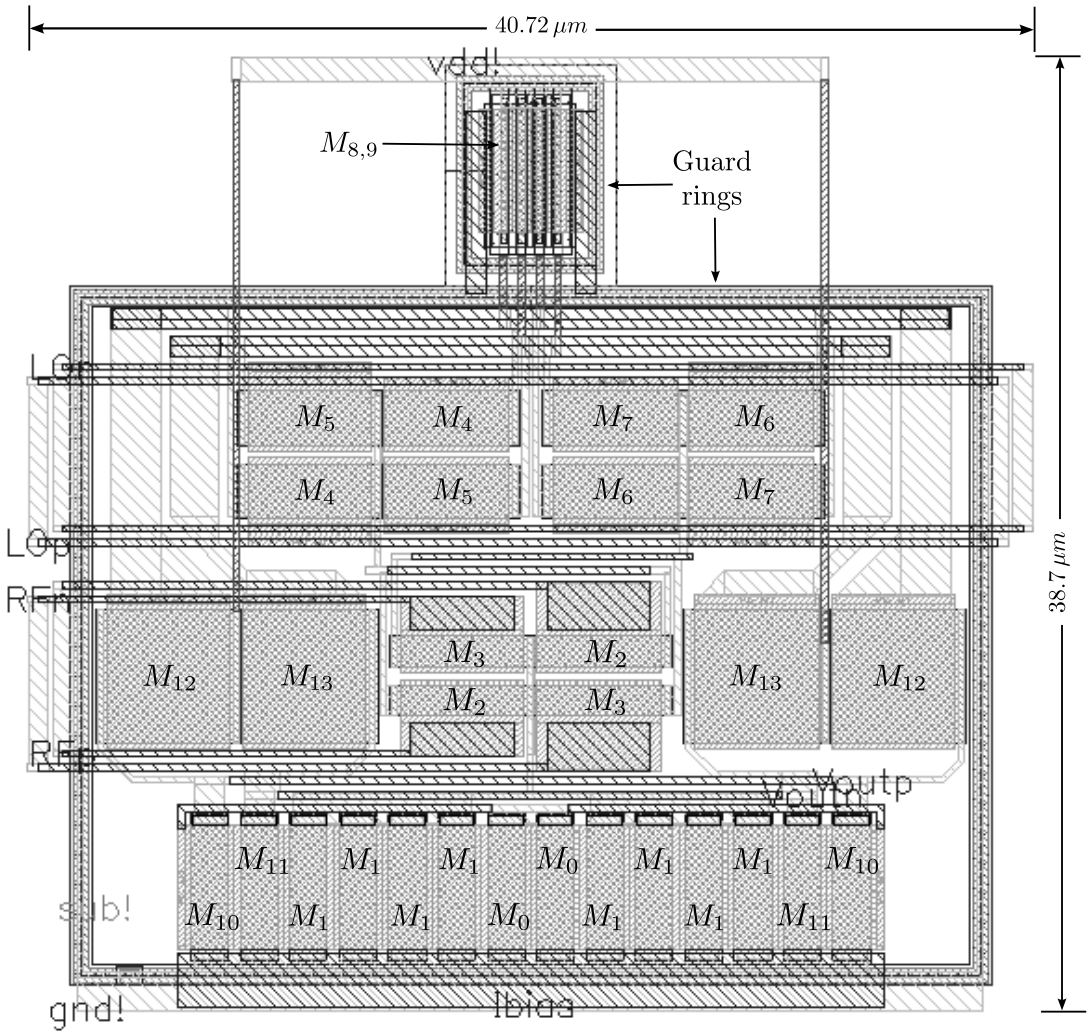


Figure 4.3: Mixer layout.

connected through it. To avoid latch-up, another guard ring, connecting the wafer substrate to the power ground, was placed around each transistor *nwell*. This also assured a proper spacing between the *nwells*.

The attenuators ($M_{A1,A2}$) must match, and should be put close together, but each one was placed in one side of the differential pair, so as to make the connections between the attenuators and the transistor gates of equal length. The cascode NMOS transistors (M_{10-13}) were placed in a common-centroid configuration, sharing source and drain diffusion areas. PMOS transistors $M_{4,5}$ and $M_{8,9}$ of the differential pair current source and cascode, should be matched, but ended up getting away from each other to share diffusion areas. Common-mode rejection circuit transistors, M_{C1-C4}, were rotated by 90 degrees and placed below and above cascode transistors, to enable equal length connections to other parts of the circuit.

All PMOS transistor share a common *nwell* and are surrounded by a guard ring. Another guard ring wraps the differential pair and NMOS transistors.

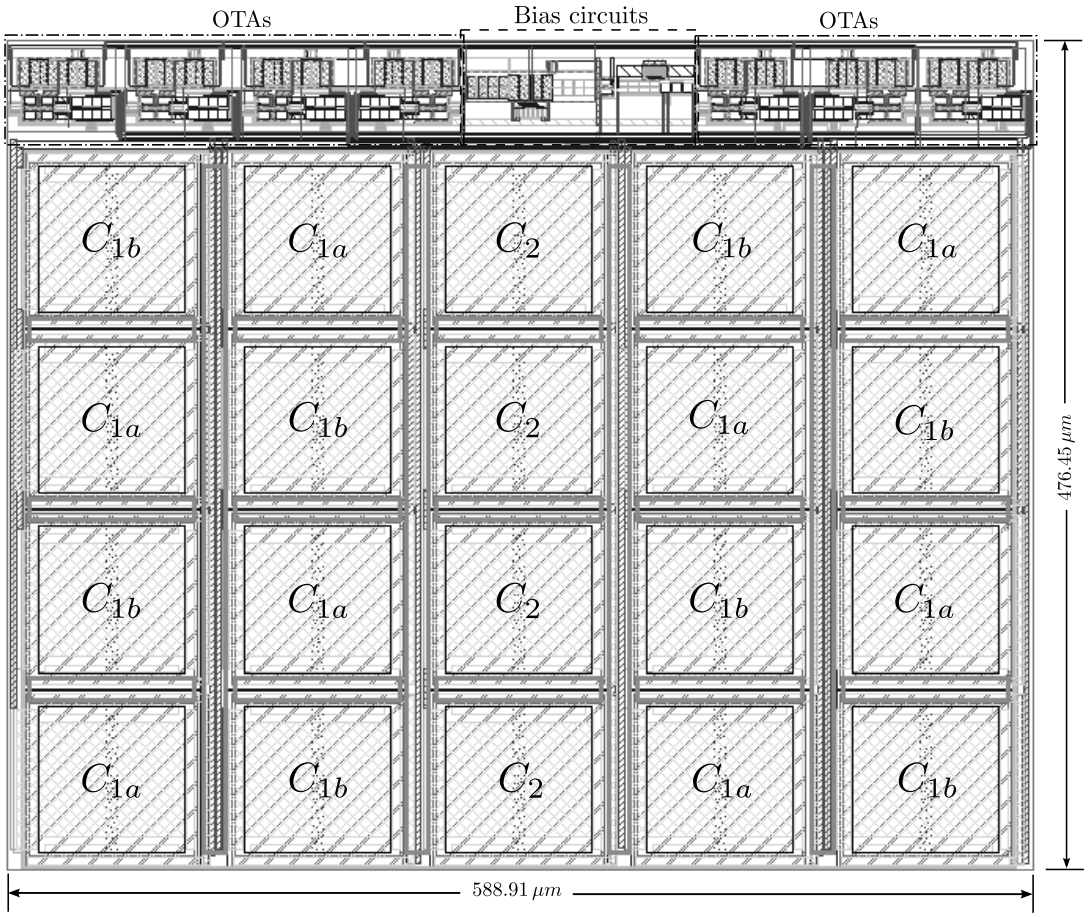


Figure 4.4: Low-pass filter layout.

Degeneration transistor M_{tun} was placed above the differential pair to ease interconnection.

4.5 Lock-in amplifier

The complete lock-in amplifier layout is shown in Figure 4.6, where, as can be seen, the output low-pass filter capacitors occupy most of the area, with the low-pass filter of the DC photocurrent rejection circuit lying beside it. The differential pair responsible for draining the DC photocurrent is placed above this filter in an AABBAABB interdigitated pattern, thereby sharing diffusion areas. Above the differential pair lie the transimpedance amplifier, the mixer and the output low-pass filter, with the PMOS and NMOS bias current mirrors, respectively, above and below the mixer.

A larger view of the layout of the OTA used in the DC photocurrent rejection circuit is shown in Figure 4.7. The NMOS current mirrors (M_{2-7}) are placed at the bottom, near the ground rail, with transistors length oriented vertically so that a better aspect ratio could be obtained.

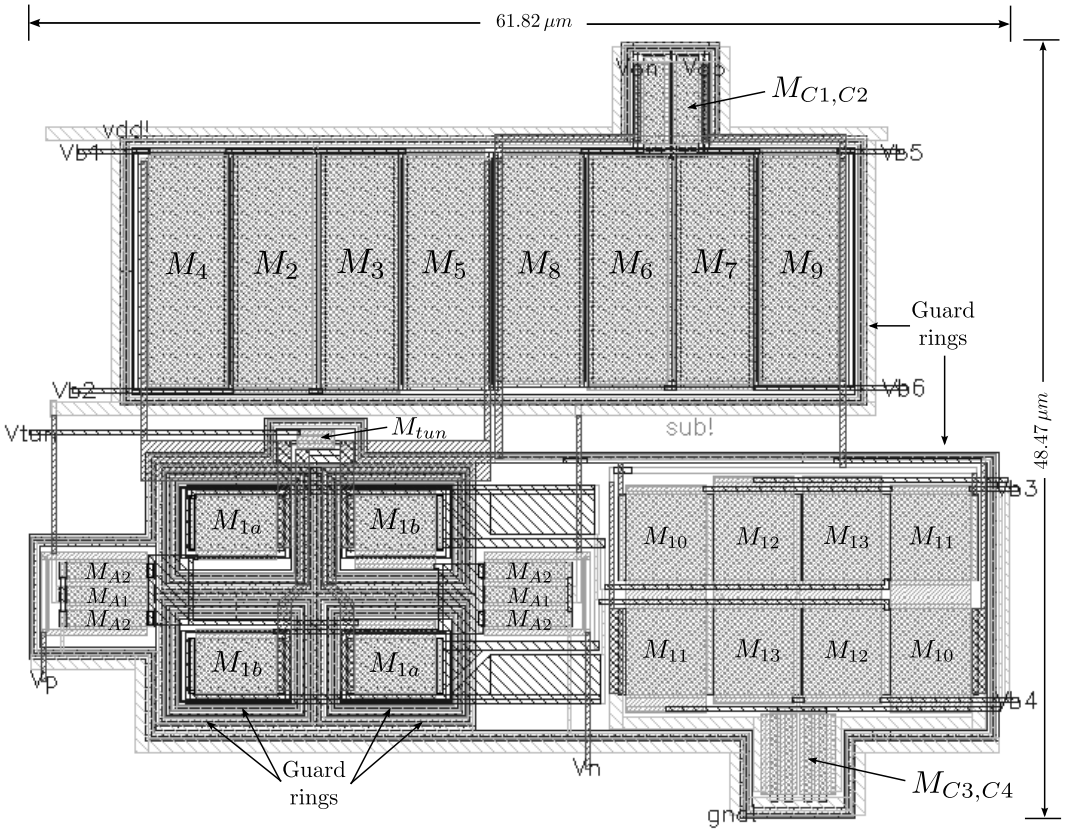


Figure 4.5: Low-pass filter OTA layout.

The attenuators are placed above the current mirrors and a single guard ring encloses both the current mirrors, the attenuators and the degeneration transistor M_{tun}.

The differential pair is arranged in a common-centroid configuration with the current sources above it. The PMOS current mirrors lie one at each side of the current sources. The transistors of both, the current source and current mirrors have their channel length oriented vertically, with the current mirrors placed in an ABBAABBAABBAABBA pattern to simplify interconnections.

A circuit to generate a constant voltage to the degeneration transistor is placed at the right, outside the guard rings that enclose both the NMOS and PMOS transistors, wrapped in its own guard ring.

4.6 Integrated circuit

The layout of the entire integrated circuit sent to fabrication is shown in Figure 4.8. The lock-in amplifier can be seen on the upper left corner, while some blocks (mixer, Miller operational amplifier, transimpedance amplifier and low-pass filter) are distributed over the top and top-right regions of the chip.

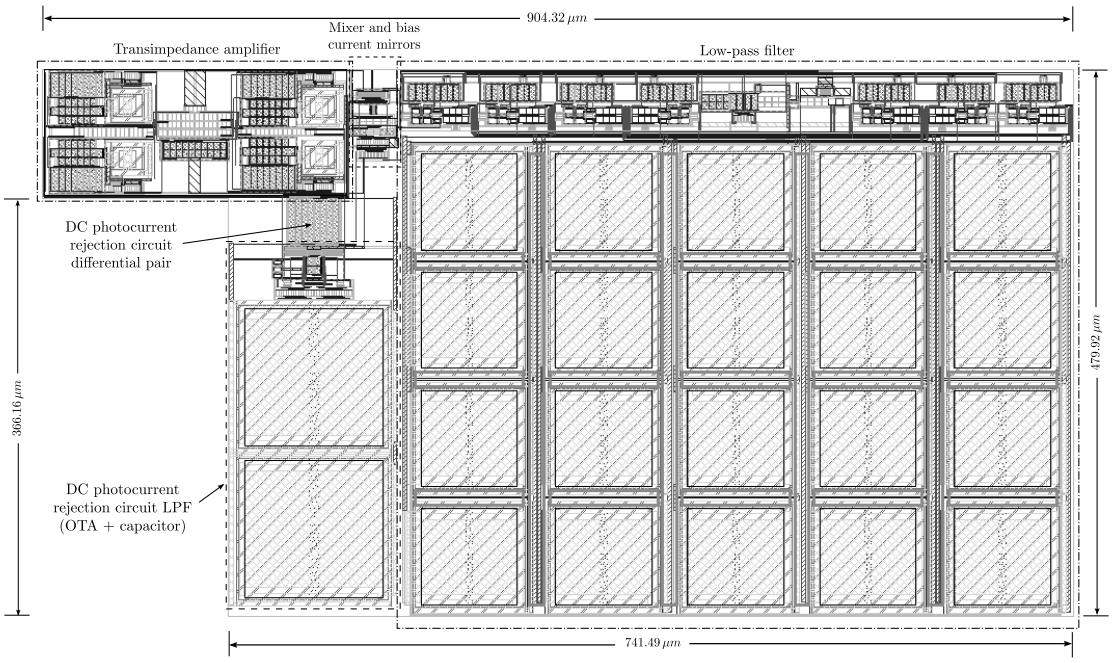


Figure 4.6: Complete lock-in amplifier layout.

The chip occupies the minimum area allowed by the prototyping service. Chip guard-ring and pad ring are within this area. Other projects, voltage references and digital filters, share the fabrication run.

Ground connection is common to all circuits in the wafer and is distributed from the pad at the middle of the row of pads at the bottom of the chip, identified with the number 1. An exclusive pad is used to power the pad ring, this pad is identified by the number 64. Each circuit or set of related circuits are also powered by exclusive power sources connected through an I/O pad. In such way, each circuit (or set of circuits) can be independently switched on or off and its power consumption could be measured at the bench. The disadvantage of not powering on circuits is that the *nwell* rings are left unbiased, which could give rise to latchup.

The package used for encapsulating the integrated circuit was the JLCC84 (84 pins). Each pad of the IC is associated with a package pin. In addition to the ground (pin 1) and the pad-ring power (pin 64), the pins listed in Table 4.1 are associated with the lock-in amplifier.

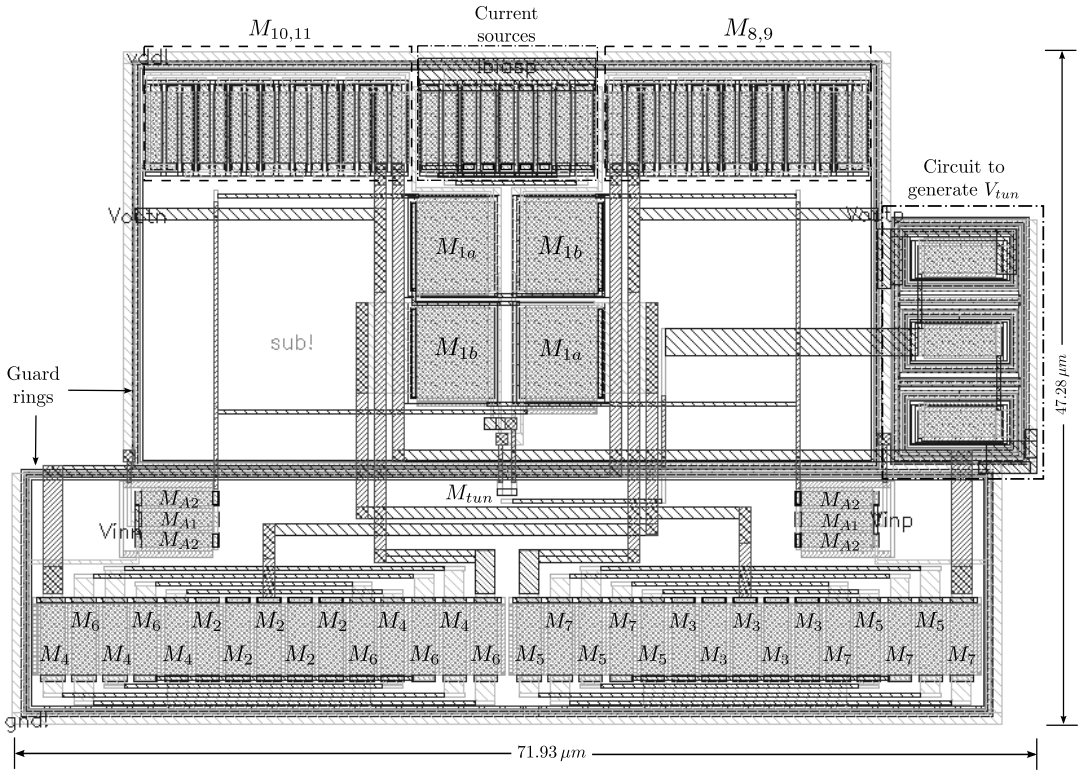


Figure 4.7: DC photocurrent rejection circuit OTA layout.

Table 4.1: Integrated circuit pins mapping

Pin number	Pin description
54	LIA power supply (1.8V)
55	photodiode cathode
56	photodiode anode
57	LIA common-mode voltage (0.9V)
58	reference signal positive terminal (1.2V common-mode voltage)
59	reference signal negative terminal (1.2V common-mode voltage)
60	LIA bias current (1μA)
61	demodulator low-pass filter gain adjustment
62	LIA output negative terminal
63	LIA output positive terminal

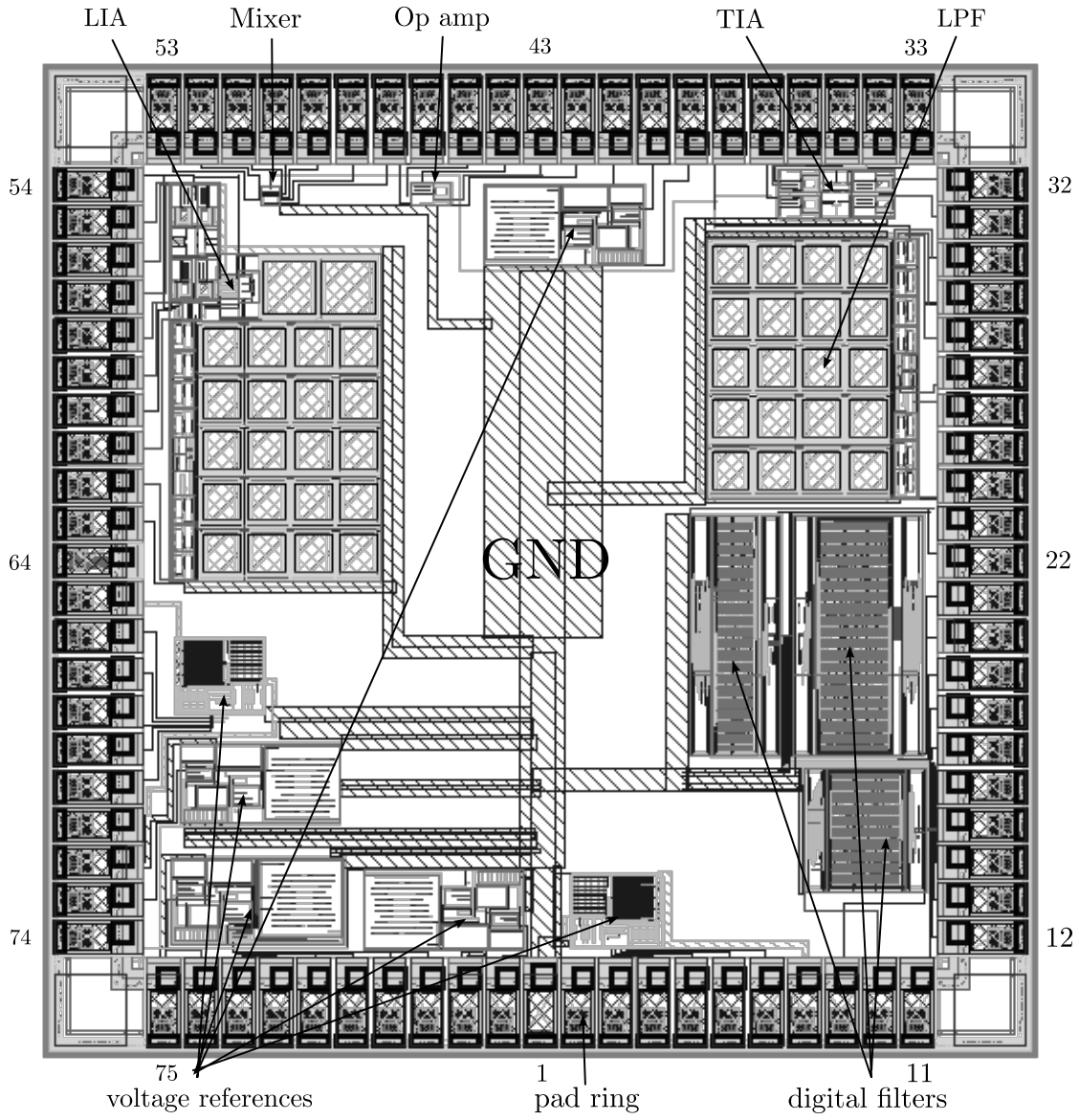


Figure 4.8: Integrated circuit sent to fabrication.

Chapter 5

Simulation Results

To evaluate the operation and performance of the lock-in amplifier and its building blocks, testbenchs were created for each desired test. The more relevant results are presented in this chapter.

All results presented are from simulations made over the parasitics extracted layouts using the Cadence tools[1]. The technology used was the AMS H18A6 [33] (0.18 μm minimum feature and 6 levels of metals) and the respective process design kit (PDK) was furnished by the CMP prototyping service [44]. The PDK employs the PSP compact MOSFET model [32] to represent the low-voltage devices used in this project.

Monte Carlo simulations, unless stated otherwise, considers both mismatch and process parameter variations.

5.1 Transimpedance amplifier

Figure 5.1 shows the transimpedance amplifier frequency response. The analysis confirms the gain predicted in Section 3.3 by Equation 3.5 up to a frequency of 10 kHz, which is enough to amplify the input 200 Hz signal.

The transimpedance amplifier is within a loop formed by a feedback path that senses and reject the input DC photocurrent. This feedback modifies the amplifier frequency response, as shown in Figure 5.2a, attenuating the components of the input current signal at frequencies roughly below 200 Hz and amplifying to 20 kΩ the components above this frequency and extending to roughly 10 kHz, from where the signal components start to be attenuated again.

From Figure 5.2b it can be observed that, in view of the large number of Monte Carlo simulation runs ($N = 1000$), a few samples were unable to reject the DC photocurrent, and others presented deviations in the frequency response. Recurring to

[1]Industrial-grade set of software tools for the development of IC designs.

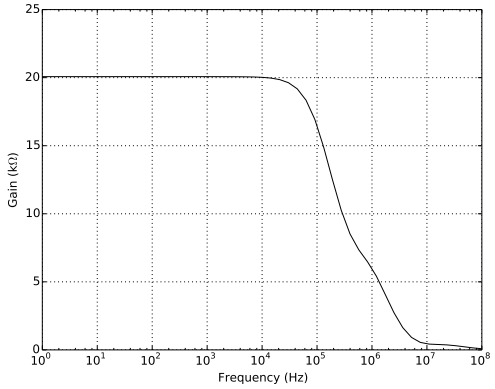
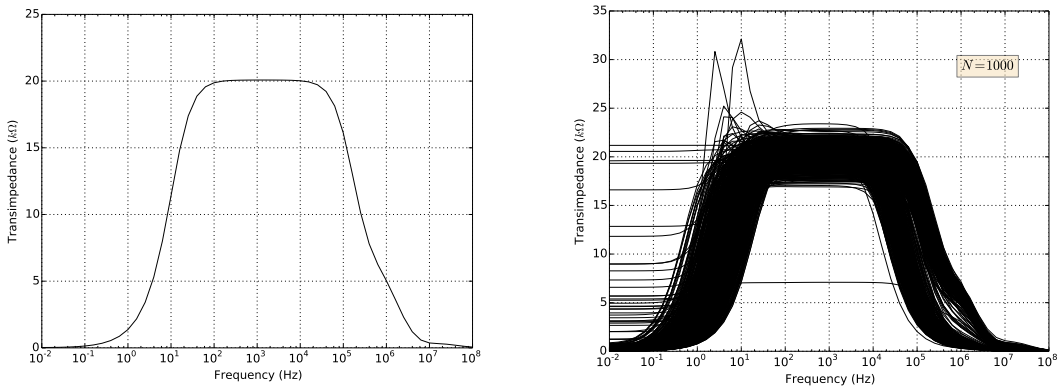


Figure 5.1: Transimpedance amplifier frequency response.



(a) (b)

Figure 5.2: Nominal (a) and Monte Carlo (b) simulation of the TIA frequency response within the DC photocurrent rejection circuit loop.

Equation 3.4, the variation in the gain value can be explained by the transimpedance amplifier gain susceptibility to process variations, while the deviation from expectation of some frequency responses is probably due to, also, transistors $M_{1,2}$ and OTA transconductances susceptibility to process variations and the association of these values in a more complex way.

For a Monte Carlo analysis, from the confidence levels expressed in Table 5.1, the following expressions [45] could be used to determine the error margin and the number of Monte Carlo simulations needed for a desired confidence level and error margin.

$$e = \frac{z}{2\sqrt{N}} \tag{5.1}$$

$$N = \left(\frac{z}{2e}\right)^2 \tag{5.2}$$

where e is the error margin, N is the sample size, that is, the number of Monte

Carlo runs and z is a variable related to the confidence level, as given in Table 5.1.

Table 5.1: Parameter value for the computation of the margin of error

z	Confidence level
1.96	95%
2.58	99%
3.29	99.9%

The linearity of the transimpedance amplifier can be measured by its total harmonic distortion (THD) if the frequency of the signal used in the analysis enables the consideration of a reasonable number of harmonics without attenuation due to its frequency response. Considering the frequency response shown in Figure 5.2a, it was adopted a frequency of 200 Hz for the input sine wave signal used in the analysis. This way, all harmonics, till roughly 10 kHz, would pass through the amplifier without attenuation, enough to make the analysis representative of the amplifier linearity. The input signal amplitude was swept from 1 nA to 15 μA in 50 linear steps and the THD values were ploted in Figure 5.3, connected by straight lines.

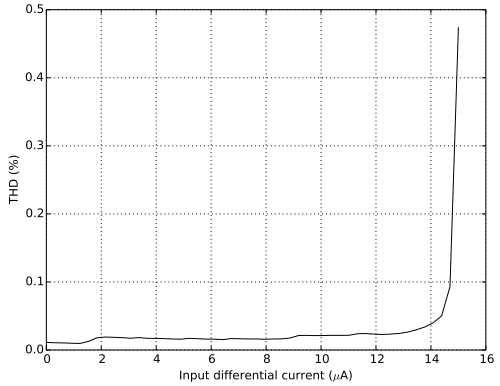
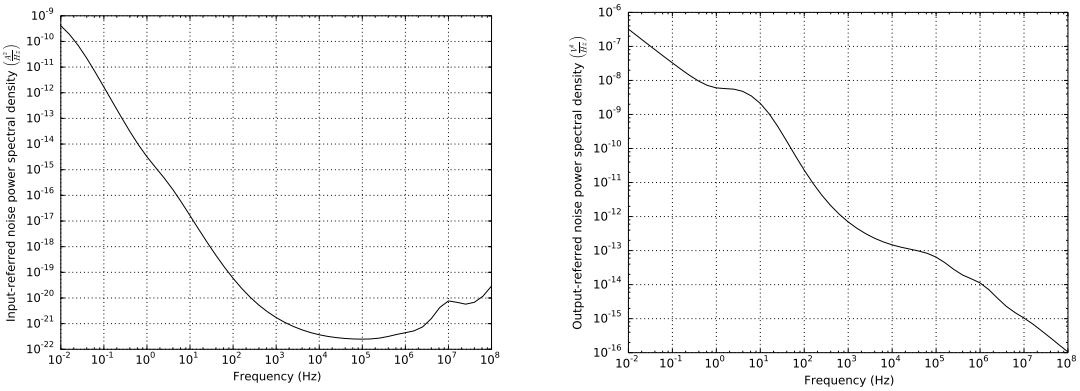


Figure 5.3: Transimpedance amplifier THD.

It can be seen in Figure 5.3 that after an input amplitude of 14 μA the THD rises exponentially. This means that this value can be considered a limit to the maximum current value that can be accepted at the input without incurring in great signal distortion. Considering the DC photocurrent rejection circuit capability, the input photocurrent should be limited to a DC value of 10 μA superimposed by an AC value of 14 μA.

Taking the maximum value for the input photocurrent amplitude, the transimpedance amplifier generates an output voltage signal with amplitude near 300 mV. This is the maximum signal amplitude that can be applied to the RF input of the mixer to guaranty that the transistors of the input mixer differential pair operate in saturation region.

Figure 5.4a and 5.4b shows, respectively, the input- and output-referred noise power spectral densities of the circuit composed by the transimpedance amplifier and the feedback path for the rejection of the DC photocurrent. At 200 Hz, the input-referred noise amplitude spectral density is 128.3 $pA/\sqrt{Hz}$, and the output-referred noise amplitude spectral density is 2.568 $\mu V/\sqrt{Hz}$.



(a) (b)

Figure 5.4: Input-referred (a) and output-referred (b) noise spectral densities of the TIA, taking on account the feedback path for the rejection of the DC photocurrent.

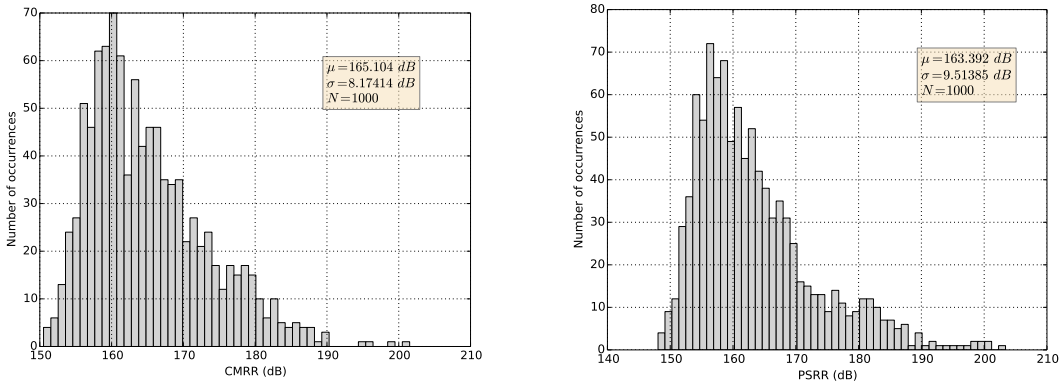
As the linearity gives a measure of the maximum signal amplitude that a circuit can accept, and the noise the minimum signal amplitude that it can distinguish, the THD and the noise spectral density are used to inform about the circuit dynamic range.

The fully-differential structure of the transimpedance amplifier is known to present very good common-mode and power-supply rejection ratios, respectively known as CMRR and PSRR. Figure 5.5 shows the values for the CMRR and PSRR obtained from a thousand runs of a Monte Carlo simulation.

In this work, the CMRR is considered as the ratio between the transimpedance differential gain and the common-mode gain, and the PSRR as the transimpedance differential gain divided by the gain from the power supply to the output [25]. The CMRR indicates the circuit capacity of rejecting common-mode signals, and should be as high as possible. PSRR is an important measure of the circuit ability to reject power supply noise, which is particularly important when the circuit shares the power supply with a noisy digital part.

5.2 Mixer

The mixer gain as a function of frequency, for an LO amplitude of 100 mV peak is shown in Figure 5.6. It can be seen that the gain characteristic is flat until almost 10 kHz, not influencing input signal processing.



(a) (b)

Figure 5.5: Monte Carlo simulations showing the CMRR (a) and PSRR (b) values for the TIA.

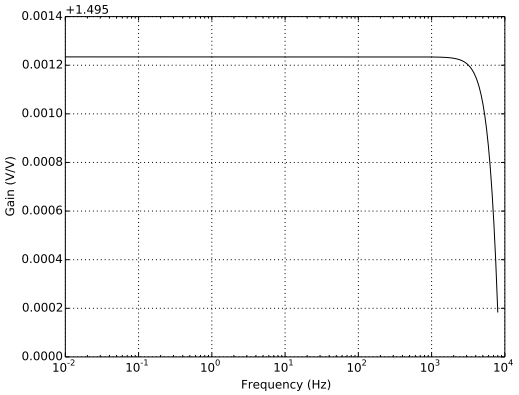
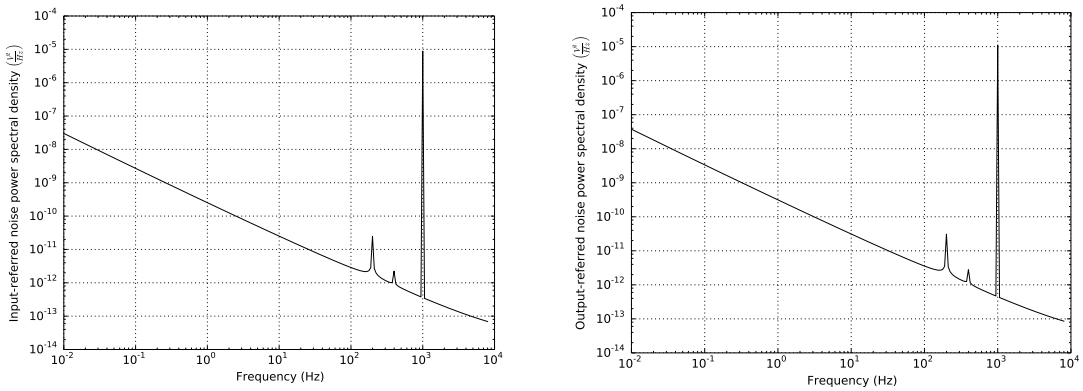


Figure 5.6: Mixer gain as a function of frequency.

Figure 5.7 shows, respectively, the mixer input- and output-referred noise. The graphs are almost identical, as the input noise is computed by dividing the output noise by the gain, and the mixer gain is near unity.

The peaks seen in the plots are due to intermodulation effects, whereby the noise signal is multiplied by the harmonics of the input signal that leak through the mixer. The peak at 1 kHz, clearly visible as this point, is exactly one of the simulation steps. The peaks at 200 and 400 kHz are smaller because simulation stepped very near, but not exactly over these harmonics. Peaks at 600 and 800 kHz harmonics could not be seen as the simulation did not step so close to them.

Intermodulation is inevitable in any process which depends on a non-linear operation. On high input signal-to-noise ratios the effect does not cause problems, but at low signal-to-noise ratios the intermodulation products can dominate and give rise to the phenomenon of threshold or signal suppression, which corresponds to a loss of information in that the detector output no longer contains a term which is simply proportional to the desired modulation [23].



(a) (b)

Figure 5.7: Input-referred (a) and output-referred (b) noise spectral density of the mixer.

Traditional small signal analysis to compute noise and gain do not apply to mixers, as they have a time varying operating point. Gain and noise simulations of the mixer were carried out using specialized analysis, namely the PSS (periodic steady state) and PNOISE (periodic noise). The PSS calculates the steady state response with a time varying periodic input, and PNOISE performs the small signal analysis based on the periodic operating point to compute noise and gain of the circuit.

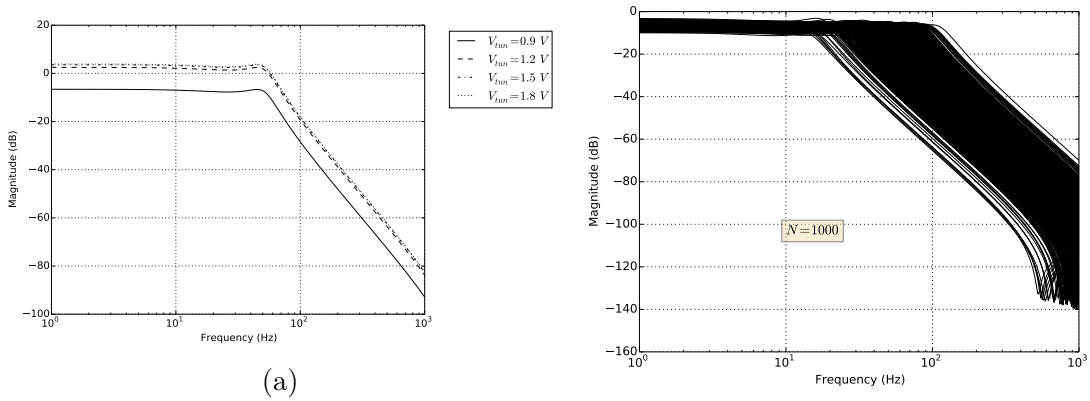
5.3 Low-pass filter

The low-pass filter frequency response is shown in Figure 5.8a for different values of V_{tun}. Figure 5.8b shows Monte Carlo simulations for a thousand runs of the frequency response of the lock-in amplifier output low-pass filter. The V_{tun} voltage is generated by a string of two diode connected PMOS transistors between the power supply and ground.

The filter cutoff frequency is dependent on the OTAs transconductance, and the large variation seen in the cutoff frequency shown in Figure 5.8b is due to the susceptibility of the OTAs transconductance to process variations, while the variation in the magnitude frequency response is basically due to the mismatch between the transconductance of the filter OTAs.

Despite the wide variation in frequency response, in the worst case the filter will attenuate in more than 40 dB all components from 400 Hz upward and, in the better case, the cutoff frequency will be lowered to frequencies as low as 20 Hz, generating an even better higher harmonics attenuation.

As mentioned previously, a cutoff frequency tunning scheme was not implemented in this prototype, but one such scheme is essential to allow the filter to have a cutoff



(a) (b)

Figure 5.8: Nominal frequency response of the LPF for different values of V_{tun} (a) and Monte Carlo simulation of the LPF frequency response for $V_{tun} = 0.9\,V$ (b).

Table 5.2: Filter low-frequency poles

	Real part (Hz)	Imaginary part (Hz)	Quality factor
Pole 1	-25.89	0.0	0.5
Pole 2	-12.96	50.08	1.995
Pole 3	-12.96	-50.08	1.995

frequency equal to the bandwidth of the signal of interest. In such condition the system will be performing as better as possible.

A pole-zero analysis confirms the stability of the filter, as no pole lie in the right half plane. The low-frequency poles for the unloaded filter block are registered in table 5.2:

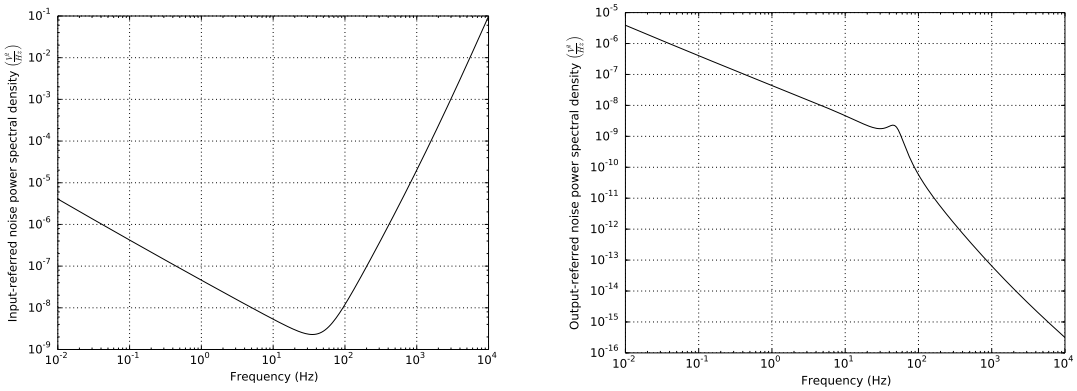
Plots of the input- and output-referred noise of the low-pass filter are shown in Figure 5.9. The input-referred noise shows an increase after the filter cutoff frequency due to the fact that, after this frequency, the filter gain drops faster than does the output noise.

The total harmonic distortion as a function of the input differential voltage for the low-pass filter is pictured in Figure 5.10. It shows that the filter has a high linear input range.

5.4 Lock-in amplifier

The gain of the lock-in amplifier as a function of the frequency is pictured in Figure 5.11. The plot presents a characteristic similar to that of the output low-pass filter, and shows that signals up to 50 Hz are amplified by almost 80 dbΩ, while presenting an attenuating factor above this frequency of nearly 60 dBΩ/decade.

The Input- and output-referred noise of the lock-in amplifier is presented in



(a) (b)

Figure 5.9: Input-referred (a) and output-referred (b) noise spectral density of the low-pass filter.

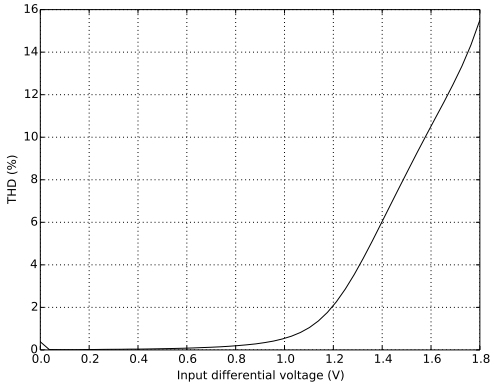


Figure 5.10: Low-pass filter THD.

Figure 5.12. Its characteristic is similar to that of the output low-pass filter, but presents a peak at 1 kHz due to the inevitably intermodulation effect to which the mixer is subject, as explained in Section 5.2.

Table 5.3 lists, in chronological order, some characteristics and performances of the various analog integrated lock-in amplifiers found in the literature. The characteristics and simulated performance of the prototype developed in this work is listed at the last line and can be compared to the previous works.

Care must be taken when comparing such results, as various designs did not implement some components or blocks on-chip and, probably, did not consider their influences of such components on the system overall performance. The frequency at which the systems were designed to work will also dictate their performances, e.g. systems designed to work at high frequencies, will have a higher power dissipation.

All the works in the literature announce the input-referred noise of the input amplifier as the input-referred noise of the whole lock-in amplifier, without considering the frequency translation performed by the mixer. In Table 5.3 both values

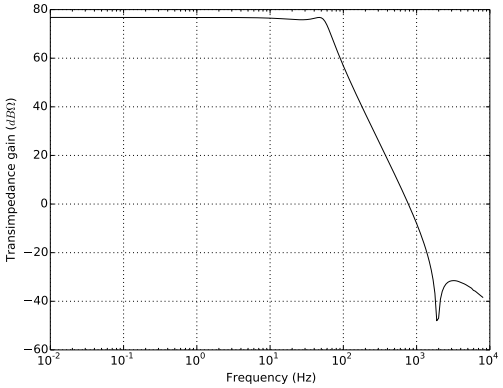
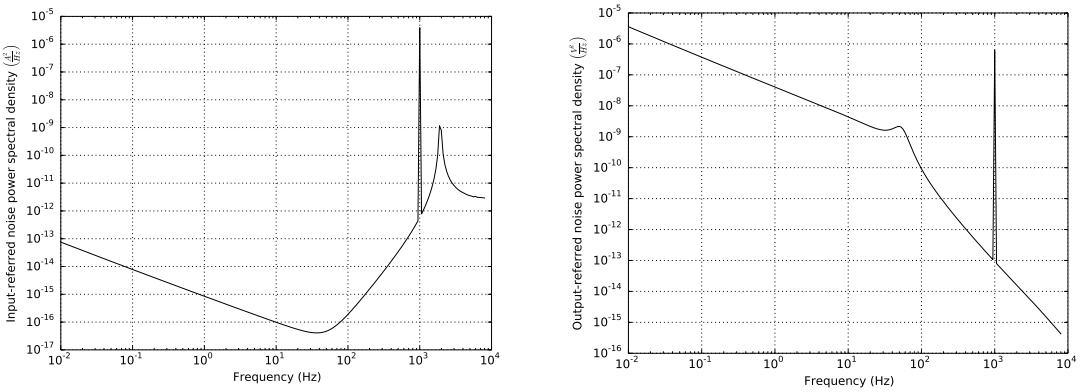


Figure 5.11: Lock-in amplifier gain.



(a) (b)

Figure 5.12: Input-referred (a) and output-referred (b) noise spectral density of the lock-in amplifier.

are given for this work, and it can be perceived that the consideration of the noise of the low-pass filter, associated with the frequency translation operated by the mixer, influences the input-referred noise of the whole system.

Table 5.3: Characteristics of the various designed lock-in amplifiers

	Power supply (V)	Power dissipation (mW)	Area (mm^2)	Input frequency range	Input refered noise	Gain
[18]	±2.5	25	6.5	2 - 50 KHz	17 nV/$\sqrt{Hz}$@20 KHz (LNA)	51 - 109 dB
[5]	2		5	1/10 KHz	<20 nV/$\sqrt{Hz}$@1 KHz <20 nV/$\sqrt{Hz}$@10 KHz (LNA)	40 - 80 dB
[6]	2			11/17/77 Hz	34 nV/$\sqrt{Hz}$@77 Hz (LNA)	
[11]				100 KHz	2 pA/$\sqrt{Hz}$@100 KHz (photoreceiver)	
[12]	3.3±0,3	110	2.5		15 nV/$\sqrt{Hz}$@20 KHz (LNA)	36.2 - 56.2 dB
[14]	1.8	2	2	10 - 100 KHz		
[13]	3.3±0.3	110	2.5	30 KHz	15 nV/$\sqrt{Hz}$@20 KHz (LNA)	36.2 - 56.2 dB
[7]	±1	3	5	77 Hz	34 nV/$\sqrt{Hz}$@77 Hz (LNA)	
[15]	3.3	12.79		13 - 25 KHz		
[8]				77 Hz		
[9]				77 Hz		126 dB
[19]	1.8	0.3509	0.013	1/10 KHz	28.1 uVrms	22.7 - 40 dB
[20]	1.8	0.3514	0.013	1/10 KHz	5.9 nV/$\sqrt{Hz}$@1 kHz	20.9 - 39.5 dB
[17]	1.2	3.7	0.16	10 MHz	3.8 nV/$\sqrt{Hz}$@10 MHz (LNA)	70 dB
[10]	1.8	2		2.5 - 25 Hz		80 dB
[22]	1.8	37	5	15 - 20 MHz		
[16]				13 - 26 KHz		56 dB
[21]	1.8	0.417	0.013	0.6 - 125 KHz		24.7 - 42 dB
This work	1.8	0.275	0.37438	200 Hz	68 pA/$\sqrt{Hz}$@200 Hz (TIA) 40 nA/$\sqrt{Hz}$@200 Hz (LIA)	76 - 87 dBΩ

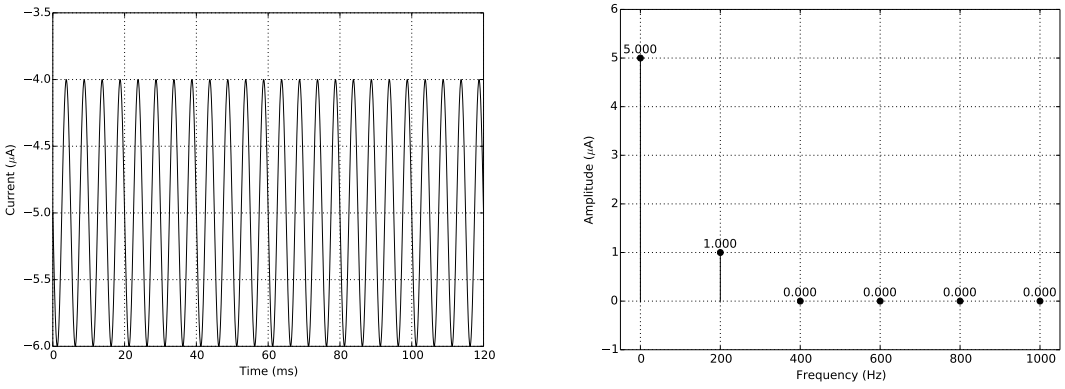
5.4.1 Simulation under nominal conditions and without interference

To better understand and verify the working principle of the lock-in amplifier, a simulation of the entire system under nominal conditions and, at first, without interference, has been carried out. The following figures show the signals and their respective discrete Fourier transforms (DFTs) in certain nodes of the system, which are the inputs and outputs of the various subblocks shown if Figure 2.8.

A simple sinusoidal input signal was used to simplify simulation and visualization (Figure 5.13), but simulations are representative of an amplitude modulated signal, as the spectrum of the modulated signal would appear around the 200 Hz impulse, representing the carrier wave spectrum. This input narrow band signal has a bandwidth smaller than that of the low-pass filter, and occupies a small frequency band around the 200 Hz impulse.

The DFT plots are generated based on the period after which the wave signal has achieved steady state, that is, from the time interval between 100 and 120 milliseconds of the transient simulation, and using a rectangular window and 2048 samples. This settings generates a DFT plot with a 50 Hz resolution. The frequencies where the DFT values are more significant are the multiples of 200 Hz. As the DFT values of frequency components lying between the 200 Hz multiples are orders of magnitude smaller than those at multiples of 200 Hz, they were ignored in the plot, to enable the annotation of a more precise DFT value without cluttering.

Figure 5.13 represents the input photocurrent i_p as a sinusoidal signal composed by a large -5 μA DC component and a small fundamental 1 μA component at 200 Hz.

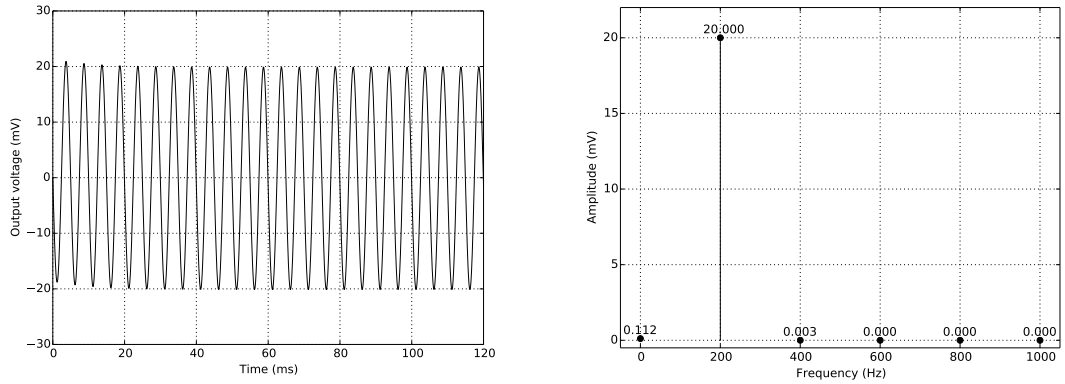


(a) (b)

Figure 5.13: Lock-in amplifier input photocurrent signal (a) and its DFT (b).

After passing through the TIA, the photocurrent has its DC component attenuated (Figure 5.14), while the fundamental component is amplified by a factor

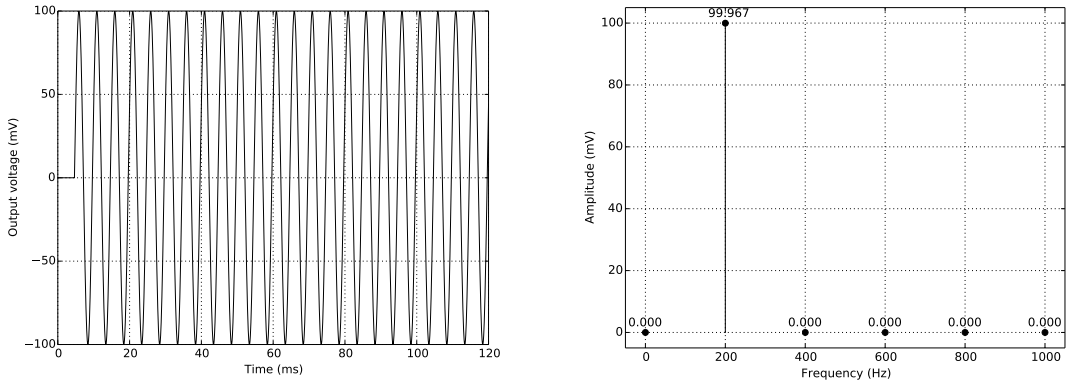
expressed by Equation 3.5, due to the combined action of the TIA and the DC photocurrent rejection feedback circuit. A tinny second harmonic appears, owing to the nonlinearity of the amplifier.



(a) (b)

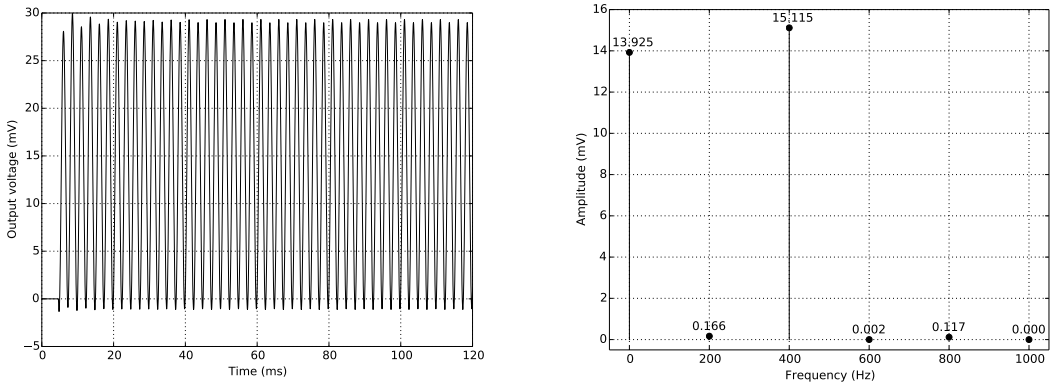
Figure 5.14: Differential signal waveform at the TIA output (a) and its DFT (b).

By means of the LO reference (Figure 5.15), the TIA output is processed in the mixer, generating the response shown in Figure 5.16. Here, the LO reference has the same phase and frequency as those of the RF signal. In this condition, the mixer amplifies the RF signal and operates over the RF frequency spectrum by translating half of the resulting component to DC and the other half to a frequency twice greater than the LO and RF signal frequencies. Here, a sinusoidal signal is used for the LO as, in the frequency domain, it is represented by a single impulse, but a square LO is commonly used, even though it will generate a large number of harmonic components. This LO wave signal is used in all simulations in what follows.



(a) (b)

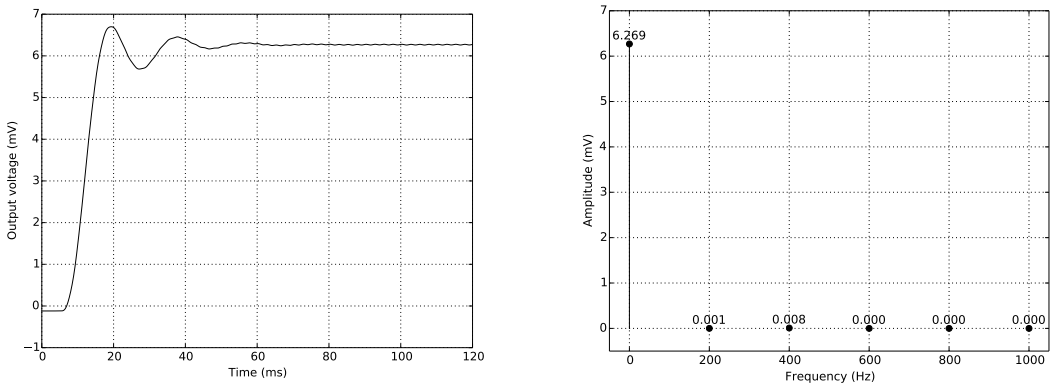
Figure 5.15: LO signal (a) and its DFT (b).



(a) (b)

Figure 5.16: Waveform at the output of the mixer (a) and its DFT (b).

The signal in Figure 5.16 is then filtered by the third-order Chebyshev low-pass filter at the lock-in amplifier output, resulting in the DC signal shown in Figure 5.17. As expected, the signal reduces by fifty percent the DC component, as the filter was synthesized through a doubly terminated ladder, while largely attenuating frequency components above 50 Hz. Small magnitude, higher harmonics cause a small ripple at the output.



(a) (b)

Figure 5.17: Lock-in amplifier output signal (a) and its DFT (b).

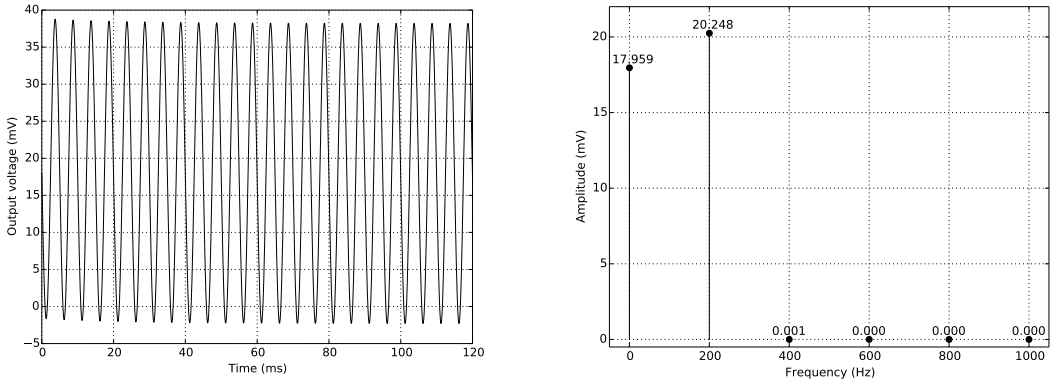
Under nominal conditions, it can be observed that the simulations agree well with the theoretical results obtained in Section 2.4.

5.4.2 Monte Carlo simulation without interference

To evaluate the influence of mismatch and process variations over the operation of the lock-in amplifier, a Monte Carlo simulation with 200 runs was performed, where the results of a particular run was picked to be shown in this section. All

runs presented similar behaviors of the system in nominal conditions, presented in Section 5.4.1. The simulation run shown here was chosen as an attempt to demonstrate the performance of one of the worst representative cases, with large offsets and ripple at the output.

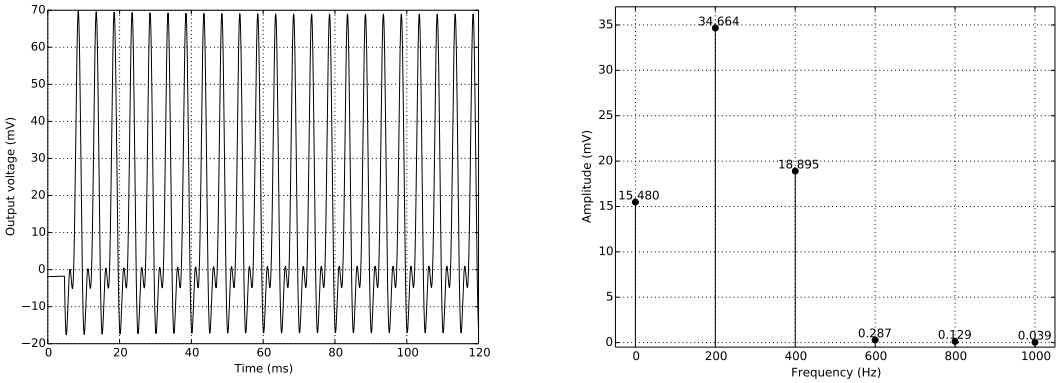
Figure 5.18, which can be compared with Figure 5.14, presents a significant offset appears at the output of the transimpedance amplifier. This offset is inherent to the amplifier and, if its magnitude presents a sufficiently large value, mixer operation can be impaired.



(a) (b)

Figure 5.18: Differential signal waveform at the TIA output (a) and its DFT (b).

As explained previously, mixer operation translates half of the signal to DC and the other half to 400 Hz, but Figure 5.19 also shows that the DC offset was translated to 200 Hz. Yet, mismatch and process variations could contribute to make part of the LO reference leak through the mixer and appear at its output, at 200 Hz, contributing with an increase of the component at that frequency.

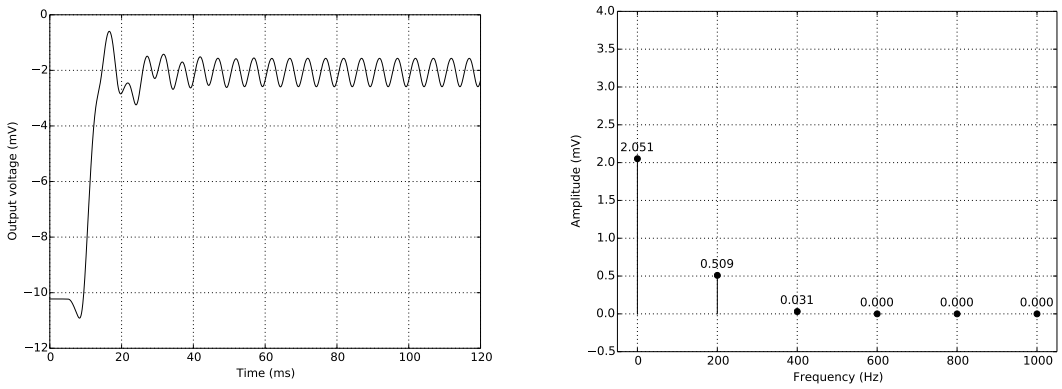


(a) (b)

Figure 5.19: Waveform at the output of the mixer (a) and its DFT showing an undesired component in 200 Hz due to the TIA offset (b).

In this simulation, the mixer presents a slightly negative offset, which can be perceived in Figure 5.19a, as the waveform starts at a shifted position with respect to zero. This offset contributes to the difference in magnitude between the frequency components in DC and in 400 Hz that, ideally, should be equal.

The consequence of the TIA offset, as can be seen in Figure 5.20, is that the filter was not capable of completely removing the 200 Hz undesired component, and a significant ripple appears at the lock-in amplifier output.



(a) (b)

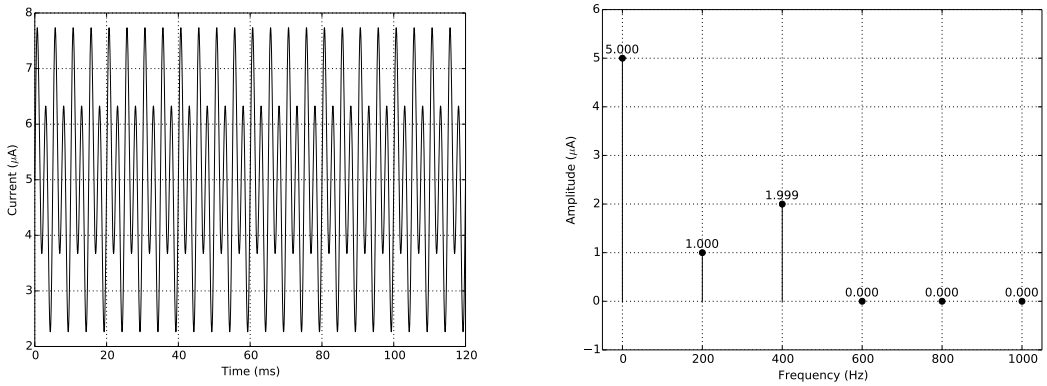
Figure 5.20: Lock-in amplifier output signal (a) showing ripple and its DFT (b) presenting the magnitude of the high order components responsible for this ripple.

Due to the idiosyncrasies of such high time constant Gm-C filter, a high offset will generally appear at the output of the filter. This offset can be noted in Figure 5.20a, where, due to the offset, the wave signal starts near the -10 mV value. In practice, to determine the offset magnitude, it is sufficient to remove the input signal and observe the lock-in amplifier output. The determination of this offset value is essential for the adjustment of the measurement system and the attainment of meaningful measurements.

5.4.3 Simulation under nominal conditions and with interference

To evaluate the reliability of the lock-in amplifier operation under the influence of interfering signals, the following simulations were conducted under nominal conditions and with an interfering signal with two times the magnitude and spaced from the signal of interest by 200 Hz (Figure 5.21). The input signal still presents a DC component, that should be mitigated by the control loop around the transimpedance amplifier.

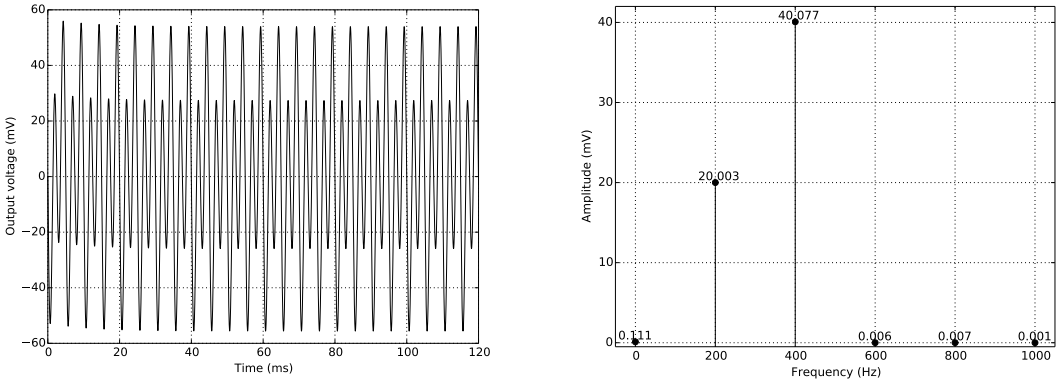
Here, the interference is added to the input signal and is present at the input of the lock-in amplifier. It is not coupled to any internal net. After passing through the



(a) (b)

Figure 5.21: Lock-in amplifier input photocurrent signal superposed with a interference signal at 400 Hz (a) and its DFT (b).

transimpedance amplifier, the signal and interference are amplified by the same factor, while the DC component is attenuated due to the frequency response characteristic of the transimpedance amplifier associated with the DC photocurrent rejection loop (Figure 5.22).

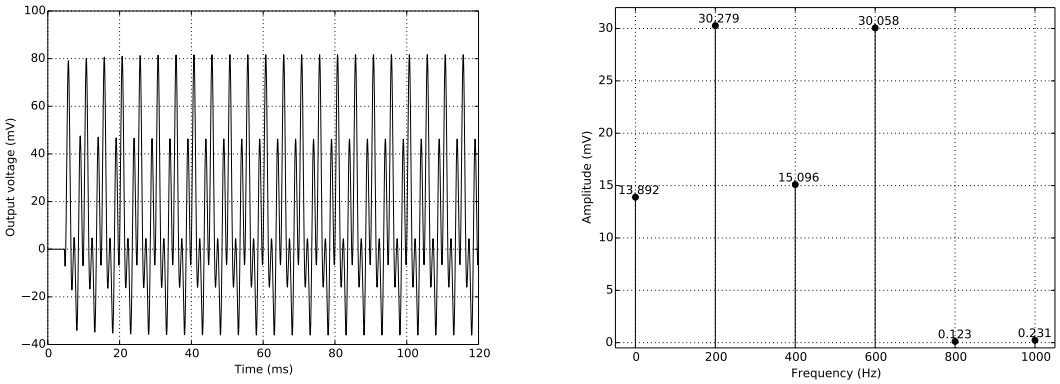


(a) (b)

Figure 5.22: Differential signal waveform at the TIA output with interference (a) and its DFT (b).

The mixer operates over the signal as expected (Figure 5.23b), shifting half of it to DC and the other half to two times its frequency. However, the frequency shift promoted by the mixer makes part of the interference signal to be shifted toward DC, in this particular case, half the interference signal is shifted to 200 Hz and half to 600 Hz. The filter should be sharp enough to be able to reject the component near DC and avoid ripples in the output.

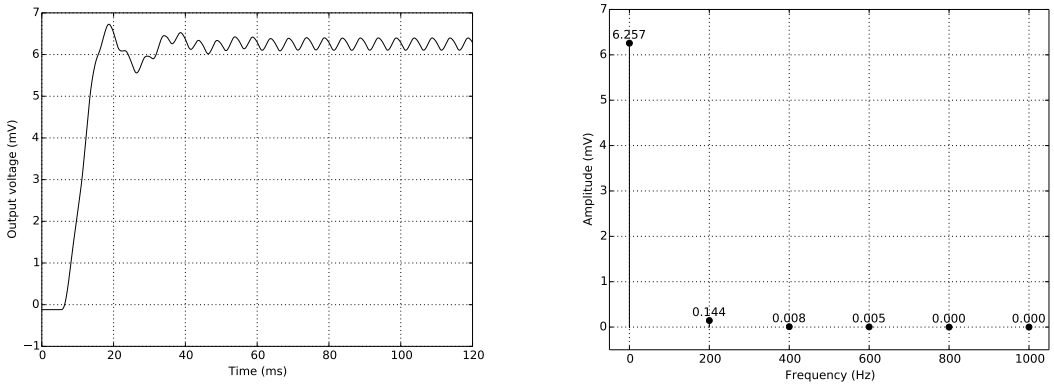
Figure 5.24 shows that the component at 200 Hz, relative to the interfering signal was highly attenuated, but not sufficiently to avoid ripple at the output.



(a) (b)

Figure 5.23: Waveform at the output of the mixer (a) and its DFT (b).

Nevertheless, the scenario considered here is an extreme one, with an interference very near and much larger than the signal.



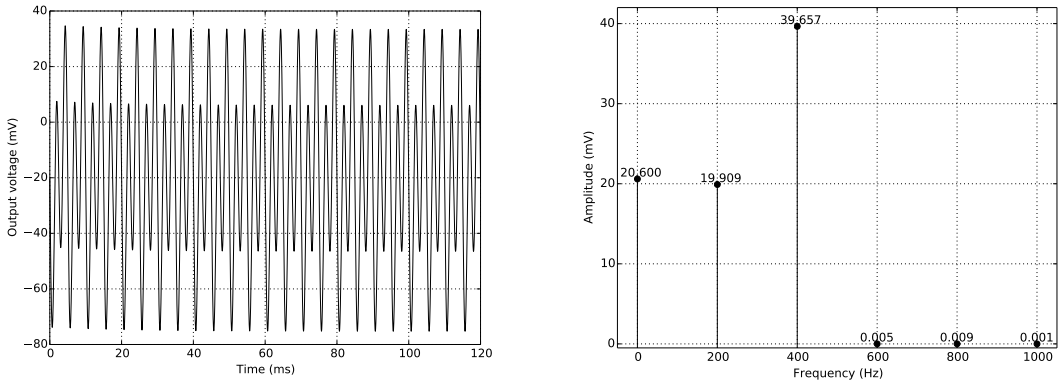
(a) (b)

Figure 5.24: Lock-in amplifier output signal (a) with small ripple and its DFT (b) showing the magnitude of the high order components responsible for the ripple.

5.4.4 Monte Carlo simulation including interference

To take into account mismatch and process variations, and thus obtain a more realistic prognostic of the lock-in amplifier behavior, 200 Monte Carlo runs were performed over the same condition of the previous subsection. Similarly to what was done in Section 5.4.2, a single run, representative of one of the worst cases was chosen to be presented here, one with large offsets and ripple.

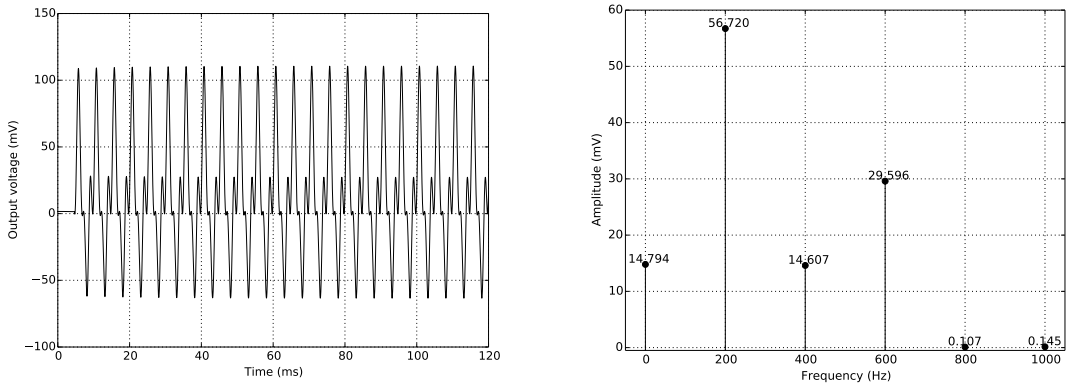
Figure 5.25 shows a significant offset at the output of the transimpedance amplifier due to mismatch, but signal and interference are amplified as expected. Compared to Figure 5.23, Figure 5.26 shows a even more unfavorable situation. Here,



(a) (b)

Figure 5.25: Differential signal waveform at the TIA output (a) and its DFT (b).

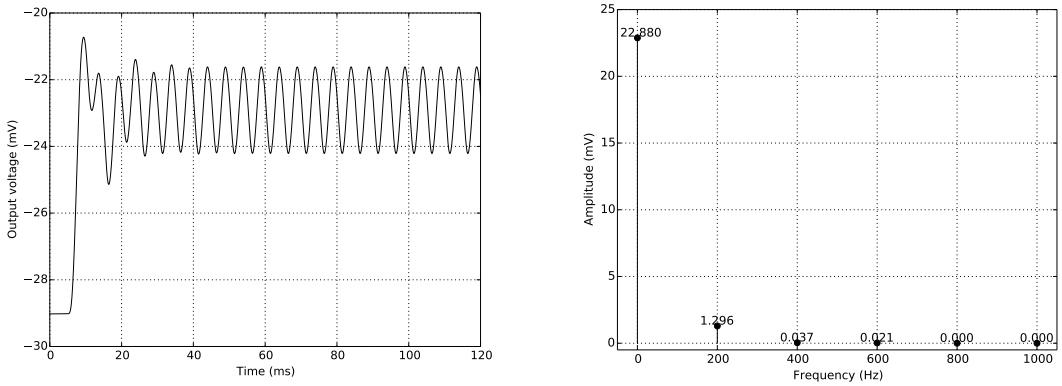
beyond half the interference that is shifted toward DC, the offset component is also shifted, falling exactly at 200 Hz, adding with the interference component, and creating a even higher component that should be suppressed to not generate ripple at the system output.



(a) (b)

Figure 5.26: Waveform at the output of the mixer (a) and its DFT (b) showing an undesired component at 200 Hz owed to the translations of part of the interference and part of the DC component due to the TIA offset.

As shown in Figure 5.27, the component was still sufficiently attenuated to avoid significant ripple. Notwithstanding the large ripple at the lock-in amplifier output, it is convenient to remember that the results presented here are representative of one of the worst cases obtained in the Monte Carlo analysis, and the hypothetical scenario simulated here is challenging for any system. It is also convenient to point out that, despite the large ripples and offsets presented, none of the runs completely failed to present a coherent response, what suggests a reasonable resilience against mismatch and process parameters variations.



(a) (b)

Figure 5.27: Lock-in amplifier output signal (a) with significant ripple and its DFT (b) showing the magnitude of the high order components causing the ripple.

5.4.5 Bench evaluation tests

A printed circuit board (PCB) was designed to evaluate the manufactured integrated circuit. The board was designed in CadSoft Eagle PCB design software, and fabricated in a prototyping machine generously provided by the IEN (Instituto de Energia Nuclear).

The fabricated test board was inspected and revealed to be ready to work properly, but, early on, it was verified that the integrated circuit consumes an unexpected huge current (0.64 A) when its pad ring is powered, without even powering any circuit (as each circuit has its own power pin, in addition to the pad ring power pin). It was found that this current does not flow through the developed circuits. The tests suggest that this huge current propagates through the pad ring and is probable caused by a wrong editing made in the layout of the pads provided by the foundry, with the intent to correct an unexpected DRC error.

Chapter 6

Conclusions

The work objective was accomplished, as the architecture of an analog single-phase lock-in amplifier was proposed and designed, and its feasibility was demonstrated by means of post-layout simulations that adhere to the theoretical predictions. A physical prototype was manufactured and is being tested in the laboratory to confirm the theory.

The proposed architecture presents some interesting features not commonly seen in other designs, as a fully-differential system and constituent blocks, including the unconventional differential sensing of the unbiased photodiode. It also carried out the integrating of the output low-pass filter, that demands a cut-off frequency that tends toward DC and a steep characteristic.

In this project, a DC photocurrent rejection circuit was implemented to attenuate the DC photocurrent component before it reaches the input amplifier, avoiding its saturation.

In addition to the advantage mentioned above, the DC photocurrent rejection circuit allows biasing the photodiode with a virtually zero voltage, that compared to the other operating modes (photovoltaic and photoconductive), provides a more linear relationship between the incident radiation and the generated current, and minimizes the shot noise inherent to the photodetector.

The transimpedance amplifier topology is also an atypical characteristic of this work. It was inspired by a differential-in, differential-out instrumentation amplifier and presents extremely large CMRR and PSRR.

It was shown through post-layout simulations that the lock-in amplifier can accomplish its intended task, by rejecting an undesired DC photocurrent component, amplifying the current signal and applying the demodulation process to obtain a DC voltage level that is proportional to the input signal amplitude.

Due to its low power supply and low frequency of operation, the developed lock-in amplifier presents the smallest power dissipation among all the surveyed works in the literature (Table 5.3). It also shows a small area, even integrating the synchronous

demodulator low-pass filter.

In view of the dominance of flicker noise in lower frequencies, the input referred noise of the design is more than an order of magnitude bigger than that of [11], that works in a much bigger frequency, where thermal noise dominates. Yet, augmenting the demodulator low-pass frequency gain, the lock-in amplifier input referred noise can be made as low as 12 nA/$\sqrt{Hz}$@200 Hz.

6.1 Suggestions for future works

As the entire design of a complete silicon integrated analog lock-in amplifier is a large amount of work for a single student to accomplish in the limited time of a master course, some functionalities unimplemented in this work, are left here as possible future works:

- Implementation of a structure that enables the adjustment of the transimpedance gain. This could be accomplished by a single FET, or a R/2R or M/2M ladder network;
- Design of a circuit to automatically synchronize the LO and RF signals;
- An automatic tuning circuit to adjust the cutoff frequency of the low-pass filter, or a scheme to enable its manual adjustment;
- Implementation of a two-phase lock-in amplifier.

Additionally, the research of alternative design solutions could be pursuit, as for example:

- Investigate other types of filters, such as switched-capacitor or switched-current filters in place of the Gm-C filter, or the employment of current-conveyors to emulate capacitors that have large capacitance values;
- Design for a mixer topology with improved linearity and resilient to offsets.

Bibliography

[1] FIDANBOYLU, K., EFENDIOĞLU, H. S. "Fiber Optic Sensors and Their Applications". In: *5th International Advanced Technologies Symposium (IATS'09)*, pp. 1–6, May 2009.

[2] BERGHMANS, F., THIENPONT, H. "Plastic optical fibers for sensing applications". In: *Optical Fiber Communications Conference and Exhibition (OFC), 2014*, pp. 1–3, March 2014.

[3] YIN, S., RUFFIN, B., YU, F. *Fiber Optic Sensors*. Second ed. Boca Raton, CRC Press, 2008.

[4] RODRIGUES, D. M. C. *Desenvolvimento e caracterização de sensores a fibra óptica plástica para refratometria baseados em modulação de amplitude*. Tese de Mestrado, Universidade Federal do Rio de Janeiro, Rio de Janeiro, 2013.

[5] FERRI, G., LAURENTIIS, P. D., D'AMICO, A., et al. "A low-voltage integrated {CMOS} analog lock-in amplifier prototype for {LAPS} applications", *Sensors and Actuators A: Physical*, v. 92, n. 1–3, pp. 263 – 272, 2001. ISSN: 0924-4247. doi: http://dx.doi.org/10.1016/S0924-4247(01)00581-7. Available in: <`http://www.sciencedirect.com/science/article/pii/S0924424701005817`>. Selected Papers for Eurosensors {XIV}.

[6] DE MARCELLIS, A., FERRI, G., PATRIZI, M., et al. "An integrated analog lock-in amplifier for low-voltage low-frequency sensor interface". In: *Advances in Sensors and Interface, 2007. IWASI 2007. 2nd International Workshop on*, pp. 1–5, June 2007. doi: 10.1109/IWASI.2007.4420033.

[7] D'AMICO, A., MARCELLIS, A. D., CARLO, C. D., et al. "Low-voltage low-power integrated analog lock-in amplifier for gas sensor applications", *Sensors and Actuators B: Chemical*, v. 144, n. 2, pp. 400 – 406, 2010. ISSN: 0925-4005. doi: http://dx.doi.org/10.1016/j.snb.2009.01.045. Available in: <`http://www.sciencedirect.com/science/`

article/pii/S092540050900063X>. 22nd International Conference on Eurosensors Dresden, Germany, 7-10 September 2008.

[8] MARCELLIS, A. D., GIANSANTE, A. D., FERRI, G., et al. "Analog automatic lock-in amplifier for very low gas concentration detection", *Procedia Engineering*, v. 5, n. 0, pp. 200 – 203, 2010. ISSN: 1877-7058. doi: http://dx.doi.org/10.1016/j.proeng.2010.09.082. Available in: <http://www.sciencedirect.com/science/article/pii/S1877705810006296>. Eurosensor {XXIV} Conference Eurosensor {XXIV} Conference.

[9] DE MARCELLIS, A., FERRI, G., D'AMICO, A., et al. "A Fully-Analog Lock-In Amplifier With Automatic Phase Alignment for Accurate Measurements of ppb Gas Concentrations", *Sensors Journal, IEEE*, v. 12, n. 5, pp. 1377–1383, May 2012. ISSN: 1530-437X. doi: 10.1109/JSEN.2011.2172602.

[10] DE MARCELLIS, A., FERRI, G., MANTENUTO, P., et al. "A new single-chip analog lock-in amplifier with automatic phase and frequency tuning for physical/chemical noisy phenomena detection". In: *Advances in Sensors and Interfaces (IWASI), 2013 5th IEEE International Workshop on*, pp. 121–124, June 2013. doi: 10.1109/IWASI.2013.6576057.

[11] XU, W., MATHINE, D. L., BARTON, J. K. "Analog CMOS Design for Optical Coherence Tomography Signal Detection and Processing", *Biomedical Engineering, IEEE Transactions on*, v. 55, n. 2, pp. 485–489, Feb 2008. ISSN: 0018-9294. doi: 10.1109/TBME.2007.905402.

[12] AZZOLINI, C., MAGNANINI, A., TONELLI, M., et al. "Integrated lock-in amplifier for contactless interface to magnetically stimulated mechanical resonators". In: *Design and Technology of Integrated Systems in Nanoscale Era, 2008. DTIS 2008. 3rd International Conference on*, pp. 1–6, March 2008. doi: 10.1109/DTIS.2008.4540233.

[13] AZZOLINI, C., MAGNANINI, A., TONELLI, M., et al. "A CMOS Vector Lock-in Amplifier for Sensor Applications", *Microelectron. J.*, v. 41, n. 8, pp. 449–457, ago. 2010. ISSN: 0026-2692. doi: 10.1016/j.mejo.2009.11.002. Available in: <http://dx.doi.org/10.1016/j.mejo.2009.11.002>.

[14] XU, J., MEYNANTS, G., MERKEN, P. "Low-power lock-in amplifier for complex impedance measurement". In: *Advances in sensors and Interfaces, 2009. IWASI 2009. 3rd International Workshop on*, pp. 110–114, June 2009. doi: 10.1109/IWASI.2009.5184779.

[15] HU, A., CHODAVARAPU, V. "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array", *Biomedical Circuits and Systems, IEEE Transactions on*, v. 4, n. 5, pp. 274–280, Oct 2010. ISSN: 1932-4545. doi: 10.1109/TBCAS.2010.2051438.

[16] SANTHANALAKSHMI, M., PRABHU, D. V. "A Low-Power Analog Lock-In Amplifier for Bio-Medical Applications", *International Journal of Electrical, Electronics and Computer Systems (IJEECS)*, v. 2, pp. 32–39, 2014. ISSN: 2347-2820.

[17] XU, R. "Design of a Lock-in Amplifier for Terahertz Detector and Imager Arrays on Monolithic CMOS". Intel Science Talent Search 2013 Competition, 2012. Plano Senior High School.

[18] GNUDI, A., COLALONGO, L., BACCARANI, G. "Integrated lock-in amplifier for sensor applications". In: *Solid-State Circuits Conference, 1999. ESSCIRC '99. Proceedings of the 25th European*, pp. 58–61, Sept 1999.

[19] MAYA-HERNÁNDEZ, P., SANZ-PASCUAL, M. T., CALVO, B., et al. "A CMOS low-power lock-in amplifier". In: *Instrumentation and Measurement Technology Conference (I2MTC), 2012 IEEE International*, pp. 1804–1807, May 2012. doi: 10.1109/I2MTC.2012.6229269.

[20] MAYA-HERNANDEZ, P., SANZ-PASCUAL, M. T., CALVO, B. "A 1.8V-0.18μm CMOS lock-in amplifier for portable applications". In: *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*, pp. 668–671, May 2012. doi: 10.1109/ISCAS.2012.6272121.

[21] MAYA-HERNÁNDEZ, P. M., ÁLVAREZ SIMÓN, L. C., SANZ-PASCUAL, M. T., et al. "An Integrated Low-Power Lock-In Amplifier and Its Application to Gas Detection", *Sensors*, v. 14, n. 9, pp. 15880–15899, 2014. ISSN: 1424-8220. doi: 10.3390/s140915880. Available in: <`http://www.mdpi.com/1424-8220/14/9/15880`>.

[22] HU, A., CHODAVARAPU, V. P. "General-purpose High-speed Integrated Lock-in Amplifier with 30 dB Dynamic Reserve at 20 MHz", *Analog Integr. Circuits Signal Process.*, v. 75, n. 3, pp. 369–382, jun 2013. ISSN: 0925-1030. doi: 10.1007/s10470-013-0042-x. Available in: <`http://dx.doi.org/10.1007/s10470-013-0042-x`>.

[23] MEADE, M. L. *Lock-in Amplifiers: Principles and Applications (e-edition)*. IEE electrical measurement series. London, UK, Peter Peregrinus Ltd,

1983. ISBN: 9780906048948. Available in: <https://sites.google.com/site/lockinamplifiers/home>.

[24] JOVIĆ, O. "Susceptibility of ICs to Conducted Electromagnetic Interference". .

[25] RAZAVI, B. *Design of Analog CMOS Integrated Circuits*. 1 ed. New York, NY, USA, McGraw-Hill, Inc., 2001. ISBN: 0072380322, 9780072380323.

[26] CARUSONE, T. C., JOHNS, D. A., MARTIN, K. W. *Analog Integrated Circuit Design*. Analog Integrated Circuit Design. Hoboken, NJ, USA, Wiley, 2011. ISBN: 9780470770108.

[27] TSIVIDIS, Y., MCANDREW, C. *Operation and Modeling of the MOS Transistor*. The Oxford Series in Electrical and Computer Engineering Series. New York, NY, USA, Oxford University Press, 2011. ISBN: 9780195170153.

[28] TSIVIDIS, Y. P. "Integrated continuous-time filter design - an overview", *Solid-State Circuits, IEEE Journal of*, v. 29, n. 3, pp. 166–176, Mar 1994. ISSN: 0018-9200. doi: 10.1109/4.278337.

[29] SOARES, C. F. T. *Métodos para Aprimorar o Projeto e o Layout de Filtros Analógicos em Circuitos Integrados CMOS*. Tese de Doutorado, UFRJ/COPPE/Programa de Engenharia Elétrica, Rio de Janeiro, 2009.

[30] JESPERS, P. G. *The Gm/ID Methodology, a Sizing Tool for Low-voltage Analog CMOS Circuits: The Semi-empirical and Compact Model Approaches*. New York, NY, USA, Springer Publishing Company, Incorporated, 2012.

[31] BINKLEY, D. *Tradeoffs and Optimization in Analog CMOS Design*. Chichester, England, Wiley, 2008. ISBN: 9780470033692.

[32] LI, X., WU, W., GILDENBLAT, G., et al. *PSP 102.3 documentation*. Arizona State University and NXP-TSMC Research Center and Philips Research Europe, May 2008.

[33] *ENG-331: 0.18 um HV CMOS Process Parameters*. AMS, Unterpremstaetten, Austria, June 2013.

[34] ZAND, B., PHANG, K., JOHNS, D. "Transimpedance amplifier with differential photodiode current sensing". In: *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, v. 2, pp. 624–627 vol.2, Jul 1999. doi: 10.1109/ISCAS.1999.780842.

[35] ZAND, B., PHANG, K., JOHNS, D. "A transimpedance amplifier with DC-coupled differential photodiode current sensing for wireless optical communications". In: *Custom Integrated Circuits, 2001, IEEE Conference on.*, pp. 455–458, 2001. doi: 10.1109/CICC.2001.929821.

[36] XU, W., MATHINE, D., BARTON, J. "High-gain differential CMOS transimpedance amplifier with on-chip buried double junction photodiode", *Electronics Letters*, v. 42, n. 14, pp. 803–805, July 2006. ISSN: 0013-5194. doi: 10.1049/el:20061560.

[37] ARNAUD, A., GALUP-MONTORO, C. "Pico-A/V range CMOS transconductors using series-parallel current division", *Electronics Letters*, v. 39, n. 18, pp. 1295–1296, Sept 2003. ISSN: 0013-5194. doi: 10.1049/el:20030840.

[38] FIORELLI, R., ARNAUD, A., GALUP-MONTORO, C. "Series-parallel association of transistors for the reduction of random offset in non-unity gain current mirrors". In: *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, v. 1, pp. I–881–4 Vol.1, May 2004. doi: 10.1109/ISCAS.2004.1328336.

[39] ARNAUD, A., FIORELLI, R., GALUP-MONTORO, C. "Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors", *Solid-State Circuits, IEEE Journal of*, v. 41, n. 9, pp. 2009–2018, Sept 2006. ISSN: 0018-9200. doi: 10.1109/JSSC.2006.880606.

[40] GARRETT, P. H. *Advanced Instrumentation and Computer I/O Design: Real-Time Computer Interactive Engineering*. Hoboken, NJ, USA, Wiley, 2000. ISBN: 9780780360136.

[41] WRIGHT, P., OZANYAN, K., CAREY, S., et al. "Design of high-performance photodiode receivers for optical tomography", *Sensors Journal, IEEE*, v. 5, n. 2, pp. 281–288, April 2005. ISSN: 1530-437X. doi: 10.1109/JSEN.2004.841869.

[42] ALIOTO, M., PALUMBO, G. *Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL and SCL Digital Circuits*. Norwell, NA, USA, Springer, 2005. ISBN: 9781402028786. Available in: <`https://books.google.com.br/books?id=rv13_kMvjFEC`>.

[43] SOARES, C. F. T. "Circuitos Analógicos Integráveis para o Processamento de Sinais", Material de apoio as aulas.

[44] "CMP: Circuits Multi-Projets". `http://cmp.imag.fr/`. Accessed: 2016-07-21.

[45] ELLARD, D. J., ELLARD, P. A. "S-Q Course Book", November 2003. Available in: <http://ellard.org/dan/www/Courses/sq98_root.pdf>.

Appendix A

TIA Differential Gain Derivation

The expression for the TIA differential gain is derived below. For easy reference, the TIA schematic is copied here.

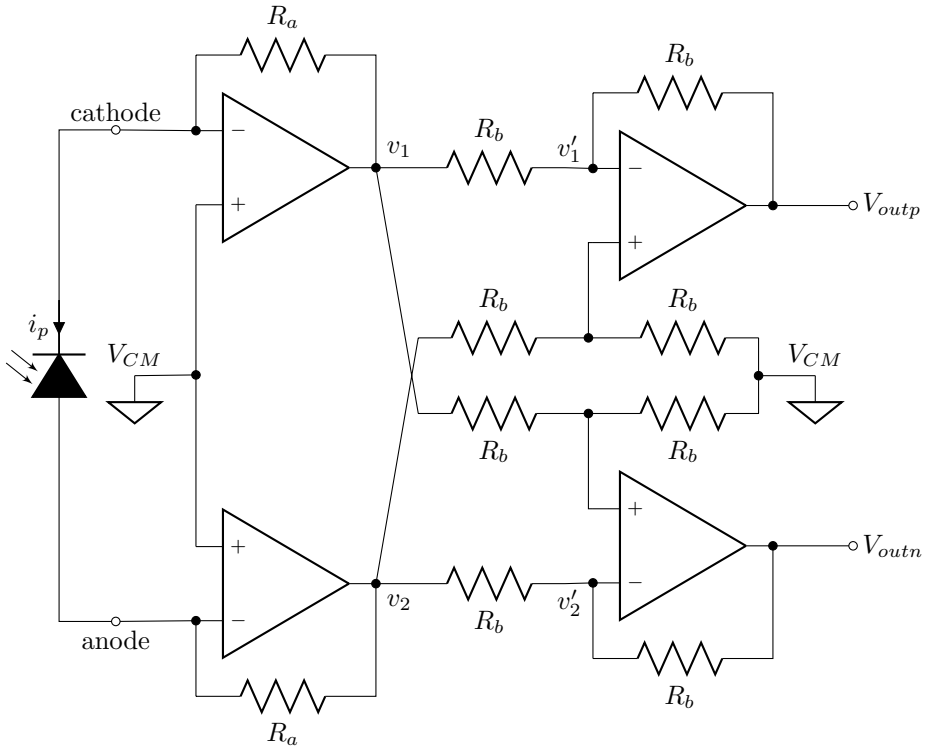


Figure A.1: Trasimpedance amplifier (TIA) topology.

$$\begin{cases} v_1 = V_{CM} + i_p R_a \\ v_2 = V_{CM} - i_p R_a \end{cases} \tag{A.1}$$

$$
\begin{aligned}
i_1 &= \frac{v_1 - V_{outp}}{2R} \\
v_1' &= V_{outp} + i_1 R = V_{outp} + \frac{v_1 - V_{outp}}{2R} R = \frac{2V_{outp} + v_1 - V_{outp}}{2} = \frac{1}{2}\left(V_{outp} + v_1\right)
\end{aligned}
\tag{A.2}
$$

$$
\begin{aligned}
i_2 &= \frac{v_2 - V_{outn}}{2R} \\
v_2' &= v_{outn} + i_2 R = V_{outn} + \frac{v_2 - V_{outn}}{2R} R = \frac{2V_{outn} + v_2 - V_{outn}}{2} = \frac{1}{2}\left(V_{outn} + v_2\right)
\end{aligned}
\tag{A.3}
$$

$$
\begin{aligned}
i_3 &= \frac{v_2 - V_{CM}}{2R} \\
v_1' &= V_{CM} + i_3 R = V_{CM} + \frac{v_2 - V_{CM}}{2R} R = \frac{2V_{CM} + v_2 - V_{CM}}{2} = \frac{1}{2}\left(V_{CM} + v_2\right)
\end{aligned}
\tag{A.4}
$$

$$
\begin{aligned}
i_4 &= \frac{v_1 - V_{CM}}{2R} \\
v_2' &= v_{CM} + i_4 R = V_{CM} + \frac{v_1 - V_{CM}}{2R} R = \frac{2V_{CM} + v_1 - V_{CM}}{2} = \frac{1}{2}\left(V_{CM} + v_1\right)
\end{aligned}
\tag{A.5}
$$

From A.2 and A.4, follows that:

$$
\begin{aligned}
\frac{1}{2}\left(V_{outp} + v_1\right) &= \frac{1}{2}\left(V_{CM} + v_2\right) \\
V_{outp} &= V_{CM} + \left(v_2 - v_1\right)
\end{aligned}
\tag{A.6}
$$

From A.3 and A.5, follows that:

$$
\begin{aligned}
\frac{1}{2}\left(V_{outn} + v_2\right) &= \frac{1}{2}\left(V_{CM} + v_1\right) \\
V_{outn} &= V_{CM} + \left(v_1 - v_2\right)
\end{aligned}
\tag{A.7}
$$

$$
\begin{aligned}
V_{outp} - V_{outn} &= V_{CM} + \left(v_2 - v_1\right) - \left[V_{CM} + \left(v_1 - v_2\right)\right] \\
&= 2\left(v_2 - v_1\right) \\
&= 2\left[V_{CM} - ipR_a - \left(V_{CM} + ipR_a\right)\right] \\
&= 2\left(-2ipR_a\right) \\
&= -4ipR_a
\end{aligned}
\tag{A.8}
$$

$$
\boxed{\text{transimpedance gain} = \frac{v_{outp} - v_{outn}}{i_p} = -4R_a}
\tag{A.9}
$$